



[Home](#)



# **OS-9<sup>®</sup> for ARM CL89712 Board Guide**

## **Version 4.7**



**RadiSys.**  
THE POWER OF WE

[www.radisys.com](http://www.radisys.com)

Revision A • July 2006

## Copyright and publication information

This manual reflects version 4.7 of Microware OS-9. Reproduction of this document, in part or whole, by any means, electrical, mechanical, magnetic, optical, chemical, manual, or otherwise is prohibited, without written permission from RadiSys Microware Communications Software Division, Inc.

## Disclaimer

The information contained herein is believed to be accurate as of the date of publication. However, RadiSys Corporation will not be liable for any damages including indirect or consequential, from use of the OS-9 operating system, Microware-provided software, or reliance on the accuracy of this documentation. The information contained herein is subject to change without notice.

## Reproduction notice

The software described in this document is intended to be used on a single computer system. RadiSys Corporation expressly prohibits any reproduction of the software on tape, disk, or any other medium except for backup purposes. Distribution of this software, in part or whole, to any other party or on any other system may constitute copyright infringements and misappropriation of trade secrets and confidential processes which are the property of RadiSys Corporation and/or other parties. Unauthorized distribution of software may cause damages far in excess of the value of the copies involved.

July 2006  
Copyright ©2006 by RadiSys Corporation  
All rights reserved.

EPC and RadiSys are registered trademarks of RadiSys Corporation. ASM, Brahma, DAI, DAQ, MultiPro, SAIB, Spirit, and ValuePro are trademarks of RadiSys Corporation.

DAVID, MAUI, OS-9, OS-9000, and SoftStax are registered trademarks of RadiSys Corporation. FasTrak, Hawk, and UpLink are trademarks of RadiSys Corporation.

† All other trademarks, registered trademarks, service marks, and trade names are the property of their respective owners.

---

# Table of Contents

---

## Chapter 1: Installing and Configuring OS-9 5

---

6	Development Environment Overview
7	Requirements and Compatibility
7	Host Hardware Requirements (PC Compatible)
7	Host Software Requirements (PC Compatible)
7	Target Hardware Requirements
7	Software Compatibility
8	OS-9 Architecture
10	Connecting the Target to the Host
10	Attaching the Cables
11	Building the OS-9 ROM Image
11	Coreboot
11	Bootfile
12	Using the Configuration Wizard
14	Configuring Coreboot Options
15	Configuring Bootfile Options
17	Transferring the ROM Image to the Target
17	Download Steps

## Chapter 2: Board Specific Reference 19

---

20	The Fastboot Enhancement
20	Overview
20	Implementation Overview
21	B_QUICKVAL
21	B_OKROM
22	B_1STINIT
22	B_NOIRQMASK
22	B_NOPARITY
23	Implementation Details

23	Compile-time Configuration
23	Runtime Configuration

---

<b>Appendix A: Board Specific Modules</b>	<b>25</b>
---	-----------

26	Low-Level System Modules
27	High-Level System Modules
28	Common System Modules List

---

<b>Product Discrepancy Report</b>	<b>31</b>
-----------------------------------	-----------

---

---

# Chapter 1: Installing and Configuring

## OS-9®

---

This chapter describes installing and configuring OS-9® on the ARM CDB89712 board. It includes the following sections:

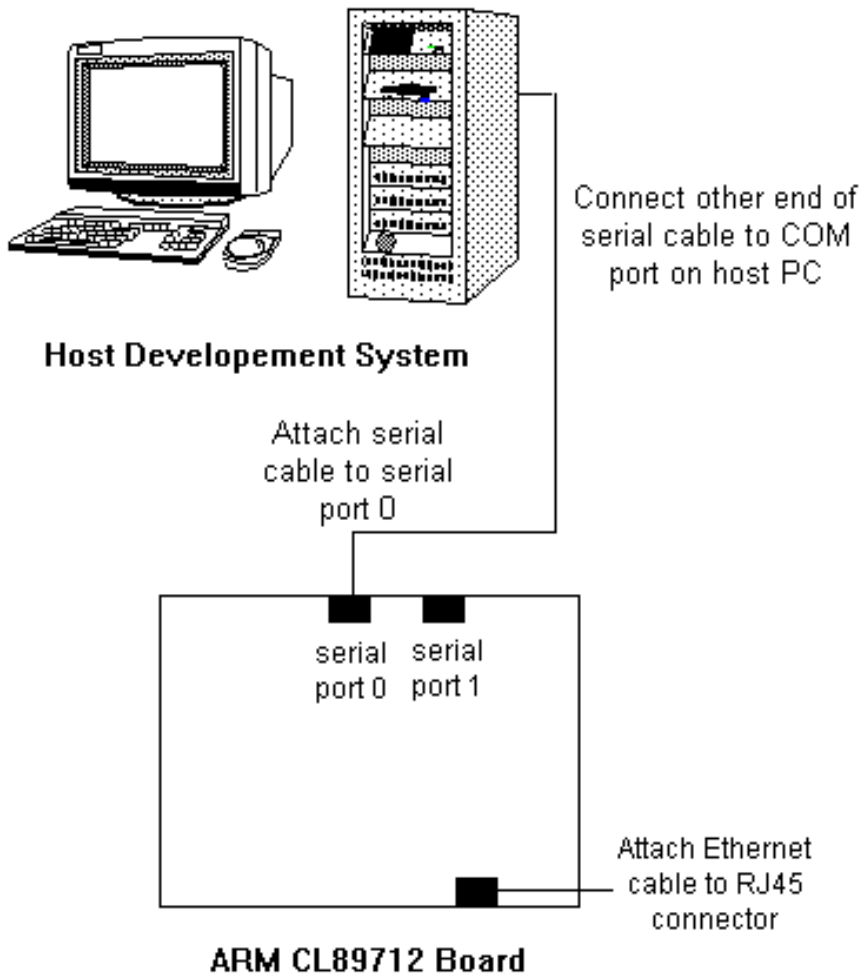
- **Development Environment Overview**
- **Requirements and Compatibility**
- **Building the OS-9 ROM Image**
- **Transferring the ROM Image to the Target**
- **Optional Procedures**



# Development Environment Overview

**Figure 1-1** shows a typical development environment for the ARM CDB89712 board. The components shown include the minimum required to enable OS-9 to run on the ARM CDB89712 board.

**Figure 1-1 ARM CL89712 Development Environment**



# Requirements and Compatibility

---

## Host Hardware Requirements (PC Compatible)

Your host PC must have the following minimum hardware characteristics:

- the recommended amount of RAM for the host operating system
- an Ethernet network card

## Host Software Requirements (PC Compatible)

Your host PC must have the following software installed:

- Windows 95, 98, ME, 2000, or NT 4.0
- Microware OS-9 for ARM

## Target Hardware Requirements

Your ARM CDB89712 evaluation board requires the following hardware:

- a power supply
- an RS-232 null modem serial cable (for serial console)
- an Ethernet cable or a second RS-232 null modem serial cable (for down-loading programs to the board)

## Software Compatibility

Microware OS-9 for ARM/StrongARM is compatible with the following software:

- RadiSys Hawk™ Version
- RadiSys SoftStax®

## Connecting the Target to the Host

---

Connecting the ARM CDB89712 to your host PC involves attaching the power, serial, and Ethernet cables to the reference board. Once you have the board connected, you can use the serial console in Hawk to verify the serial connection.



---

### Note

Before installing and configuring OS-9 on your evaluation board, refer to the hardware documentation for information on hardware setup.

---

## Attaching the Cables

Complete the following steps to attach the cables:

- 
- Step 1. Attach an Ethernet cable to the RJ45 connector labeled “10BASE-T”.
  - Step 2. Connect a serial cable to the connector labeled “Serial Port 0”.
  - Step 3. Connect the other end of the serial cable to a COM port on the host PC.
  - Step 4. Attach the power cable and plug the AC Adapter into a power outlet.
-



## Building the OS-9 ROM Image

---

The OS-9 ROM Image is a set of files and modules that collectively make up the OS-9 operating system. The specific ROM Image contents can vary from system to system depending on hardware capabilities and user requirements.

To simplify the process of loading and testing OS-9, the ROM Image is generally divided into two parts—the low-level image, called `coreboot`; and the high-level image, called `bootfile`.

### Coreboot

The coreboot image is generally responsible for initializing hardware devices and locating the high-level (or bootfile) image as specified by its configuration. Depending on the reference board's capabilities, the coreboot could be located on a FLASH part, a hard disk, or a floppy disk. It is also responsible for building basic structures based on the image it finds and passing control to the kernel to bring up the OS-9 system.

### Bootfile

The bootfile image contains the kernel and other high-level modules (initialization module, file managers, drivers, descriptors, applications). The image is loaded into memory based on the device selected from the boot menu. The bootfile image normally brings up an OS-9 shell prompt, but can be configured to automatically start an application.

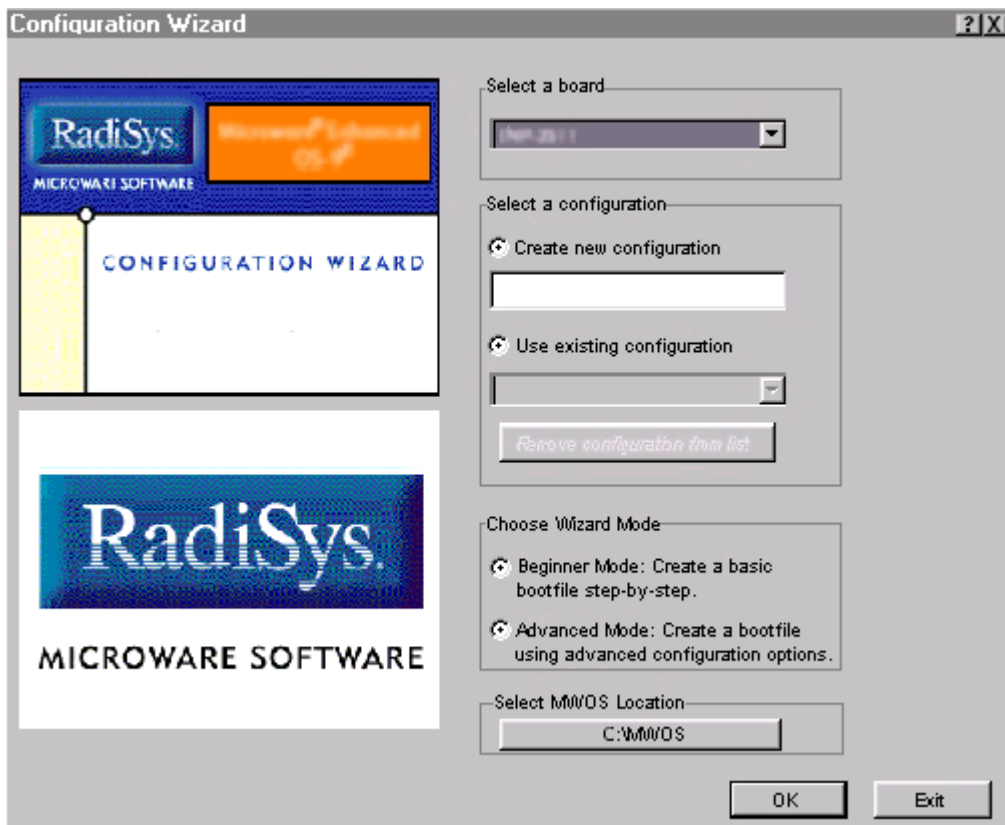
Microware provides a Configuration Wizard to create a coreboot image, a bootfile image, or an entire OS-9 ROM Image. The wizard can also be used to modify an existing image. The Configuration Wizard is automatically installed on the host PC during the OS-9 installation process.

## Starting the Configuration Wizard

The Configuration Wizard is the application used to build the coreboot, bootfile, or ROM image. To start the Configuration Wizard, perform the following steps:

- Step 1. From the Windows desktop, select **Start -> RadiSys -> Microware OS-9 for <product> -> Configuration Wizard**. You should see the following opening screen:

**Figure 1-2 Configuration Wizard Opening Screen**



- Step 2. Select your target board from the **Select a board** pull-down menu.

- Step 3. Select the **Create new configuration** radio button from the **Select a configuration** menu and type in the name you want to give your ROM image in the supplied text box. This names your new configuration, which can later be accessed by selecting the **Use existing configuration** pull down menu.
- Step 4. Select the **Advanced Mode** radio button from the **Choose Wizard Mode** field and click **OK**. The Wizard's main window is displayed. This is the dialog from which you will proceed to build your image. An example is shown in **Figure 1-3**.

**Figure 1-3 Configuration Wizard Main Window**



## Configuring Coreboot Options

From the Configuration Wizard's main window, complete the following steps to configure your coreboot options:

- 
- Step 1. Click the **Coreboot Main Configuration** button.
  - Step 2. Click on the **Debugger** tab. Make sure **Ethernet** is selected in the **Remote Debug Connection** area and **Remote** is selected in the **Select Debugger** area. Remote debugging is enabled so that system-state debugging can be performed in Hawk.
  - Step 3. Click on the **Ethernet** tab and enter the Ethernet address information in the address text boxes. For most situations you will need to fill out the following text boxes:
    - IP Address
    - IP Broadcast
    - Subnet Mask
    - IP Gateway
    - MAC Address

If you are uncertain of the values for these text boxes, contact your system administrator.
  - Step 4. Click **OK** to close the window. The default settings for the other tabs do not require modification.
-

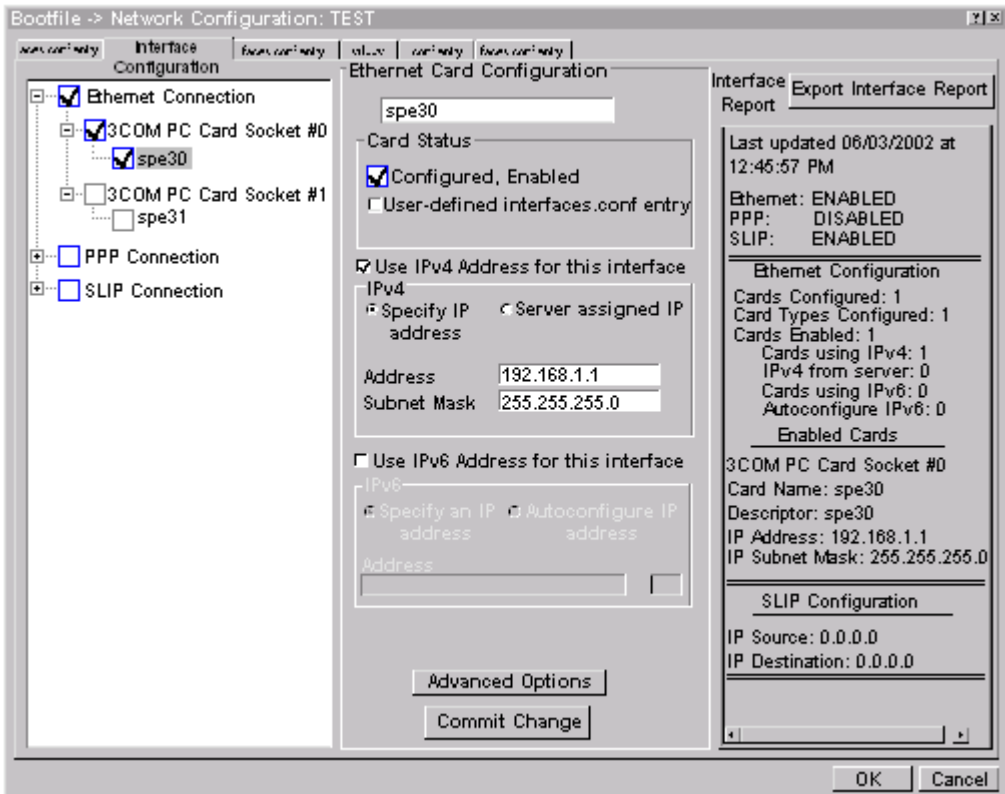
## Configuring Bootfile Options

Most of the default options in the dialogs that control the configuration of the bootfile are correct. There are a few functions, however, such as Ethernet, that require additional information in order to be configured correctly. To configure your bootfile options, complete the following steps:

- 
- Step 1. If you want to use the target board across a network, you will need to configure the Ethernet settings within the Configuration Wizard. To do this, select **Configure** -> **Bootfile** -> **Network Configuration** from the Wizard's main menu.

- Step 2. From the **Network Configuration** dialog, select the **Interface Configuration** tab. From here you can select and enable the interface. For example, you can select the appropriate Ethernet card from the list of options on the left and specify whether you would like to enable IPv4 or IPv6 addressing. **Figure 1-4** shows an example of the **Interface Configuration** tab.

**Figure 1-4 Bootfile -> Network Configuration -> Interface Configuration**



## For More Information

To learn more about IPv4 and IPv6 functionalities, refer to the **Using LAN** manual, included with this product CD.



---

## For More Information

Contact your system administrator if you do not know the network values for your board.

---

- Step 3. Once you have made your settings in the **Network Configuration** dialog, click **OK**.
  - Step 4. Click on the **SoftStax Setup** tab and select **Enable SoftStax**.
  - Step 5. Click **OK** to close the dialog box.
  - Step 6. Click on the **System Disk Configuration** button and verify that the default settings are acceptable to you.
  - Step 7. Leave the other default settings alone and click the **Build Images** button to display the **Master Builder** window.
  - Step 8. Select the following check boxes as they are appropriate to your setup:
    - SoftStax (SPF) Support
    - User State Debugging Modules
    - If you are using a RAM disk, select **Disk Support**.
    - If you are using a RAM disk, select **Disk Utilities**.
  - Step 9. Click **Coreboot + Bootfile** and click **Build**. This will build the ROM image that can be burned into flash memory. The name of the ROM image is `rom`.
  - Step 10. Click **Finish** and then select **File -> Save Settings** to save the configuration.
  - Step 11. Select **File -> Exit** to quit from the Configuration Wizard.
-

## Transferring the ROM Image to the Target

---

Once you have built a ROM image, you can transfer it to the on-board flash memory on target board. Microware supplies a utility called `cl_download` that performs this transfer. `cl_download` takes a binary file and transfers it across any COM port at any desired baud rate. By default, `cl_download` uses COM1 and a baud rate of 115200. The defaults can be changed via command line options. Below are some usage examples:

The following command uses COM1 AND 115200 baud:

```
$ cl_download rom
```

The following command uses COM3 AND 115200 baud:

```
$ cl_download rom 3
```

The following command uses COM3 AND 19200 baud:

```
$ cl_download rom 3 19200
```

On the ARM CDB89712 reference board, Serial Port 0 will receive the download. The target board must be put into flash burn/download mode. The ROM image must be programmed into flash and the board must be rebooted in its normal running mode. The following section describes how to do this.

### Download Steps

Complete the following steps to put the board in download mode:

- 
- Step 1. Open a DOS shell and navigate to the following directory:  
`<drive>:\mws\OS9000\ARMV4\PORTS\CDB89712\BOOTS\INSTALL\PORTBOOT`
  - Step 2. Remove power from the board.
  - Step 3. Close the JP31 jumper. The jumper is located near the center of the board by the processor.
  - Step 4. Apply power to the board.



Step 5. Run `cl_download` by typing the following command:

```
cl_download rom 1 19200
```

A message, “Waiting for the board to wakeup,” should appear.

Step 6. Press the **POR** button, then the **RESET** button, then the **WAKEUP** button. The board should begin receiving data.

If the board does not start to receive data, press each button again for at least one half of a second. Once the file has been downloaded and burned into flash memory, the message “Successfully programmed rom” appears. Repeat steps two through six if this message does not appear.

Step 7. Remove power from the board and open jumper JP31.

Step 8. Start HyperTerminal or the serial console in Hawk. Apply the following settings: 19200 baud rate, 8 bits, 1 stop bit, and no flow control.

Step 9. Apply power to the board and press **POR** followed by **RESET** and **WAKEUP**. The OS-9 bootstrap message appears in the terminal program’s window.

When you see the shell prompt “\$”, the board is booted and running OS-9.

---

## Optional Procedures

---

### Compressing the Bootfile Image

OS-9 bootfiles can be compressed to allow more modules to be loaded into a bootfile; this can be useful if you plan on storing your image on a small FLASH part or a floppy disk.



#### Note

The bootfile compression utility performs the compression at approximately a 2.5:1 ratio.

---

Complete the following steps to compress your image:

- Step 1. Verify that your coreboot contains the uncompress module. This module can be found in the pre-built ROM and coreboot images that were shipped with your Microware OS-9 product.



#### Note

The uncompress module must be included in order for the compression to execute properly.

---

- Step 2. Open the Configuration Wizard and select **Configure** -> **Coreboot** -> **Main Configuration** from the main menu.
- Step 3. Select the **Bootfile Compression** tab. Verify that the **Include bootfile uncompress module** box is checked and select OK.

- Step 4. When you are ready to build the image, open the **Master Builder** dialog. Verify that the **Compress Bootfile** box is checked and then press **Build** to begin the installing the image.
-



---

## Chapter 2: Board Specific Reference

---

This chapter contains porting information specific to the ARM CDB89712 board. It includes the following sections:

- **The Fastboot Enhancement**



# The Fastboot Enhancement

---

The Fastboot enhancements to OS-9 were added to address the needs of embedded systems that require faster system bootstrap performance. The Fastboot concept exists to inform OS-9 that the defined configuration is static and valid. This eliminates the dynamic search OS-9 usually performs during the bootstrap process. It also allows the system to perform for a minimal amount of runtime configuration. As a result, a significant increase in bootstrap speed is achieved.

## Overview

The Fastboot enhancement consists of a set of flags that control the bootstrap process. Each flag informs some portion of the bootstrap code of a particular assumption, and that the associated bootstrap functionality should be omitted.

One important feature of the Fastboot enhancement is the ability of the flags to become dynamically altered during the bootstrap process. For example, the bootstrap code might be configured to query dip switch settings, respond to device interrupts, or respond to the presence of specific resources that indicate different bootstrap requirements.

Another important feature of the Fastboot enhancement is its versatility. The enhancement's versatility allows for special considerations under a variety of circumstances. This can be useful in a system in which most resources are known, static, and functional, but whose additional validation is required during bootstrap for a particular instance (such as a resource failure).

## Implementation Overview

The Fastboot configuration flags have been implemented as a set of bit fields. One 32-bit field has been dedicated for bootstrap configuration. This four-byte field is contained within a set of data structures shared by

the kernel and the ModRom sub-components. Hence, the field is available for modification and inspection by the entire set of system modules (both high-level and low-level).

Currently, there are six-bit flags defined, with eight bits reserved for user-definable bootstrap functionality. The reserved user-definable bits are the high-order eight bits (31-24). This leaves bits available for future enhancements. The currently defined bits and their associated bootstrap functionality are listed in the following sections.

## **B\_QUICKVAL**

The `B_QUICKVAL` bit indicates that only the module headers of modules in ROM are to be validated during the memory module search phase. Limiting validation in this manner will omit the CRC check on modules, which may save you a considerable amount of time. For example, if a system has many modules in ROM, in which access time is typically longer than it is in RAM, omitting the CRC check will drastically decrease the bootstrap time. Furthermore, since it is rare that data corruption will occur in ROM, omitting the CRC check is a safe option.

In addition, the `B_OKRAM` bit instructs the low-level and high-level systems to accept their respective RAM definitions without verification. Normally, the system probes memory during bootstrap based on the defined RAM parameters. This method allows system designers to specify a possible range of RAM the system will validate upon startup; thus, the system can accommodate varying amounts of RAM. However, in an embedded system (where the RAM limits are usually statically defined and presumed to be functional) there is no need to validate the defined RAM list. Bootstrap time is saved by assuming that the RAM definition is accurate.

## **B\_OKROM**

The `B_OKROM` bit causes acceptance of the ROM definition without probing for ROM. This configuration option behaves similarly to the `B_OKRAM` option with the exception that it applies to the acceptance of the ROM definition.

## B\_1STINIT

The `B_1STINIT` bit causes acceptance of the first `init` module found during cold-start. By default, the kernel searches the entire ROM list passed up by the ModRom for `init` modules before it takes the `init` module with the highest revision number. Using the `B_1STINIT` in a statically defined system omits the extended `init` module search, which can save a considerable amount of time.

## B\_NOIRQMASK

The `B_NOIRQMASK` bit instructs the entire bootstrap system to not mask interrupts for the duration of the bootstrap process. Normally, the ModRom code and the kernel cold-start mask interrupts for the duration of the system startup. However, in systems with a well-defined interrupt system (systems that are calmed by the `sysinit` hardware initialization code) and a requirement to respond to an installed interrupt handler during startup, this option can be used. Its implementation will prevent the ModRom and kernel cold-start from disabling interrupts. (This is useful in power-sensitive systems that need to respond to “power-failure” oriented interrupts.)



---

### Note

Some portions of the system may still mask interrupts for short periods during the execution of critical sections.

---

## B\_NOPARITY

If the RAM probing operation has not been omitted, the `B_NOPARITY` bit causes the system to not perform parity initialization of the RAM. Parity initialization occurs during the RAM probe phase. The `B_NOPARITY` option is useful for systems that either require no parity initialization or only require it for “power-on” reset conditions. Systems that only require parity initialization for initial power-on reset conditions can dynamically use this option to prevent parity initialization for subsequent “non-power-on” reset conditions.



## Implementation Details

This section describes the compile-time and runtime methods by which you can control the bootstrap speed of your system.

### Compile-time Configuration

The compile-time configuration of the bootstrap is provided by a pre-defined macro, `BOOT_CONFIG`, which is used to set the initial bit-field values of the bootstrap flags. You can redefine the macro for recompilation to create a new bootstrap configuration. The new, over-riding value of the macro should be established as a redefinition of the macro in the `rom_config.h` header file or a macro definition parameter in the compilation command.

The `rom_config.h` header file is one of the main files used to configure the ModRom system. It contains many of the specific configuration details of the low-level system. Below is an example of how you can redefine the bootstrap configuration of your system using the `BOOT_CONFIG` macro in the `rom_config.h` header file:

```
#define BOOT_CONFIG (B_OKRAM + B_OKROM + B_QUICKVAL)
```

Below is an alternate example showing the default definition as a compile switch in the compilation command in the makefile:

```
SPEC_COPTS = -dNEWINFO -dNOPARITYINIT  
-dBOOT_CONFIG=0x7
```

This redefinition of the `BOOT_CONFIG` macro results in a bootstrap method, which accepts the RAM and ROM definitions without verification. It also validates modules solely on the correctness of their module headers.

### Runtime Configuration

The default bootstrap configuration can be overridden at runtime by changing the `rinf->os->boot_config` variable from either a low-level P2 module or from the `sysinit2()` function of the

`sysinit.c` file. The runtime code can query `jumper` or other hardware settings to determine which user-defined bootstrap procedure should be used. An example P2 module is shown below.



## Note

If the override is performed in the `sysinit2()` function, the effect is not realized until after the low-level system memory searches have been performed. This means that any runtime override of the default settings pertaining to the memory search must be done from the code in the P2 module code.

```
#define NEWINFO
#include <rom.h>
#include <types.h>
#include <const.h>
#include <errno.h>
#include <romerrno.h>
#include <p2lib.h>

error_code p2start(Rominfo rinf, u_char *gblbs)
{
    /* if switch or jumper setting is set... */
    if (switch_or_jumper == SET) {
        /* force checking of ROM and RAM lists */
        rinf->os->boot_config &= ~(B_OKROM+B_OKRAM);
    }
    return SUCCESS;
}
```

---

# Appendix A: Board Specific Modules

---

This chapter describes the modules specifically written for the ARM CDB89712 board. It includes the following sections:

- **Low-Level System Modules**
- **High-Level System Modules**
- **Common System Modules List**



## Low-Level System Modules

---

The following low-level system modules are tailored specifically for the ARM CDB89712 board. They are located in the following directory:

MWOS/OS9000/ARMV4/PORTS/CDB89712/CMDS/BOOTOBS/ROM

<code>cnfgdata</code>	contains low-level configuration data
<code>cnfgfunc</code>	provides access services to the <code>cnfgdata</code>
<code>commcnfg</code>	inits communication port defined in <code>cnfgdata</code>
<code>conscnfg</code>	inits console port defined in <code>cnfgdata</code>
<code>io89712</code>	low-level based serial IO driver
<code>l18900</code>	Low-level Ethernet ROM driver
<code>portmenu</code>	inits booters defined in the <code>cnfgdata</code>
<code>romcore</code>	bootstrap code
<code>tmr89712</code>	ROM timer services
<code>usedebug</code>	debugger configuration module

## High-Level System Modules

---

The following OS-9 system modules are tailored specifically for the ARM CDB89712 board.

Modules located in the following directory:

MWOS/OS9000/ARMV4/PORTS/CDB89712/CMDS/BOOTOBSJS

sc89712	Serial driver that supports baud rates up to 115200. Default Baud Rate is 19,200. Descriptors <code>/term</code> and <code>/t1</code> are assigned to Port 0. Descriptors <code>/term2</code> and <code>/t2</code> are assigned to Port 1.
tkarm	System clock module

Modules located in the following directory:

MWOS/OS9000/ARMV4/PORTS/CDB89712/CMDS/BOOTOBSJS/SPF

sp8900	Driver module for the Ethernet controller
spsc0	Descriptor for the Ethernet driver sp8900

Modules located in the following directory:

MWOS/OS9000/ARMV4/CMDS/BOOTOBSJS

vect110	Vector module for ARM
fpu	ARM FPU emulator

## Common System Modules List

---

The following low-level system modules provide generic services for OS9000 Modular ROM. They are located in the following directory:

MWOS/OS9000/ARMV4/CMDS/BOOTOBSJS/ROM

<code>bootsys</code>	provides booter registration services
<code>console</code>	provides console services
<code>dbgentry</code>	inits debugger entry point for system use
<code>dbgserv</code>	provides debugger services
<code>exception</code>	provides low-level exception services
<code>fdc765</code>	provides PC style floppy support
<code>flboot</code>	is a SCSI floptical drive disk booter
<code>flshcach</code>	provides low-level cache management services
<code>hlproto</code>	provides user level code access to protoman
<code>ide</code>	provides target-specific standard IDE support, including PCMCIA ATA PC cards
<code>llbootp</code>	provides bootp services
<code>llip</code>	provides low-level IP services
<code>llkermit</code>	provides a booter that uses kermit protocol
<code>llslip</code>	provides low-level SLIP services
<code>lltcp</code>	provides low-level TCP services
<code>lludp</code>	provides low-level UDP services
<code>notify</code>	provides state change information for use with LL and HL drivers

override	provides a booter that allows a choice between menu and auto booters
parser	provides argument parsing services
pcman	provides a booter that reads MS-DOS file system
protoman	provides a protocol management module
restart	provides a booter that causes a soft reboot of the system
romboot	provides a booter that allows booting from ROM
rombreak	provides a booter that calls the installed debugger
rombug	provides a low-level system debugger
scsiman	is a target-independent booter support module that provides general SCSI command protocol services
sndp	provides low-level system debug protocol
srecord	provides a booter that accepts S-Records
swtimer	provides timer services via software loops
tsboot	is a SCSI TEAC tape drive booter
type41	is a primary partition type

