Heterogeneous System Integration – A Key Technology for Future Microelectronic Applications

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Abstract

Heterogeneous system integration is one of the key topics for future system integration. Scaling of System on Chip (SoC) alone does not address today's requirements in terms of performance, functionality, miniaturization, low production cost and time to market of smart electronic system.
The traditional microelectronic packaging will more and more convert into complex system integration. "More than Moore" will be required due to tighter integration of system level components at the package level. This trend leads to advanced System in Package solutions (SiP) which require the synergy and a combination of wafer level and board integration technologies and which are rapidly evolving from a specialty technology used in a narrow set of applications to a high volume technology with wide ranging impact on electronics markets especially due to the high volume and very cost competitive consumer and communication market. Advanced SiP approaches explore the third dimension which results in complex system architectures that also require, beside new technologies and improved materials, adequate system design tools and reliability models. One of the most promising technology approaches is 3D packaging which involves a set of different integration approaches including stacked packages, silicon interposer with Through Silicon Vias (TSV) and embedding technologies.
The paper highlights future system and potential technical solutions.

1 Introduction

Requirements on packaging and system integration are today mainly driven by the consumer market especially by the wireless product segment (mobile phones, mp3 devices, multi media devices, etc.). Higher functionality, high miniaturization, high reliability and low production costs are in focus of developments.

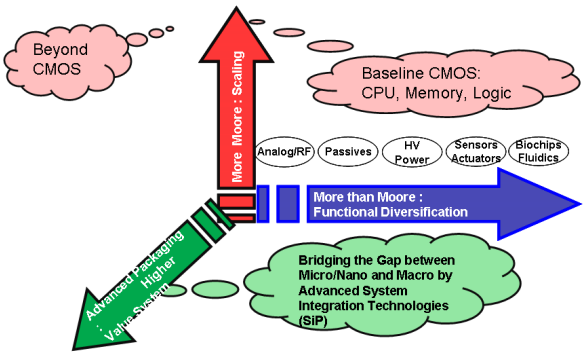


Figure 1 System Integration "More Moore" and "More than Moore" [1]

Besides increasing integration level and functionality on chip level according to Moore´s law "More Moore"– different components, e.g. µP, memory, passives, MEMS, etc., are integrated in one package as a system or subsystem. This technique is known as "System in Package" (SiP) - "More than Moore" (Figure 1). In SiPs different technologies from wafer and board level and different materials are used, whereas organic material as a substrate carrier is of high importance because of the low cost.
Figure 2 gives an overview about up-to-date categories of System in Package (SiP).

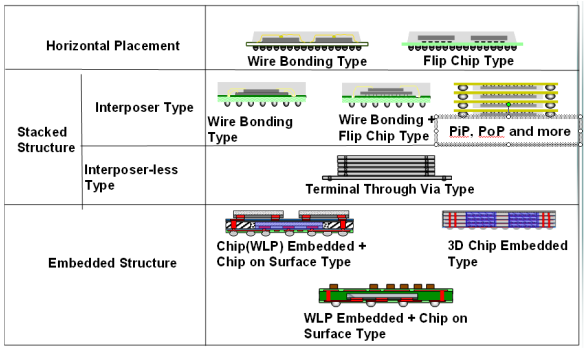


Figure 2 System in Package (SiP) Kategorien [2]

Present technologies enable the realization of organic substrates (PCB) with high density wiring and micro-vias.
Passive and active components are assembled on both sides of the substrate. The lateral required space can be reduced to a minimum by using CSP´s (Chip Size Packages) or Flip Chips. Figure 3 shows an example of a multifunctional board, assembled with a wide variety of components such as CSP, BGA, embedded devices, CoB FC, CSP-IP, MEMS. Further miniaturization requires 3D integration of components with stacked dies, wire bonded or flip chip

bonded to an carrier. Apart from miniaturization, in new applications signal frequencies of various GHz are required, which are difficult to realize due to long interconnection length on the PCB and the long wire bonds.

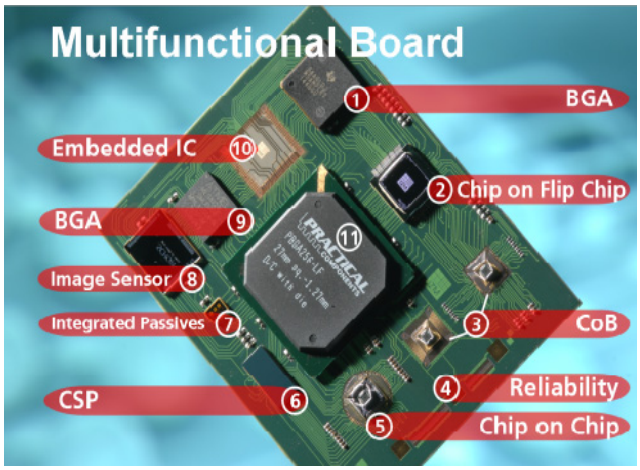


Figure 3 Multifunctional Board – assembled demonstration board with different electronic components

For signal integrity short and impedance controlled wiring are necessary. This can be realized e.g. with embedded components. Embedding implies the positioning of the conductor not only below but also on top of the embedded component. The component is electrically connected with the upper and/or the lower conductor layer.
Several manufacturers are currently developing this technique of "In Board Integration" or are already in a progressive state of implementation into production. Furthermore, embedding of components allows the linkage of electrical and optical signal paths, which in the future will be of main importance, especially for fast data transmission.

2 3D System Integration

2.1 Drivers for 3D System Integration

In general, the introduction of 3D integration technologies into the production of microelectronic systems are driven by

- Form factor: Reduction of system volume, weight and footprint,
- Performance: Improvement of integration density and reduction of interconnect length leading to improved transmission speed and reduced power consumption,
- High volume low cost production,
- Applications: e.g. image sensors, memory stacks, µp/ memory modules, sensor nodes.

3D integration is a solution to overcome the "wiring crisis" caused by signal propagation delay both, at board and at chip level, because it allows minimal interconnection lengths. The realization of advanced micro systems, as e.g. 3D image processors, will be mainly driven by the enhancement of performance while low production cost have to be in focus.
3D integration technologies enable the combination of different optimized base technologies, e.g. MEMS, CMOS, with the potential of low cost fabrication through high yield and high miniaturization degree: Device stacks (e.g. controller and memory layers) fabricated with optimized 3D integration technologies will show reduced production costs in competition to monolithic integrated SoCs. [3], [4], [5] Furthermore, new multi-functional micro-electronic systems such as ultra-miniaturized sensor nodes for applications in distributed wireless sensor networks can be realized (Figure 4). [6]
3D integration technologies have to be applied because of their relevant benefits: Extreme system volume reduction, reduction of power consumption, reliability improvement and low cost fabrication to meet high volume market requirements.

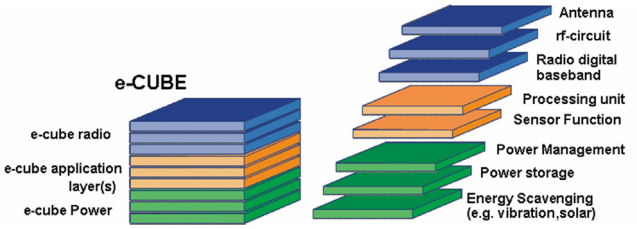


Figure 4 Schematic 3D construction for wireless sensor node [7], [8]

2.2 3D Integration Concepts

There are various kinds of advanced system integration approaches. These includes:

- Package-on-package (PoP) Package-in-Package (PiP),
- Die stacking on PCB (wirebond and flip chip),
- Stacking of flexible functional layers with embedded devices,
- Advanced Printed Circuit Board (PCB) stacking w/ or w/o embedded electronic devices,
- Wafer level system integration based on Through-Silicon-Vias (TSV).

3 Board Integration Techniques

3.1 International Status of Board Integration

Worldwide different approaches for single and multichip integration into a Printed Circuit Board are being investigated. Figure 5 provides a general overview of the technological approaches.

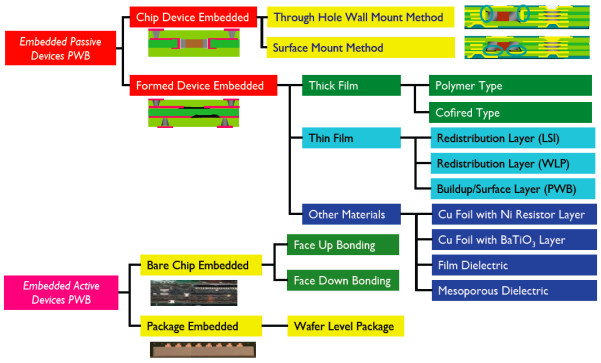


Figure 5 technological integration approaches for embedded devices [9]

Especially Japanese and Korean PCP manufacturer are already in high volume production of embedded devices or are just about to finish the R&D process. This is true for companies such as Clover Electronics, CMK, Ibiden, Kyocera SLC Technology, NEC Toppan Circuit Solutions, Oki Printed Circuit and Shinko Electro Industry and Samsung [11]. The main reason for the application of embedded devices is the reduction of module size which allows a size reduction of the board e. g. of portable electronic devices (watches, mobile phone, multi media devices) up to 30 %. Miniaturization is an important driving force for further developments of these new technologies. For device packaging discrete components – SMD (resistor, capacities) – are used as well as pre-packed wafer level packages or "Bare Dies" which can be integrated "face up" or "face down".

3.2 Chip in Polymer Technology

At Fraunhofer IZM an embedding concept was developed, which is based on the embedding of Si chips into the build-up layers of Printed Circuit Boards (PCB). The basic structure of this approach is shown in Figure 6. The interconnection to the chip bond pads, as well as to the pads on the PCB is realized by the formation of a microvia. This embedding technology focuses on the use of standard printed circuit board processes. [10]

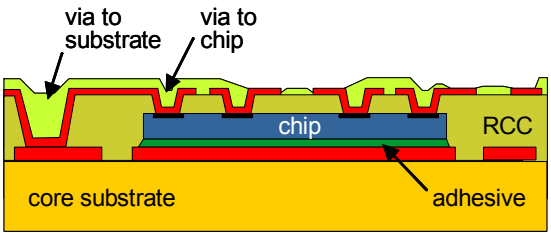


Figure 6 Basic structure of embedded chip in a PCB buildup

The I/O pads of the chip have to be conditioned to be compatible to a PCB metallization process. The Al-contact areas were supplied with Cu-bumps. Following this the chips are thinned down to 50 µm. In a next step the chips are bonded using an adhesive. A precise checking of the bond line thickness is absolutely necessary to maintain a consistent thickness of the trough hole dielectric. A RCC-layer with thin Cu is laminated afterwards. The process parameters have to be adjusted to avoid a damaging of the chip during lamination. The Interconnects to the chips are realized by laser microvias, followed by a PCB-compatible Cu layer. All process steps of this technology are aligned to a size of 18" x 24". Figure 7 shows a cross section of the interconnection to the embedded die. [11]

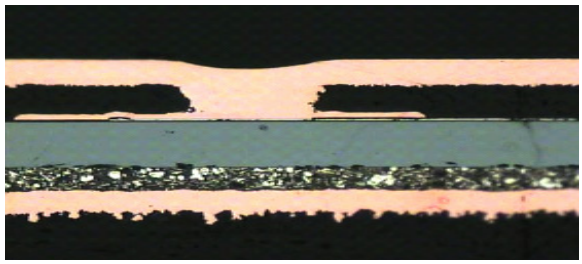


Figure 7 Cu-interconnection to embedded die

This method also allows a multi chip integration into the PCB. Figure 8 shows the schematic cross section of a 4-chip integration and Figure 9 the cross section of the real device structure.

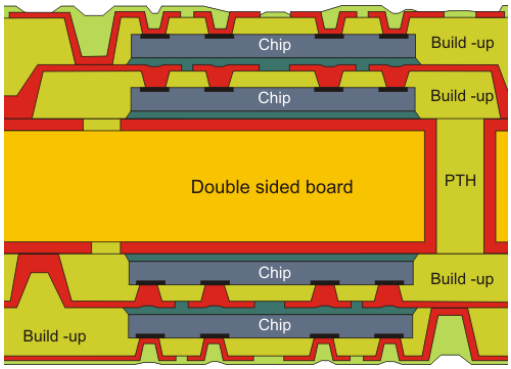


Figure 8 schematic of a 4-die embedded system in a PCB

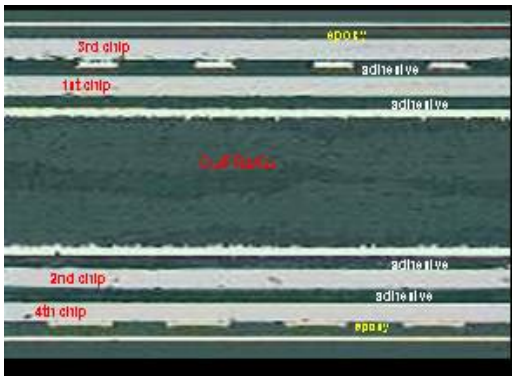


Figure 9 Cross section of the 4-die embedded system

4 Advanced Wafer Level System Integration

Wafer level packaging technologies, e.g. CSP, are already used in a high volume production. Currently, different technologies at wafer level are in development to satisfy the need to increase performance and functionality while reducing size, power and cost of the system.

Some major tasks for prospective wafer level packaging developments are:

- Integrated passive devices in RDL,
- WL assembly - die to wafer, wafer to wafer
- 3D stacking using Through-Silicon-Via (TSV),
- Embedding of active devices into the RDL,
- Active and passive interposers with TSV and embedded devices,
- Functional layer integration (actors, sensors, antennas),
- Integrated shielding (RF and power),
- Cooling
- Integration of energy storage and converter,
- Optical chip to chip interconnects.

4.1 Embedded Wafer Level Packaging

Embedded wafer level package technologies are now emerging also on wafer level processes. An innovative approach where chips are embedded in a mold compound has been developed recently. [12] [13] For this new approach the chips are reconstituted and embedded in epoxy compound to build an artificial wafer (eWLP). A thin film redistribution layer is applied instead of a laminate substrate which is typical for classical BGAs. Laminate substrates reach their limits in respect to integration density at reasonable cost. Thus, the application of thin film technology as redistribution layer opens new opportunities especially for SiP. The possibility to integrate components like inductors, capacitors, to apply transmission lines for high frequency or active devices into thin film layers opens additional design possibilities for new SiP applications. Figure 10 shows Infineons eWLB approach where chips are embedded into a mold compound. The approach can be extended for SiP solutions e. g. integrating chips side-by-side or integration passives into the thin film.

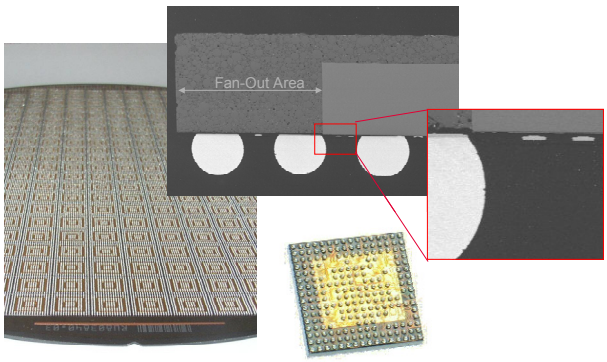


Figure 10 Embedded WLB (eWLP); Courtesy Infineon

4.2 Thin Chip Integration

Within the Fraunhofers "Wafer Level Thin Chip Integration (TCI) approach" thinned dies (thickness < 20 µm) are embedded and interconnected in a polymer dielectric layer with a multilayer thin film wiring or redistribution layer (RDL) on wafer level. A silicon interposer with or w/o trough silicon vias (TSV) can be used as a carrier. The thin chips are embedded face-up into the polymer layer. There is as well the potential for additional face-down mounted devices on top of the carrier. (Figure 12)
One of the key advantages of this approach is the integration of passive components (resistors, capacitors, inductors, etc.) close to the active dice which results in minimal parasitics. [14] Figure 11 shows an example of a filter using a metal (Cu) polymer-metal (Cu) RDL process.

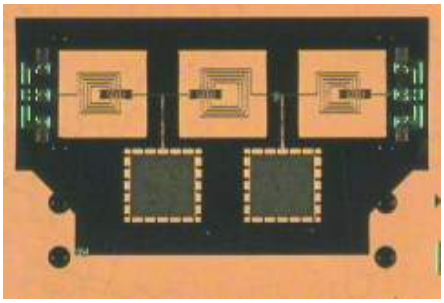


Figure 11 Low pass filter (2.4 GHz) realized in thin film technology [14]

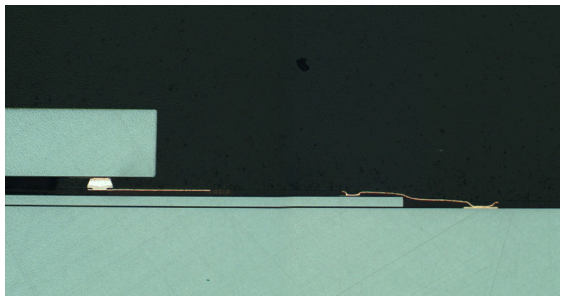


Figure 12 TCI-embedded die into RDL and interconnected by a thin film layer and a flip chip interconnect (source: European project "e Cube" [8])

Stacking of such functional TSV interposers (Figure 13) allows the realization of modularized systems e.g. complex- ultra-miniaturized sensor nodes, e.g."e Grains", with testable sub-module layers for signal detection, data processing and transmission and power conversion at a high miniaturization degree.

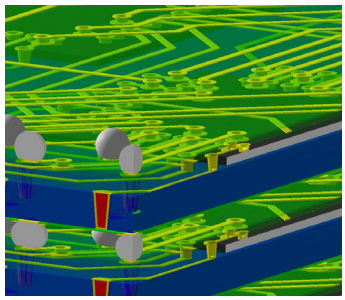


Figure 13 Schematic of a stackable silicon interposer with TSC and embedded active device

4.3 Through Silicon Via Integration Concepts

3D integration wafer level concepts such as VSI® [15] are characterized by high density vertical inter-chip wiring of stacked thinned silicon device substrates with freely positioned Through-Silicon-Vias (TSV) using standard silicon wafer processes. The VSI-TSV [16] approach can provide the shortest and most plentiful z-axis connections. The TSV technology is known to have various potential benefits such as:

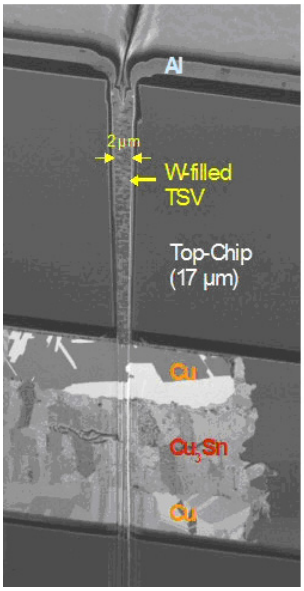
a) connection lengths can be as short as the thickness of a chip, which has the potential to significantly reduce the average wire length and shorten the electrical signal delay,
b) high-density, high-aspect-ratio interchip connections

Key process technologies are enabling 3D architectures with TSV interconnects included:

- high aspect ratio via formation with,
- isolation, barrier, and seed layer deposition,
- via metal filling,
- wafer thinning and thin wafer handling,
- temporary bond/de-bonding,
- frontside/backside multi redistribution layers (RDL),
- wafer/chip alignment, adjusted bonding (D2W, W2W).

Most of those 3D technologies are quite new to packaging industry and require a suited FE/ BE infrastructure as well as a total process integration. Many of the key technical issues and challenges for TSV interconnects are not fully resolved yet. Thus 3D wafer level approaches are today still at R&D stage but currently they are a lot of activities worldwide focusing on this as a potential solution with a high priority.

Figure 14 shows a cross section of a 3D integrated test structure after soldering. The tungsten filled ICVs are interconnected by Al wiring to the metallization of the top device and CuSn metal system to the metallization of the bottom device. The void-less metallization of the high-ratio aspect ICVs (diameter 2- 5 µm) is realized either by CVD of tungsten or copper. Though Silicon Vias with larger diameters (>5 µm to 40 µm) are filled using electrodeposition of copper with an appropriate seed layer deposition process such as CVD or PVD [17]. This allows the processing of metallized TSV in silicon substrate with a thickness of around 100 µm thickness (Figure 15).



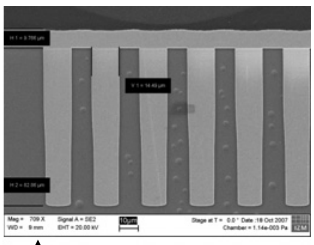


Figure 15 Cu filled TSV (15 µm diameter, 90 µm depth by electroplating [18]

Figure 14 Cross-section of interconnected devices with tungsten filled TSV using SLID [18]

Beside the SLID approach [18] [19] for the interconnection also solder micro bumps are used (e.g. SnAg) for the bonding of stacked devices to deal especially with surface incoplanarity of the devices to be stacked. Figure 14 shows an image sensor in a 3D stack configuration with a TSV silicon interposer. [20]

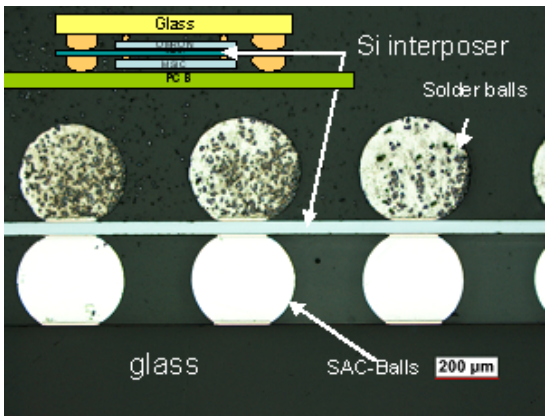


Figure 14 Cross section of a 3D stack with a TSV silicon interposer [20]

5 Conclusion

Besides the progress in silicon technology following Moore´s law there is an increasing demand for highly miniaturized complex system architectures which are based on 3D SiPs. Currently different approaches on board and level are in development, which are also combined in the new 3D SiP generation. The new 3D SiP solutions are driven by a wide range of applications e.g. medical, telecommunication, automation, ambient intelligence and environmental.

Future advanced 3D solutions will result in complex wafer level stacking approaches which can be later integrated in silicon interposers or other carrier substrates.

Figure 15 shows the Fraunhofer roadmap for wafer level 3D system integration.

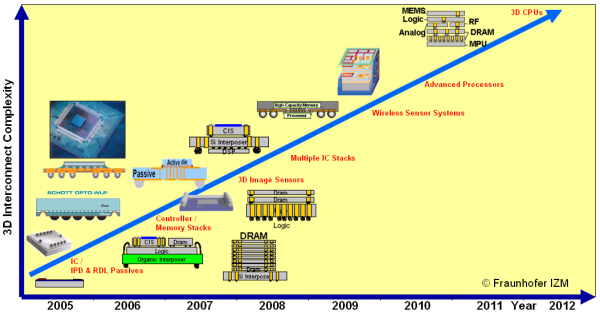


Figure 15 Roadmap of Wafer Level System Integration (Fraunhofer IZM)

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