STANDARD
MICROSYSTEMS
CORPORATION

LAN91C96I
PRELIMINARY

ISA Single-Chip Full Duplex Ethernet Controller with Magic Packet™

FEATURES

- ISA Single-Chip Ethernet Controller
- Fully Supports Full Duplex Switched Ethernet
- Supports Enhanced Transmit Queue Management
- 6K Bytes of On-Chip RAM
- Supports IEEE 802.3 (ANSI 8802-3) Ethernet Standards
- Automatic Detection of TX/RX Polarity Reversal
- Enhanced Power Management Features
- Supports "Magic Packet™" Power Management Technology
- Simultasking™ Early Transmit and Early Receive Functions
- Enhanced Early Transmit Function
- Receive Counter for Enhanced Early Receive
- Hardware Memory Management Unit
- Optional Configuration via Serial EEPROM Interface (Jumperless)
- Single 3.3V supply
- Industrial temperature range of –40°C to 85°C
- Supports Mixed Voltage External PHY Designs[1]
- Low Power CMOS Design
- 100 Pin QFP and TQFP (1.0mm body Thickness) Packages
- Pin Compatible with the LAN91C92 and LAN91C94 Bus Interface
- Direct Interface to ISA, with No Wait States
- Flexible Bus Interface
- 16 Bit Data and Control Paths
- Fast Access Time (40ns)
- Pipelined Data Path
- Handles Block Word Transfers for any Alignment
- High Performance Chained ("Back-to-Back") Transmit and Receive
- Pin Compatible with the LAN91C92 and the LAN91C94 in ISA Mode
- Dynamic Memory Allocation Between Transmit and Receive
- Flat Memory Structure for Low CPU Overhead
- Buffered Architecture, Insensitive to Bus Latencies (No Overruns/Underruns)
- Supports Boot PROM for Diskless ISA Applications

Network Interface

- Integrated 10BASE-T Transceiver Functions:
  - Driver and Receiver
  - Link Integrity Test
  - Receive Polarity Detection and Correction
- Integrated AUI Interface
- 10 Mb/s Manchester Encoding/Decoding and Clock Recovery
- Automatic Retransmission, Bad Packet Rejection, and Transmit Padding
- External and Internal Loopback Modes
- Four Direct Driven LEDs for Status/ Diagnostics

Software Drivers

- LAN9000 Drivers for Major Network Operating Systems Utilizing ISA Interface
- Software Drivers Compatible with the
- LAN91C92, LAN91C94, LAN91C100FD (100 Mb/s), and LAN91C110 (100 Mb/s) Controllers in ISA Mode
- Software Drivers Utilize Full Capability of 32 Bit Microprocessor

ORDERING INFORMATION

Order Numbers: LAN91C96IQFP, LAN91C96ITQFP
100 Pin QFP/TQFP Package Options

[1] Refer to DESCRIPTION OF PIN FUNCTIONS on Page 10 for 5V tolerant pins

GENERAL DESCRIPTION

The LAN91C96I is a VLSI Ethernet Controller that combines ISA, bus interfaces in one chip. LAN91C96I integrates all MAC and physical layer functions, as well as the packet RAM, needed to implement a high performance 10BASE-T (twisted pair) node. For 10BASE5 (thick coax), 10BASE2 (thin coax), and 10BASE-F (fiber) implementations, the LAN91C96I interfaces to external transceivers via the provided AUI port. Only one additional IC is required for most applications. The LAN91C96I comes with Full Duplex Switched Ethernet (FDSWE) support allowing the controller to provide much higher throughput. 6K bytes of RAM is provided to support enhanced throughput and compensate for any increased system service latencies. The controller implements multiple advanced powerdown modes including Magic Packet to conserve power and operate more efficiently. The LAN91C96I can directly interface with the ISA, buses and deliver no-wait-state operation. For ISA interfaces, the LAN91C96I occupies 16 I/0 locations and no memory space.

The same I/O space is used for ISA operations. Its shared memory is sequentially accessed with 40ns access times to any of its registers, including its packet memory. DMA services are not used by the LAN91C96I, virtually decoupling network traffic from local or system bus utilization. For packet memory management, the LAN91C96I integrates a unique hardware Memory Management Unit (MMU) with enhanced performance and decreased software overhead when compared to ring buffer and linked list architectures. The LAN91C96I is portable to different CPU and bus platforms due to its flexible bus interface, flat memory structure (no pointers), and its loosely coupled buffered architecture (not sensitive to latency).

The LAN91C96I is available in 100-pin QFP and TQFP (1.0 mm body thickness) packages. The low profile TQFP is ideal for mobile applications such as PC Card LAN adapters. The LAN91C96I operates with a single power supply voltage of 3.3V. The industrial temperature range for LAN91C96I is –40°C to 85°C.

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Magic Packet™ is a trademark of Advanced Micro Devices.

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OVERVIEW

A unique architecture allows the LAN91C96I to combine high performance, flexibility, high integration and simple software interface.

The LAN91C96I incorporates the LAN91C92 functionality for ISA environments. The LAN91C96I consists of the same logical I/O register structure in ISA modes. The MMU (Memory Management Unit) architecture used by the LAN91C96I combines the simplicity and low overhead of fixed areas with the flexibility of linked lists providing improved performance over other methods.

Packet reception and transmission are determined by memory availability. All other resources are always available if memory is available. To complement this flexible architecture, bus interface functions are incorporated in the LAN91C96I, as well as a 6144 byte packet RAM - and serial EEPROM-based setup. The user can select or modify configuration choices. The LAN91C96I integrates most of the 802.3 functionality, incorporating the MAC layer protocol, the physical layer encoding and decoding functions with the ability to handle the AUI interface. For twisted pair networks, LAN91C96I integrates the twisted pair transceiver as well as the link integrity test functions.

The LAN91C96I is a true 10BASE-T single chip device able to interface to a system or a local bus.

Support for direct-driven LEDs for installation and run-time diagnostics is provided. 802.3 statistics are gathered to facilitate network management.

The LAN91C96I is a single chip Ethernet controller designed to be 100% pin and software compatible with the LAN91C92 and LAN91C94 in ISA mode.

The LAN91C96I has been designed to support full duplex switched Ethernet and provides Fully independent transmit and receive operations.

The LAN91C96I internal packet memory is extended to 6k bytes, and the MMU will continue to manage memory in 256 byte pages. The increase in memory size accommodates the potential for simultaneous transmit and receive traffic in some full duplex applications as well as support for enhanced performance on systems that introduce increased latency.

The LAN91C96I has the ability to retrieve configuration information from a serial EEPROM on reset or power-up. In ISA mode, the serial EPROM acts as storage of configuration and IEEE Ethernet address information compatible with the existing LAN91C90, LAN91C92, and LAN91C94 ISA Ethernet controllers. External Flash ROM is required for CIS storage.

The LAN91C96I offers:

High integration:

Single chip controller including:

- Packet RAM
- ISA bus interface
- EEPROM interface
- Encoder/decoder with AUI interface
- 10BASE-T transceiver

High performance:

Chained ("Back-to-back") packet handling with no CPU intervention:

- Queues transmit packets
- Queues receive packets
- Stores results in memory along with packet
- Queues interrupts
- Optional single interrupt upon completion of transmit chain

Fast block move operation for load/unload:

- CPU sees packet bytes as if stored continuously.
- Handles 16 bit transfers regardless of address alignment.
- Access to packet through fixed window.

Fast bus interface:

Compatible with ISA type and faster buses.

Flexibility:

Flexible packet and header processing:

- Can be set to Simultasking - Early Receive and Transmit modes. With enhanced Early Receive functions.
- Can access any byte in the packet.
- Can immediately remove undesired packets from queue.
- Can move packets from receive to transmit queue.
- Can alter receive processing order without copying data.
- Can discard or enqueue again a failed transmission.

Resource allocation:

- Memory dynamically allocated for transmit and receive.
- Can automatically release memory on successful transmission.

Configuration:

ISA:

Uses non-volatile jumperless setup via serial EEPROM.
nROMon LAN91C96I, is left open with a pullup for ISA mode. This pin is sampled at the end of RESET.

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PIN CONFIGURATION

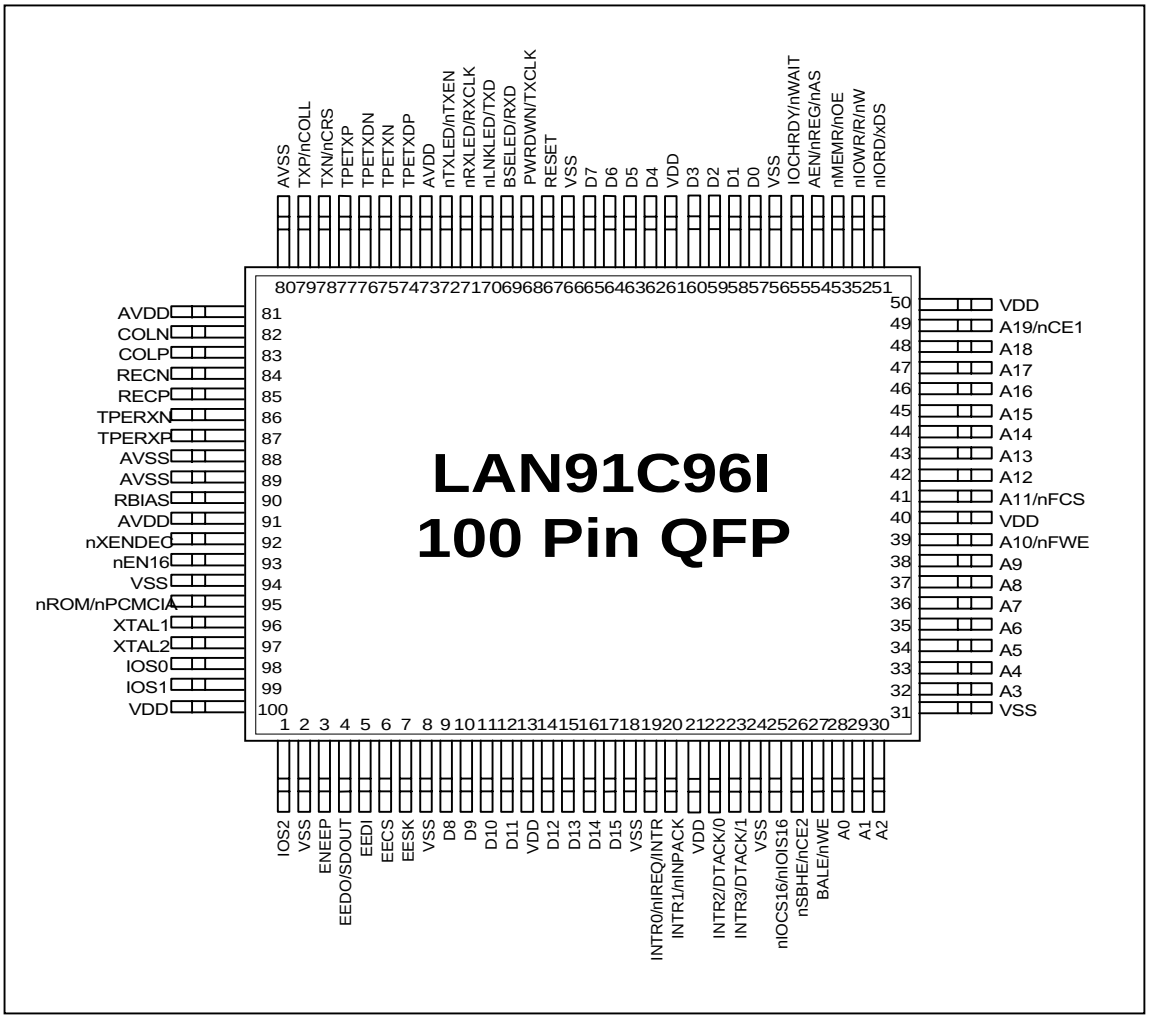


FIGURE 1 – PIN CONFIGURATION OF LAN91C96I QFP

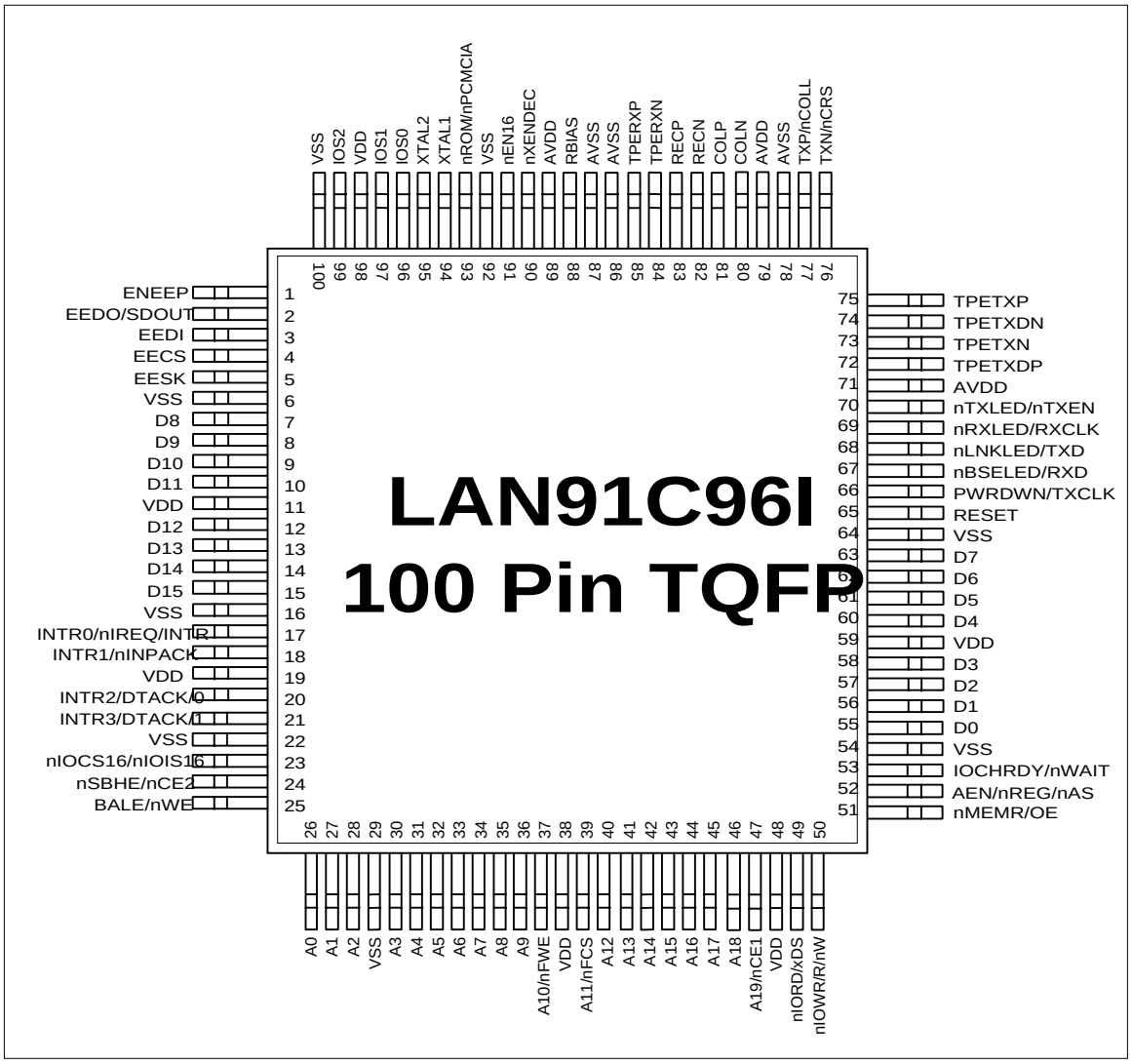


FIGURE 2 – PIN CONFIGURATION OF LAN91C96I TQFP

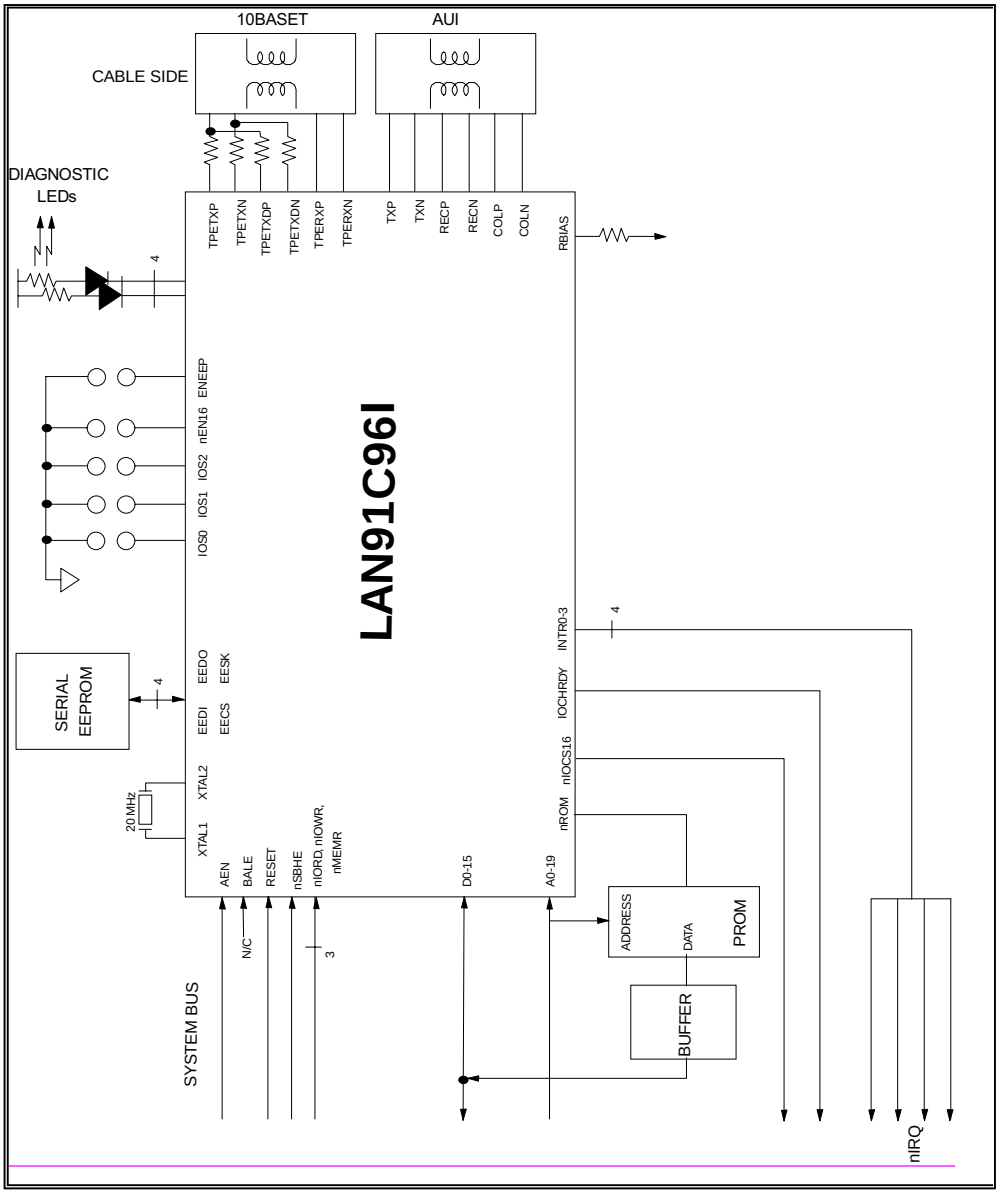


FIGURE 3 - SYSTEM DIAGRAM FOR ISA BUS WITH BOOT PROM

ISA VS. PIN REQUIREMENTS

FUNCTION	ISA	MAX NUMBER OF PINS
SYSTEM ADDRESS BUS	A0 A1-9 A10 A11 A12-14 A15 A16-18 A19 AEN	21
SYSTEM DATA BUS	D0-15	16
SYSTEM CONTROL BUS	RESET BALE nIORD nIOWR nMEMR IOCHRDY nIOCS16 nSBHE INTR0 INTR1 INTR2 INTR3	12
SERIAL EEPROM	EEDI EEDO EECS EESK ENEEP IOS0 IOS1 IOS2	8
CRYSTAL OSC.	XTAL1, XTAL2	2
POWER	VDD, AVDD	9
GROUND	GND, AGND	11
10BASE-T interface	TPERXP TPERXN TPETXP TPETXN TPETXDP TPETXDN	6
AUI interface	RECP RECN COLP COLN TXP/nCOLL TXN/nCRS	6
LEDs	nLNKLED/TXD nRXLED/RXCLK nBSELED/RXD nTXLED/nTXEN	4
MISC.	RBIAS PWRDWN/TX CLK nXENDEC nEN16 nROM	5

DESCRIPTION OF PIN FUNCTIONS

PIN NO.		PIN NAME	TYPE	DESCRIPTION
TQFP	QFP			
93	95	nROM	I/O4 with pullup	This pin is sampled at the end of RESET. For ISA operation this pin is left open and it is used as a ROM chip select output that goes active when nMEMR is low and the address bus contains a valid ROM address. In ISA mode the LAN91C96I is pin compatible with the LAN91C92 and LAN91C94
26-28 30-36	28,29, 30, 32-38	A0-9	I **	Input address lines 0 through 9.
37	39	A10/nFWE	I	ISA - Input address line 10.
39	41	A11/nFCS	I	ISA - Input address line 11.
40-46	42-48	A12-18	I **	Input address lines 12 through 18.
47	49	A19/nCE1	I with pullup	ISA - Input address line 19.
52	54	AEN/ nREG/ nAS	I with pullup **	ISA - Address enable input. Used as an address qualifier. Address decoding is only enabled when AEN is low.
24	26	nSBHE/ nCE2	I with pullup **	ISA - Byte High Enable input. Asserted (low) by the system to indicate a data transfer on the upper data byte.
53	55	IOCHRDY/ nWAIT	OD24 with pullup	ISA - Output. Optionally used by the LAN91C96I to extend host cycles.
55-58 60-63 7-10 12-15	57-60, 62-65, 9-12, 14-17	D0-15	I/O24	Bi-directional. 16 bit data bus used to access the LAN91C96I internal registers. The data bus has weak internal pullups. Supports direct connection to the system bus without external buffering.
65	67	RESET	IS with pullup **	Input. Active high Reset. This input is not considered active unless it is active for at least 100ns to filter narrow glitches.
25	27	BALE/nWE	IS with pullup **	ISA - Input. Address strobe. For systems that require address latching, the falling edge of BALE latches address lines and nSBHE.
17	19	INTR0/ nIREQ/ INTR	O24	ISA - Active high interrupt signal. The interrupt line selection is determined by the value of INT SEL1-0 bits in the Configuration Register. This interrupt is tri-stated when not selected.
18	20	INTR1/ nINPACK	O24	ISA - Output. Active high interrupt signal. The interrupt line selection is determined by the value of INT SEL1-0 bits in the Configuration Register. This interrupt is tri-stated when not selected.
20	22	INTR2	O24	ISA - Outputs. Active high interrupt signals. The interrupt line selection is determined by the value of INT SEL1-0 bits in the Configuration Register. These interrupts are tri-stated when not selected.
21	23	INTR3	O24	ISA - Outputs. Active high interrupt signals. The interrupt line selection is determined by the value of INT SEL1-0 bits in the Configuration Register. These interrupts are tri-stated when not selected.
23	25	nIOCS16/ nIOIS16	OD24	ISA - Active low output asserted in 16 bit mode when AEN is low and A4-A15 decode to the LAN91C96I address programmed into the high byte of the Base Address Register.
49	51	nIORD/ xDS	IS with pullup **	ISA, - Input. Active low read strobe used to access the LAN91C96I IO space.
50	52	nIOWR/ R/nW	IS with pullup **	ISA- Input. Active low write strobe used to access the LAN91C96I IO space.
51	53	nMEMR/ nOE	IS with pullup **	ISA - Active low signal used by the host processor to read from the external ROM.

PIN NO.		PIN NAME	TYPE	DESCRIPTION
TQFP	QFP			
5	7	EESK	O4	Output. 4usec clock used to shift data in and out of a serial EEPROM.
4	6	EECS	O4	Output. Serial EEPROM chip select.
2	4	EEDO/ SDOUT	O4	Output. Connected to the DI input of the serial EEPROM.
3	5	EEDI	I with pull-down **	Input. Connected to the DO output of the serial EEPROM.
96,97	98,99	IOS0-1	I with pullup	Input. External switches can be connected to these lines to select between predefined EEPROM configurations. The values of these pins are readable.
99	1	IOS2	I with pullup **	Input. External switches can be connected to these lines to select between predefined EEPROM configurations. The values of these pins are readable.
70	72	nTXLED/ nTXEN	OD16	INTERNAL ENDEC - Transmit LED output.
			O162	EXTERNAL ENDEC - Active low Transmit Enable output.
67	69	nBSELED/ RXD	OD16	INTERNAL ENDEC - Board Select LED activated by accesses to I/O space (nIORD or nIOWR active with AEN low and valid address decode for ISA). The pulse is stretched beyond the access duration to make the LED visible.
			I with pullup	EXTERNAL ENDEC - NRZ receive data input.
69	71	nRXLED/ RXCLK	OD16	INTERNAL ENDEC - Receive LED output.
			I with pullup	EXTERNAL ENDEC - Receive clock input.
68	70	nLNKLED/ TXD	OD16	INTERNAL ENDEC - Link LED output.
			O162	EXTERNAL ENDEC - Transmit Data output.
1	3	ENEEP	I with pullup **	Input. This active high input enables the EEPROM to be read or written by the LAN91C96I. Internally pulled up. Must be connected to ground if no serial EEPROM is used.
91	93	nEN16	I with pullup **	Input. When low the LAN91C96I is configured for 16 bit bus operation. If left open the LAN91C96I works in 8 bit bus mode. 16 bit configuration can also be programmed via serial EEPROM or software initialization of the CONFIGURATION REGISTER.
94	96	XTAL1	Iclk **	An external parallel resonance 20MHz crystal should be connected across these pins. If an external clock source is used, it should be connected to this pin (XTAL1) and XTAL2 should be left open.
95	97	XTAL2	Iclk	An external parallel resonance 20MHz crystal should be connected across these pins. If an external clock source is used, it should be connected to XTAL1 and this pin (XTAL2) should be left open.
83 82	85 84	RECP/ RECN	Diff. Input **	AUI receive differential inputs.
77 76	79 78	TXP/nCOL TXN/nCRS	Diff. Output	INTERNAL ENDEC - (nXENDEC pin open). In this mode TXP and TXN are the AUI transmit differential outputs. They must be externally pulled up using 150 ohm resistors.
			I **	EXTERNAL ENDEC - (nXENDEC pin tied low). In this mode the pins are inputs used for collision and carrier sense functions.
81 80	83 82	COLP COLN	Diff. Input **	AUI collision differential inputs. A collision is indicated by a 10MHz signal at this input pair.
85 84	87 86	TPERXP TPERXN	Diff. Input **	10BASE-T receive differential inputs.

PIN NO.		PIN NAME	TYPE	DESCRIPTION
TQFP	QFP			
75 73	77 75	TPETXP TPETXN	Diff. Output	INTERNAL ENDEC - 10BASE-T transmit differential outputs.
72 74	74 76	TPETXDP TPETXDN	Diff. Output	10BASE-T delayed transmit differential outputs. Used in combination with TPETXP and TPETXN to generate the 10BASE-T transmit pre-distortion.
66	68	PWRDWN/ TXCLK	I with pullup **	INTERNAL ENDEC - Powerdown input. It keeps the LAN91C96I in powerdown mode when high (open). Must be low for normal operation.
				EXTERNAL ENDEC - Transmit clock input from external ENDEC.
88	90	RBIAS	Analog Input	A 22kohm 1% resistor should be connected between this pin and analog ground.
90	92	nXENDEC	I with pullup **	When tied low the LAN91C96I is configured for EXTERNAL ENDEC. When tied high or left open the LAN91C96I will use its internal encoder/decoder.
11,19, 48,59, 98,38	13,21,40, 50, 61,100	VDD		3.3V power supply pins
71,79, 89	73,81, 91	AVDD		3.3V power supply pins
100,6, 22,29 54,64,92, 16	2,8,18, 24,31, 56,66, 94	GND		Ground pins.
78,86 87	80,88,89	AGND		Analog ground pins.

BUFFER SYMBOLS

O4	Output t buffer with 2mA source and 4mA sink.
I/O4	Output buffer with 2mA source and 4mA sink.
O162	Output buffer with 2mA source and 16mA sink.
O24	Output buffer with 12mA source and 24mA sink.
OD16	Open drain buffer with 16mA sink.
OD24	Open drain buffer with 24mA sink.
I/O24	Bi-directional buffer with 12mA source and 24mA sink.
I	Input buffer with TTL levels.
IS	Input buffer with Schmitt Trigger Hysteresis.
Iclk	Clock input buffer. Note: When the device is designed at Vcc=3.3v, the buffer symbols are not consistent with there associated drive current strengths. Please refer to the DC Electrical Section for additional details.

DC levels and conditions defined in the DC Electrical Characteristics section.

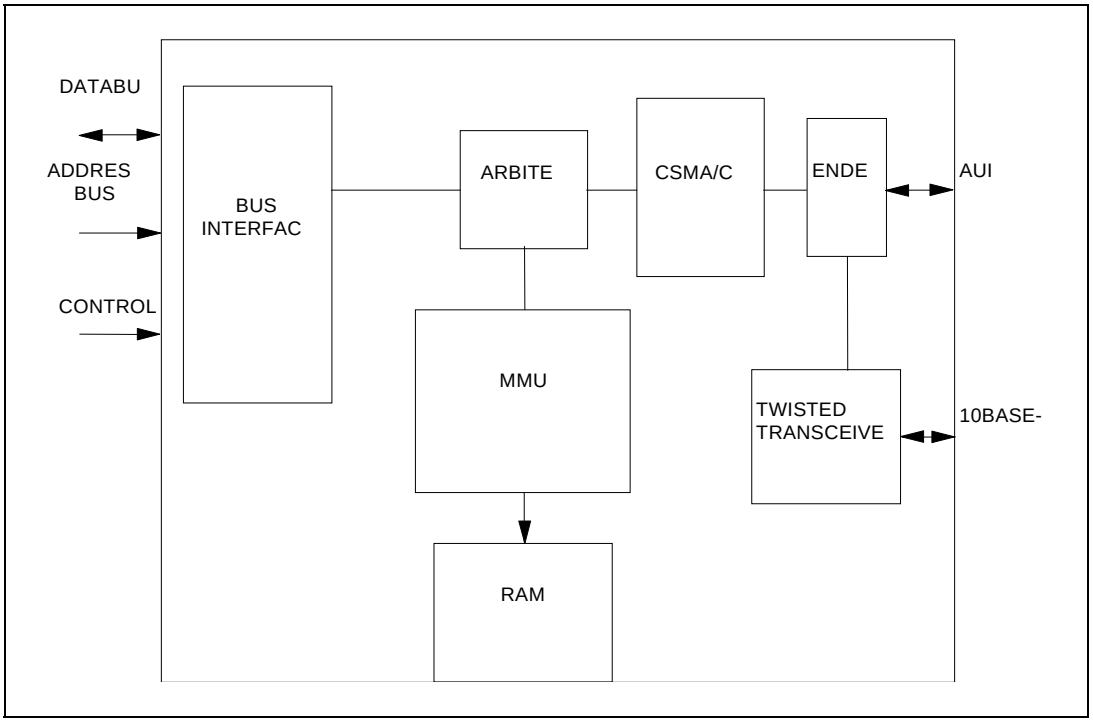


FIGURE 4 - LAN91C96I INTERNAL BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

The LAN91C96I includes an arbitrated-shared memory of 6144 bytes. Any portion of this memory can be used for receive or transmit packets.

The MMU unit allocates RAM memory to be used for transmit and receive packets, using 256 byte pages.

The arbitration is transparent to the CPU in every sense. There is no speed penalty for ISA type of machines due to arbitration. There are no restrictions on what locations can be accessed at any time. RAM accesses as well as MMU requests are arbitrated.

The RAM is accessed by mapping it into I/O space for sequential access. Except for the RAM accesses and the MMU request/release commands, I/O accesses are not arbitrated.

The I/O space is 16 bits wide. Provisions for 8 bit systems are handled by the bus interface.

In the system memory space, up to 64 kbytes are decoded by the LAN91C96I as expansion ROM. The ROM expansion area is 8 bits wide.

Device configuration is done using a serial EEPROM, with support for modifications to the EEPROM at installation time. The CSMA/CD core implements the 802.3 MAC layer protocol. It has two independent interfaces, the data path and the control path.

Both interfaces are 16 bits wide. The control path provides a set of registers used to configure and control the block. These registers are accessible by the CPU through the LAN91C96I I/O space. The data path is of sequential access nature and typically works in one direction at any given time. An internal DMA type of interface connects the data path to the device RAM through the arbiter and MMU.

The CSMA/CD data path interface is not accessible to the host CPU.

The internal DMA interface can arbitrate for RAM access and request memory from the MMU when necessary.

An encoder/decoder block interfaces the CSMA/CD block on the serial side. The encoder will do the Manchester encoding of the transmit data at 10 Mb/s, while the decoder will recover the receive clock, and decode received data.

Carrier and Collision detection signals are also handled by this block and relayed to the CSMA/CD block.

The encoder/decoder block can interface the network through the AUI interface pairs, or it can be programmed to use the internal 10BASE-T transceiver and connect to a twisted pair network.

The twisted pair interface takes care of the medium dependent signaling for 10BASE-T type of networks. It is responsible for line interface (with external pulse transformers and pre-distortion resistors), collision detection as well as the link integrity test function.

The LAN91C96I provides a 16-bit data path into RAM. The RAM is private and can only be accessed by the system via the arbiter. RAM memory is managed by the MMU. Byte and word accesses to the RAM are supported.

If the system to SRAM bandwidth is insufficient the LAN91C96I will automatically use its IOCHRDY line for flow control. However, for ISA buses, IOCHRDY will never be negated.

The LAN91C96I consists of an integrated Ethernet controller mapped entirely in I/O space.

The Ethernet controller function includes a built-in 6kbyte RAM for packet storage. This RAM buffer is accessed by the CPU through sequential access regions of 256 bytes each. The RAM access is internally arbitrated by the LAN91C96I, and dynamically allocated between transmit and receive packets. Each packet may consist of one or more 256 byte page. The Ethernet controller functionality is identical to the LAN91C94 and LAN91C95 except where indicated otherwise.

The LAN91C96I Memory Management Unit parameters are:

RAM size	6kbytes
Max. number of pages	24
Max. number of packets	24 (FIFOs have 24 entries of 5 bits)
Max. pages per packet	6
Page Size	256 bytes

BUFFER MEMORY

The logical addresses for RAM access are divided into TX area and RX area.

The TX area is seen by the CPU as a window through which packets can be loaded into memory before queuing them in the TX FIFO of packets. The TX area can also be used to examine the transmit completion status after packet transmission.

The RX area is associated to the output of the RX FIFO of packets, and is used to access receive packet data and status information.

The logical address is specified by loading the address pointer register. The pointer can automatically increment on accesses.

All accesses to the RAM are done via I/O space.

A bit in the address pointer also specifies if the address refers to the TX or RX area.

In the TX area, the host CPU has access to the next transmit packet being prepared for transmission. In the RX area, it has access to the first receive packet not processed by the CPU yet.

The FIFO of packets, existing beneath the TX and RX areas, is managed by the MMU. The MMU dynamically allocates and releases memory to be used by the transmit and receive functions.

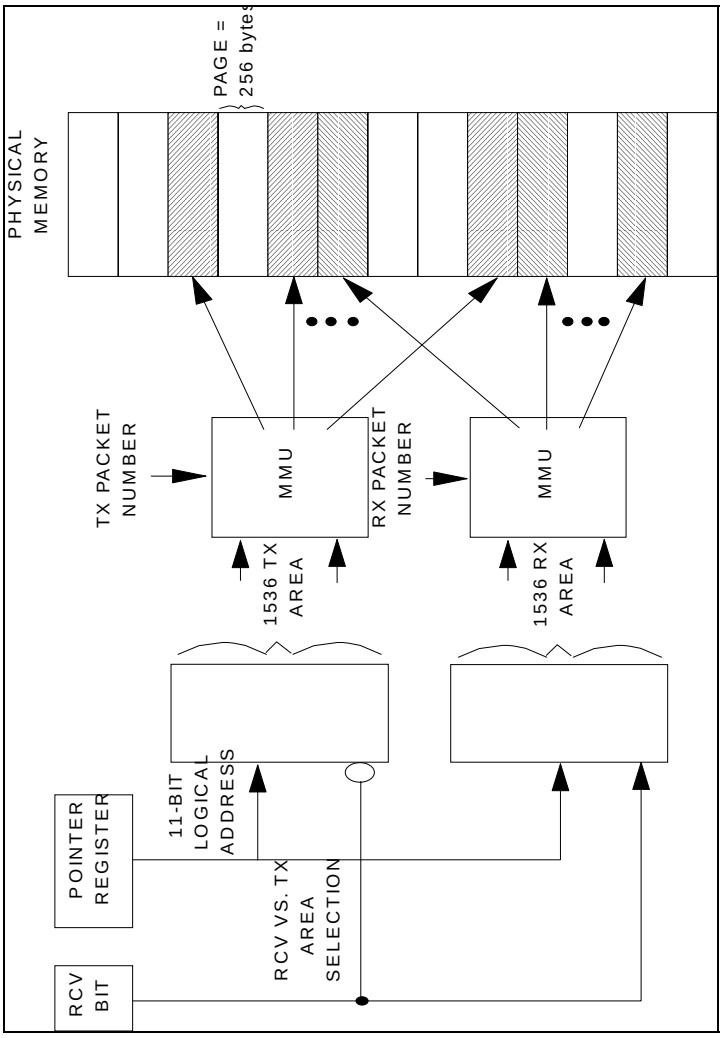


FIGURE 5 - MAPPING AND PAGING VS. RECEIVE AND TRANSMIT AREA

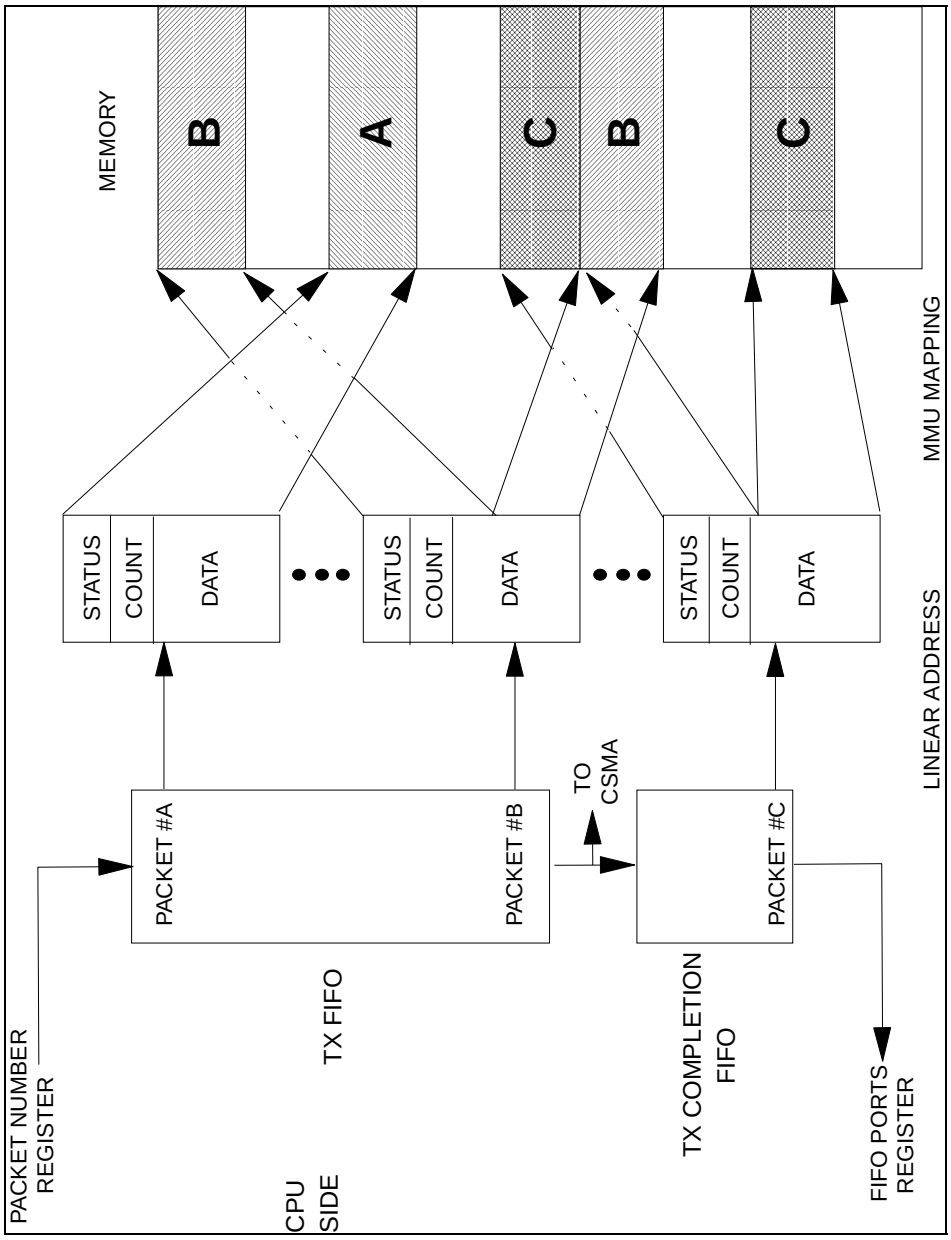


FIGURE 6 - TRANSMIT QUEUES AND MAPPING

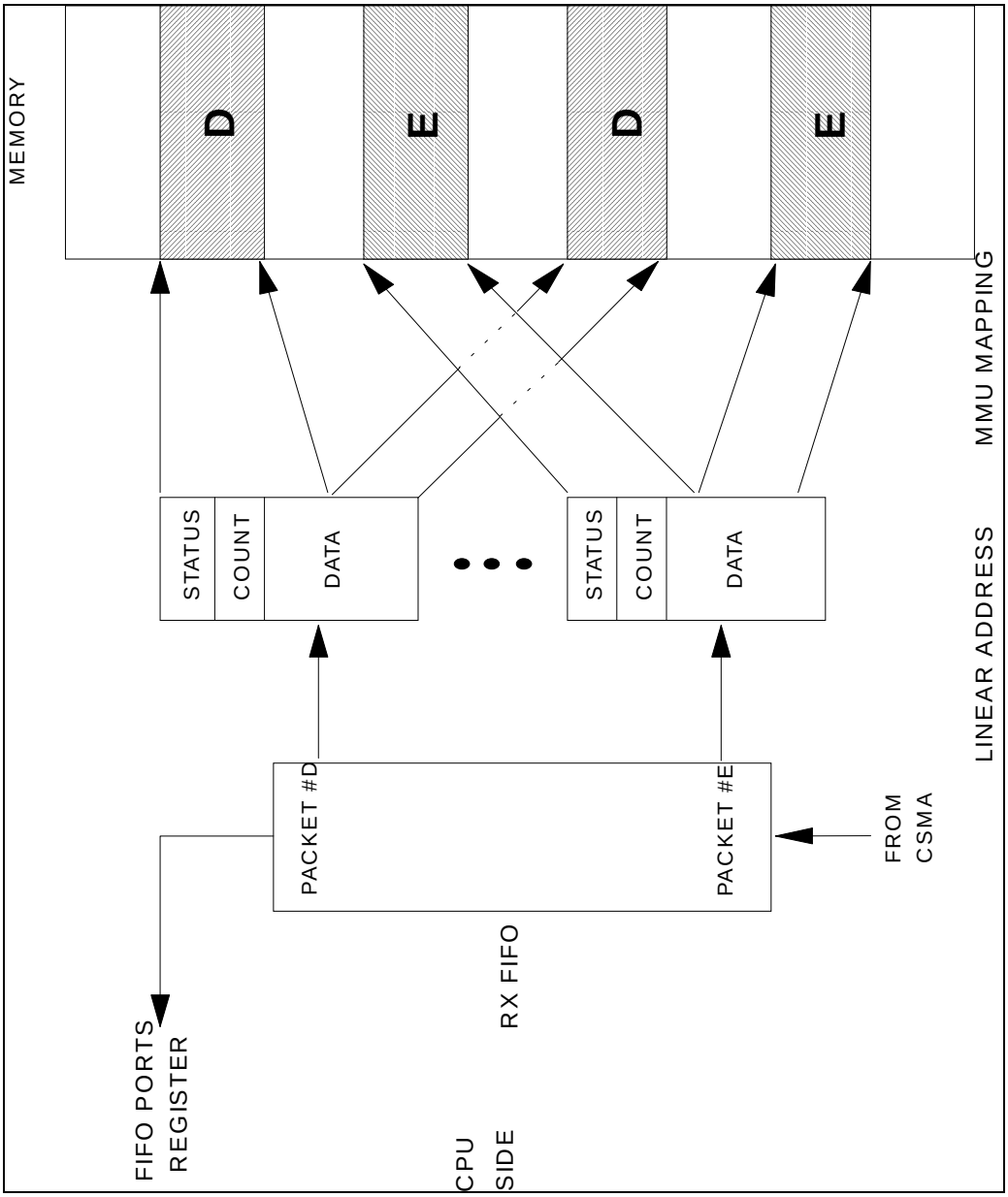


FIGURE 7 – RECEIVE QUEUES AND MAPPING

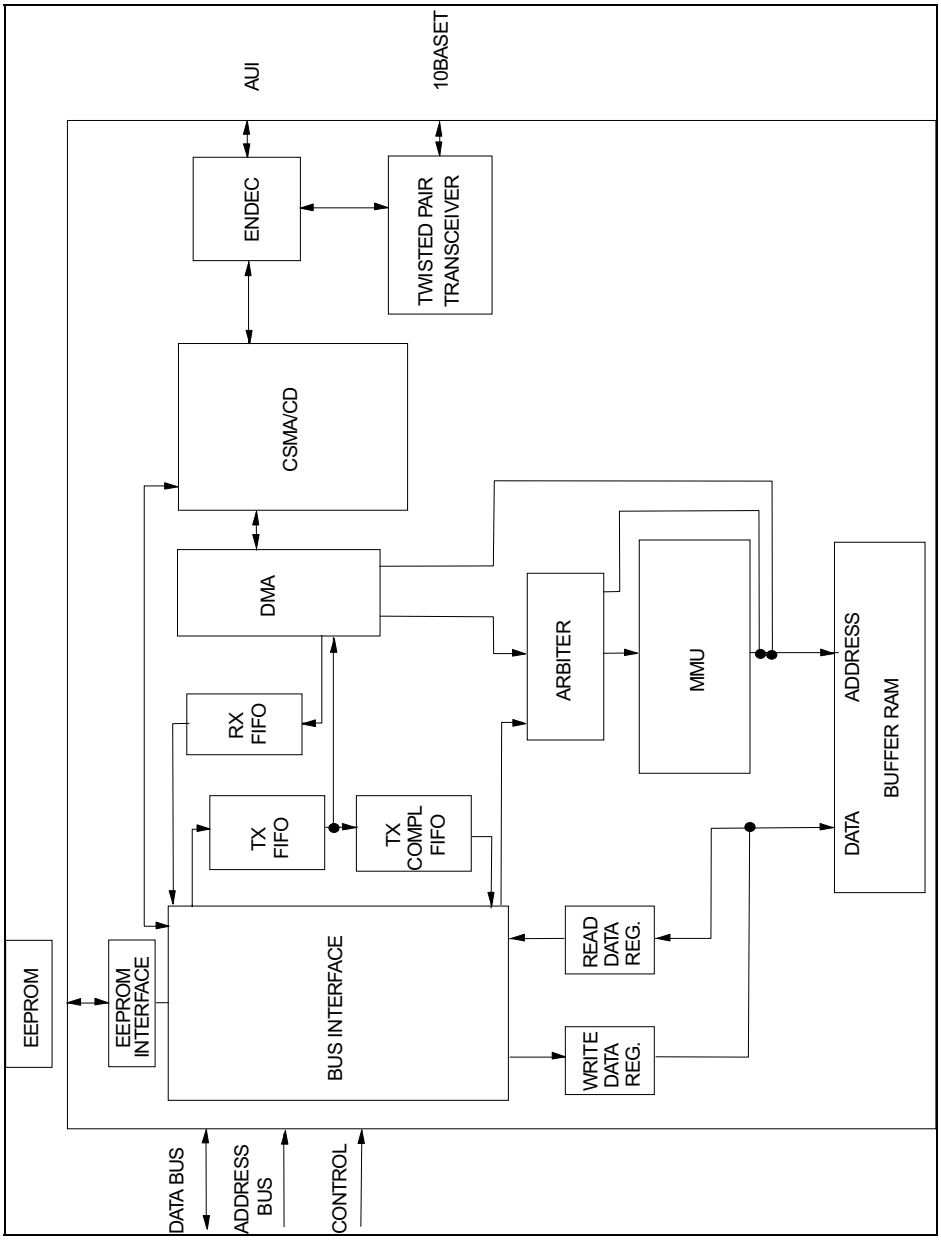


FIGURE 8 – LAN91C96I INTERNAL BLOCK DIAGRAM WITH DATA PATH

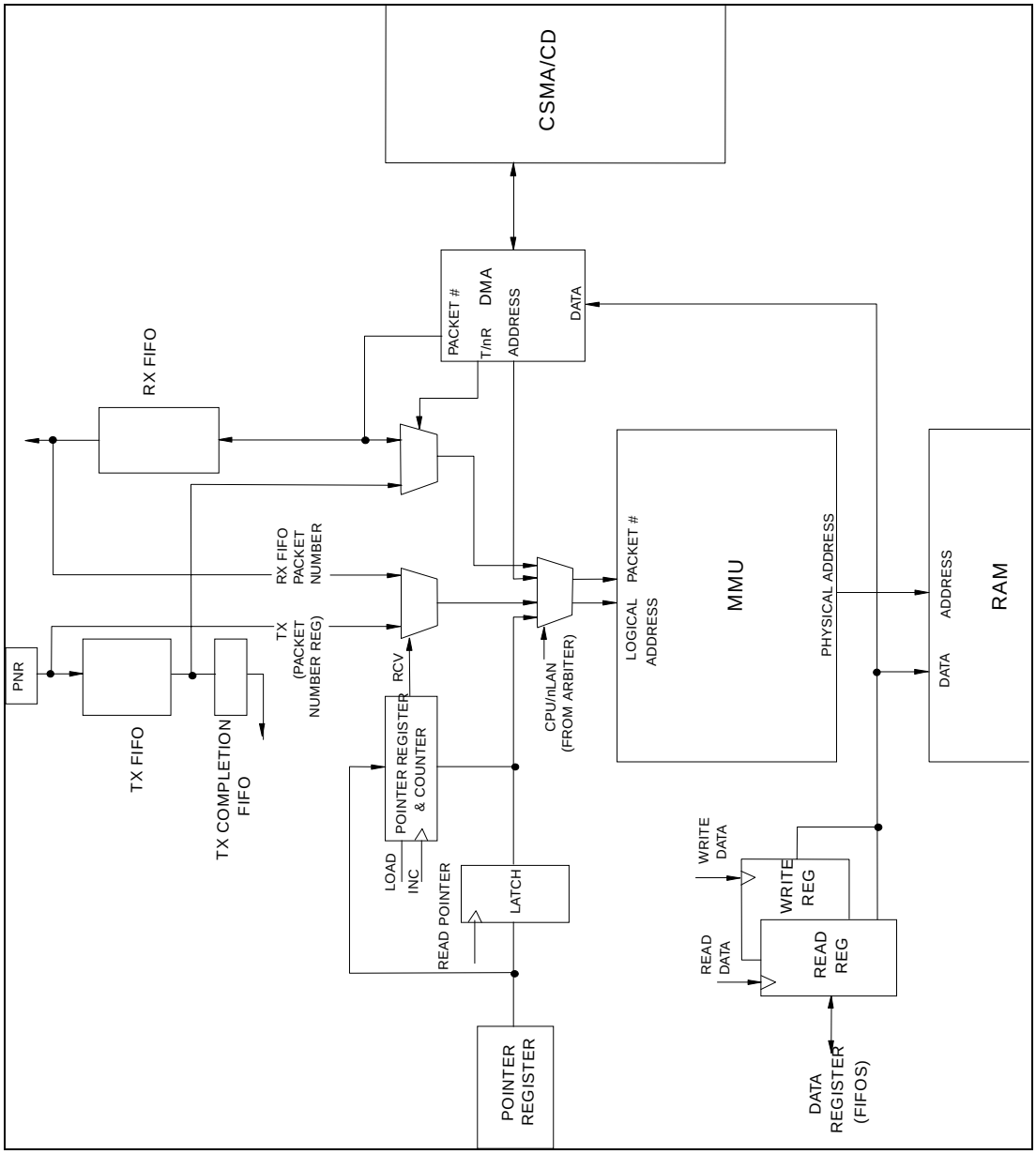


FIGURE 9 – LOGICAL ADDRESS GENERATION AND RELEVANT REGISTERS

Table 1 - LAN91C96I Address Space

	SIGNALS USED	ISA	ON-CHIP	DEPTH	WIDTH
Ethernet I/O space (1)	nIORD/ nIOWR	Y	Y	16 locations	8 or 16 bits

Table 2 - Bus Transactions In ISA Mode

	A0	nSBHE	D0-7	D8-15
8 BIT MODE ((nEN16=1) (16BIT=0))	0	X	Even byte	-
	1	X	Odd byte	-
16 BIT MODE otherwise	0	0	Even byte	Odd byte
	0	1	Even byte	-
	1	0	-	Odd byte
	1	1	Invalid cycle	

16BIT: CONFIGURATION REGISTER bit 7
IOis8: CSR register bit 5
nEN16: pin nEN16
8 Bit mode: ((IOis8 = 1) + (nMIS16 = 1)

INTERRUPT STRUCTURE

The Ethernet interrupt is conceptually equivalent to the LAN91C94 interrupt line, it is the or function of all enabled interrupts within the Ethernet core. The enabling, reporting, and clearing of these sources is controlled by the ECOR register. The interrupt structure is similar for ISA modes with the following exceptions:

Table 3 – Interrupt Merging

FUNCTION	ISA MODE
Interrupt Output	INTR0-3
Ethernet Interrupt Source	OR function of all interrupt bits specified in the Interrupt Status Register ANDed with their respective Enable bits
Ethernet Interrupt Enable	Not Applicable in ISA mode
Ethernet Interrupt Status Bit	Intr bit in ECSR

RESET LOGIC

The pins and bits involved in the different reset mechanisms are:

RESET - Input Pin
SRESET - Soft Reset bit in ECOR, or the SRESET bit
SOFT RST - EPH Soft Reset bit in RCR

Table 4 – Reset Logic

	RESETS THE FOLLOWING FUNCTIONS	SAMPLES ISA MODE	TRIGGERS EEPROM READ
RESET pin	All internal logic	Yes	Yes
ECOR Register SRESET bit	The Ethernet controller function except for the bit itself. Setting this bit also lowers the nIREQ/READY line. When cleared, the nIREQ/READY line is raised.	No	Yes
SOFT RST	The Ethernet controller itself except for the IA, CONF and BASE registers.	No	No

POWER DOWN LOGIC STATES

Tables 5A, 5B, 6A, and 6B describe the power down states of the LAN91C96I. The pins and bits involved in power down are:

1. PWRDWN/TXCLK - Input pin valid when XENDEC is not zero (0).
2. Pwrdwn bits in ECSR
3. Enable Function bit in ECOR
4. PWRDN - Legacy power down bit in Control Register.

LAN91C96I Power Down States

Table 5A - ISA Mode Defined States (Refer To Table 5B For Next States To Wake-Up Events)

CURRENT STATE							
No.	**PWRDWN PIN (A= Assrtd)**	**ECOR FUNCTION ENABLE**	**ECSR POWER DOWN**	**CTR PWRDWN BIT**	**CTR WAKEUP_EN BIT**	**POWERS DOWN**	**DOES NOT POWER DOWN**
1	A	X	X	X	X	Everything. Asserts the modem power down pin (nPWDN) also	
2	nA	X	0	0	0		Ethernet Tx, Rx, Link
3	nA	X	0	0	1	Ethernet Tx	Ethernet Rx, Link
4	nA	X	0	1	1	Ethernet Tx, Rx, Link	
5	nA	X	0	1	0	Ethernet Tx, Rx, Link	

Note 1: The chart assumes that ECOR Function Enable bit is meaningless in ISA mode.
Note 2: ECSR Power Down bit must not be set to one(1) in ISA mode.

Table 5B - ISA Mode

		NEXT STATE					
No.	**WAKES UP BY**	**PWR DWN PIN (A=Assrtd)**	**ECOR FUCNTION ENABLE**	**ECSR POWER DOWN**	**CTR PWR-DWN BIT**	**CTR WAKEUP_ EN BIT**	**COMMENTS**
..1	PWRDWN Pin deassertion	nA	No change	No change	No change	No change	ECOR Function Enable Bit value is meaningless in ISA mode
..2		nA	X	0	0	0	Fully Awake
..3	By writing a 0 to CTR WAKEUP_EN bit	nA	X	0	0	0	
..4	By writing a 0 to CTR WAKEUP_EN bit AND CTR PWRDWN bit = 0	nA	X	0	0	0	The CTR PWRDWN bit has precedence unlike the LAN91C95
..5	By writing 0 to CTR PWRDWN bit	nA	X	0	0	0	

Note 1: The chart assumes that ECOR Function Enable bit is meaningless in ISA mode.
Note 2: ECSR Power Down bit must not be set to one (1) in ISA mode.

ATTRIBUTE MEMORY

Address 0- 7FFEh

The Attribute Memory is implemented using an external parallel EEPROM, ROM or Flash ROM. A parallel EEPROM (or equivalent external device) must be used for CIS.

In ISA mode, serial EEPROM is used for configuration and IEEE Node address making it software compatible to the LAN9xxx family of Ethernet LAN Controllers. The EEPROM is optional forISArequiring a Minimum size of 64 X 16 bit word addresses.

The LAN91C96I generates the appropriate control lines (nFCS and nFWE) to read and write the Attribute memory, and it tri-states the data bus during external Attribute Memory accesses. Only even locations are used.

Attribute Memory map

The EPROM attribute memory decodes are shown below. Internal to the LAN91C96I, the memory addressing logic will allow byte or word access on even byte boundaries. LAN91C96I uses address A0-9, A15, along with nREG, nCE1, nWE and nOE.

With or Without 64x16 bit Serial EEPROM:

ATTRIBUTE MEMORY ADDRESS	EXTERNAL EPROM STORE	CONFIGURATION REGISTERS
0 - 7FFEh	X	
8000h - 8003h		X

PACKET FORMAT IN BUFFER MEMORY FOR ETHERNET

The packet format in memory is similar to that in the TRANSMIT and RECEIVE areas. The first word is reserved for the status word, the next word is used to specify the total number of bytes, and that in turn is followed by the data area. The data area holds the packet itself, and its length is determined by the byte count. The packet memory format is word oriented.

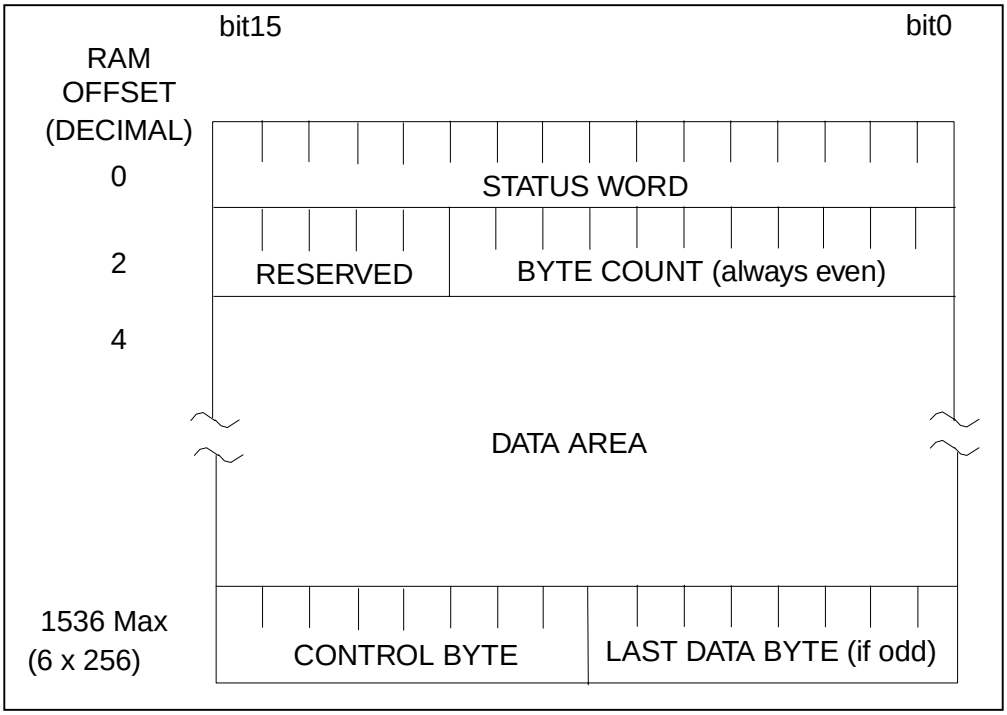


FIGURE 10 – DATA PACKET FORMAT

	TRANSMIT PACKET	RECEIVE PACKET
STATUS WORD	Written by CSMA upon transmit completion (see Status Register)	Written by CSMA upon receive completion (see RX Frame Status Word)
BYTE COUNT	Written by CPU	Written by CSMA
DATA AREA	Written/modified by CPU	Written by CSMA
CONTROL BYTE	Written by CPU to control ODD/EVEN data bytes	Written by CSMA. Also has ODD/EVEN bit

BYTE COUNT - Divided by two, it defines the total number of words, including the STATUS WORD, the BYTE COUNT WORD, the DATA AREA and the CONTROL BYTE. The receive byte count always appears as even, the ODDFRM bit of the receive status word indicates if the low byte of the last word is relevant. The transmit byte count least significant bit will be assumed 0 by the controller regardless of the value written in memory.

DATA AREA (in RAM)

The data area starts at offset 4 of the packet structure, and it can extend for up to 2043 bytes. The data area contains six bytes of DESTINATION ADDRESS followed by six bytes of SOURCE ADDRESS, followed by a variable length number of bytes.

On transmit, all bytes are provided by the CPU, including the source address. The LAN91C96I does not insert its own source address. On receive, all bytes are provided by the CSMA side.

The 802.3 Frame Length word (Frame Type in Ethernet) is not interpreted by the LAN91C96I. It is treated transparently as data for both transmit and receive operations.

CONTROL BYTE (in RAM)

The CONTROL BYTE always resides on the high byte of the last word. For transmit packets the CONTROL BYTE is written by the CPU as:

X	X	ODD	CRC	0	0	0	0

ODD - If set, indicates an odd number of bytes, with the last byte being right before the CONTROL BYTE. If clear, the number of data bytes is even and the byte before the CONTROL BYTE is not transmitted.

CRC - When set, CRC will be appended to the frame. This bit has only meaning if the NOCRC bit in the TCR is set.

For receive packets the CONTROL BYTE is written by the controller as:

0	1	ODD	0	0	0	0	0

ODD - If set, indicates an odd number of bytes, with the last byte being right before the CONTROL BYTE. If clear, the number of data bytes is even and the byte before the CONTROL BYTE should be ignored.

RECEIVE FRAME STATUS WORD (in RAM)

This word is written at the beginning of each receive frame in memory. It is not available as a register.

ALGN ERR	BROD CAST	BADCRC	ODDFRM	TOOLNG	TOO SHORT		

	HASH VALUE						MULT CAST
	5	4	3	2	1	0	

ALGNERR - Frame had alignment error.

BRODCAST - Receive frame was broadcast.

BADCRC - Frame had CRC error.

ODDFRM - This bit when set indicates that the received frame had an odd number of bytes.

TOOLNG - The received frame is longer than the 802.3 maximum size (1518 bytes on the cable).

TOOSHORT - The received frame is shorter than the 802.3 minimum size (64 bytes on the cable).

HASH VALUE - Provides the hash value used to index the Multicast Registers. Can be used by receive routines to speed up the group address search. The hash value consists of the six most significant bits of the CRC calculated on the Destination Address, and maps into the 64 bit multicast table. Bits 5,4,3 of the hash value select a byte of the multicast table, while bits 2,1,0 determine the bit within the byte selected.

Examples of the address mapping are shown in the table below:

ADDRESS	HASH VALUE 5-0	MULTICAST TABLE BIT
ED 00 00 00 00 00	000 000	MT-0 bit 0
0D 00 00 00 00 00	010 000	MT-2 bit 0
01 00 00 00 00 00	100 111	MT-4 bit 7
2F 00 00 00 00 00	111 111	MT-7 bit 7

MULTCAST - Receive frame was multicast. If hash value corresponds to a multicast table bit that is set, and the address was a multicast, the packet will pass address filtering regardless of other filtering criteria.

REGISTERS MAP IN I/O SPACE

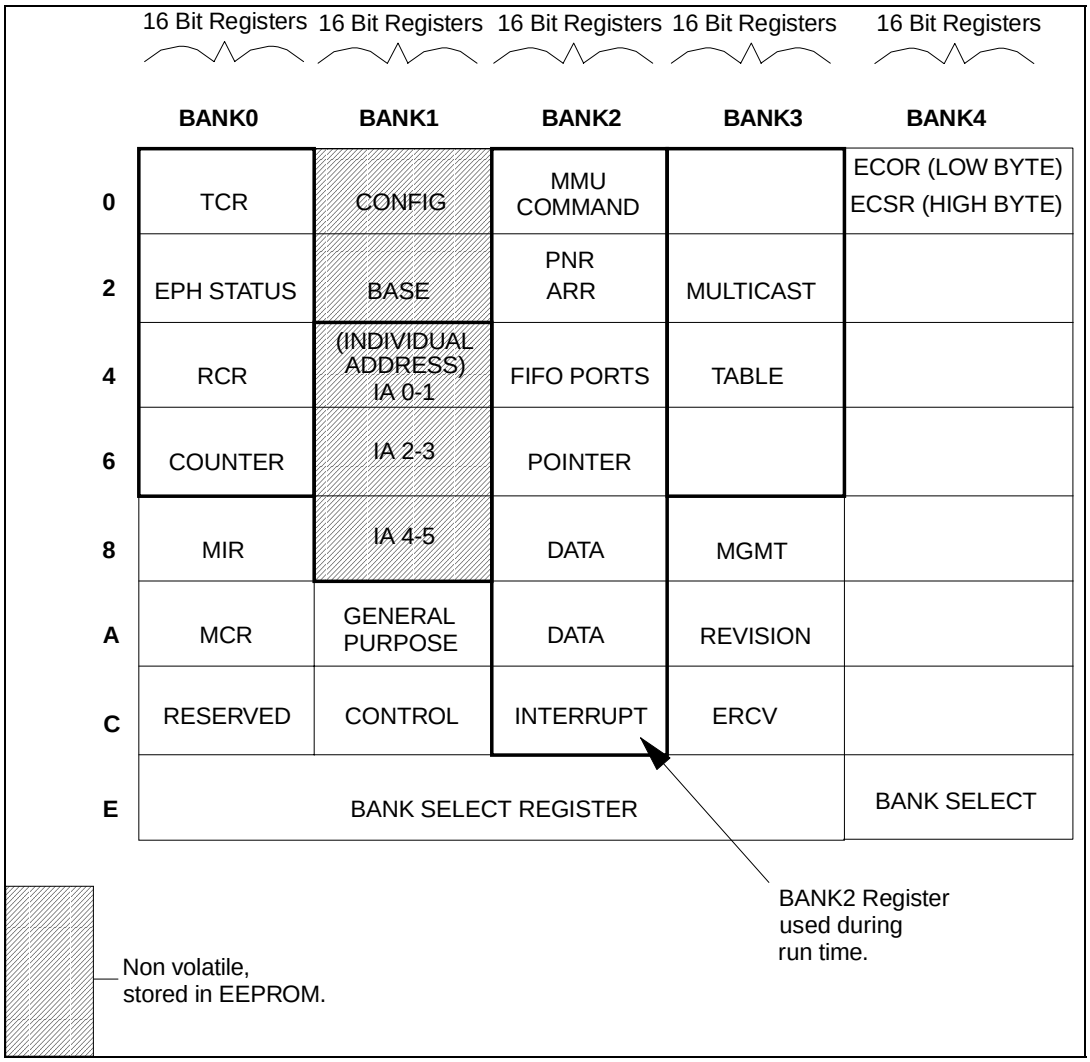


FIGURE 11 - LAN91C96I REGISTERS

I/O SPACE ACCESS

The address is determined by the Ethernet I/O Base Registers**.** The Ethernet I/O space can be configured as an 8 or 16 bit I/O space, and is similar to the LAN91C94, LAN91C92, etc. I/O space mapping. To limit the I/O space requirements to 16 locations, the registers are Split into 4 banks in ISA mode. The last word of the I/O area is shared by all banks and can be used to change the bank in use. Banks 0 through 3 functionally correspond to the LAN91C94 banks.

Registers are described using the following convention:

OFFSET	NAME	TYPE	SYMBOL
E	BANK SELECT REGISTER	READ/WRITE	BSR

BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT9	BIT8
RST Val	RST Val	RST Val	RST Val	RST Val	RST Val	RST Val	RST Val
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
RST Val	RST Val	RST Val	RST Val	RST Val	RST Val	RST Val	RST Val

OFFSET - Defines the address offset within the IOBASE where the register can be accessed at, provided the bank select has the appropriate value. The offset specifies the address of the even byte (bits 0-7) or the address of the complete word. The odd byte can be accessed using address (offset + 1).

Some registers (e.g. the Interrupt Ack. or the Interrupt Mask) are functionally described as two eight bit registers. In such case, the offset of each one is independently specified.

Regardless of the functional description, when the LAN91C96I is in 16 bit mode, all registers can be accessed as words or bytes.

RST Val - The default bit values upon hard reset are highlighted below each register.

BANK SELECT REGISTER

OFFSET	NAME	TYPE	SYMBOL
# in HEX	BANK SELECT REGISTER	READ/WRITE	BSR

0	0	1	1	0	0	1	1
0	0	1	1	0	0	1	1
					BS2	BS1	BS0
X	X	X	X	X	0	0	0

BS2, BS1, BS0 - Determine the bank presently in use.

This register is always accessible except in power down mode and is used to select the register bank in use.

The upper byte always reads as 33h and can be used to help determine the I/O location of the LAN91C96I.

The BANK SELECT REGISTER is always accessible regardless of the value of BS0-2.

Accesses to non-existing banks will ignore writes and reads will return 0x33 on byte reads.

BS2	BS1	BS0	BANK #
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	X	X	None

I/O SPACE - BANK0

OFFSET	NAME	TYPE	SYMBOL
0	TRANSMIT CONTROL REGISTER	READ/WRITE	TCR

This register holds bits programmed by the CPU to control some of the protocol transmit options.

FDSE	ETEN-TYPE	EPH LOOP	STP SQET	FDUPLX	MON_ CSN		NOCRC
0	0	0	0	0	0	X	0
PAD_EN				TXP_EN	FORCOL	LOOP	TXENA
0	X	X	X	0	0	0	0

NOCRC - Does not append CRC to transmitted frames when set, allows software to insert the desired CRC. Defaults to zero, namely CRC inserted.

FDSE - Full Duplex Switched Ethernet. When set, the LAN91C96I is configured for Full Duplex Switched Ethernet, it defaults clear to normal CSMA/CD protocol. In FDSE mode the LAN91C96I transmit and receive processes are fully independent, namely no deferral and no collision detection are implemented. When FDSE is set, FDUPLX is internally assumed high and MON_CSN is assumed low regardless of their actual values.

ETEN-TYPE - Early transmit underrun function type. When low, ETEN bit in the PTR register will enable the Early transmit underrun function as it was implemented in the LAN91C94. I.e. “The Early Transmit function allows the CPU to enqueue the first transmit packet before it is fully loaded in packet memory. The loading operation proceeds in parallel with the transmission, and in the case that the transmitter gets ahead of the CPU, the LAN91C96I will prevent the transmission of erroneous data by forcing an Underrun condition. Underruns will be triggered by starving the transmit DMA if the LAN91C96I detects that the DMA TX address exceeds the pointer address.”

With ETEN-TYPE set to one (1), ETEN bit set to one(1) in the pointer register will mean the following:

"For underrun detection purposes the RAM logical address and packet numbers of the packet being loaded are compared against the logical address and packet numbers of the packet being transmitted. If the packet numbers match and the logical address of the packet being transmitted exceeds the address being loaded, the LAN91C96I will prevent the transmission of erroneous data by forcing an Underrun condition. Underruns will be triggered by starving the transmit DMA if the LAN91C96I detects that the DMA TX address exceeds the pointer address."

Note: The bit may be available for chips with Rev. ID 6 only and may be assigned to a different function in the future.

EPH_LOOP - Internal loopback at the EPH block. Does not exercise the encoder decoder. Serial data is looped back when set. Defaults low. Note: After exiting the loopback test, an SRESET in the ECOR or the SOFT_RST in the RCR must be set before returning to normal operation.

STP_SQET - Stop transmission on SQET error. If set, stops and disables transmitter on SQE test error. Does not stop on SQET error and transmits next frame if clear. Defaults low.
FDUPLX - When set it enables full duplex operation. This will cause frames to be received if they pass the address filter regardless of the source for the frame. When clear the node will not receive a frame sourced by itself. Clearing this bit (Normal Operation), allows in promiscuous mode, not to receive it's own packet.

TXP_EN - This bit is reserved and should always be set to 0 on the LAN91C96I.

MON_CSN - When set the LAN91C96I monitors carrier while transmitting. It must see its own carrier by the end of the preamble. If it is not seen, or if carrier is lost during transmission, the transmitter aborts the frame without CRC and turns itself off.

When this bit is clear the transmitter ignores its own carrier. Defaults low.

PAD_EN - When set, the LAN91C96I will pad transmit frames shorter than 64 bytes with 00. Does not pad frames when reset.

FORCOL - When set the transmitter will force a collision by not deferring deliberately. After the collision this bit is reset automatically. This bit defaults low to normal operation.

LOOP - Local Loopback. When set, transmit frames are internally looped to the receiver after the encoder/decoder. Collision and Carrier Sense are ignored. No data is sent out. Defaults low to normal mode.

TXENA - Transmit enabled when set. Transmit is disabled if clear. When the bit is cleared the LAN91C96I will complete the current transmission before stopping. When stopping due to an error, this bit is automatically cleared.

Table 6 - Transmit Loop

AUI	FDSE	FDUPLX	EPH_LOOP	LOOP	LOOPS AT	TRANSMITS TO NETWORK
X	X	X	1	X	EPH Block	No
X	X	1	0	1	ENDEC	No
1	0	1	0	0	Cable	Yes
0	0	1	0	0	10BASE-T Driver	Yes
X	0	0	0	0	NORMAL CSMA/CD - No Loopback	Yes
X	1	1	0	0	FULL DUPLEX SWITCHED ETHERNET - No loopback and No SQET	Yes

I/O SPACE - BANK0

OFFSET	NAME	TYPE	SYMBOL
2	**EPH STATUS REGISTER**	**READ ONLY**	**EPHSR**

This register stores the status of the last transmitted frame. This register value, upon individual transmit packet completion, is stored as the first word in the memory area allocated to the packet. Packet interrupt processing should use the copy in memory as the register itself will be updated by subsequent packet transmissions. The register can be used for real time values (like TXENA and LINK OK). If TXENA is cleared the register holds the last packet completion status.

TX UNRN	LINK_ OK	RES	CTR _ROL	EXC _DEF	LOST CARR	LATCOL	WAKEUP
0	0	0	0	0	0	0	0
TX DEFR	LTX BRD	SQET	16COL	LTX MULT	MUL COL	SNGL COL	TX_SUC
0	0	0	0	0	0	0	0

TXUNRN - Transmit Under run. Set if Under run occurs, it also clears TXENA bit in TCR. Cleared by setting TXENA high. This bit should never be set under normal operation.

LINK_OK - State of the 10BASE-T Link Integrity Test. A transition on the value of this bit generates an interrupt when the LE ENABLE bit in the Control Register is set.

RES – This bit is reserved and will always return a zero(0). CTR_ROL - Counter Roll over. When set one or more 4 bit counters have reached maximum count (15). Cleared by reading the ECR register.

EXC_DEF - Excessive deferral. When set last/current transmit was deferred for more than 1518 * 2 byte times. Cleared at the end of every packet sent.

LOST_CARR - Lost carrier sense. When set indicates that Carrier Sense was not present at end of preamble. Valid only if MON_CSN is enabled. This condition causes TXENA bit in TCR to be reset. Cleared by setting TXENA bit in TCR.

LATCOL - Late collision detected on last transmit frame. If set a late collision was detected (later than 64 byte times into the frame). When detected the transmitter JAMs and turns itself off clearing the TXENA bit in TCR. Cleared by setting TXENA in TCR.

WAKEUP - When this bit is set, it indicates that a receive packet was received that had the “Magic” packet (MP) signature of the node’s own Individual address repetitions in it. This bit indicates a valid detection for magic packet.

TX_DEFR - Transmit Deferred. When set, carrier was detected during the first 6.4 uSec of the inter frame gap. Cleared at the end of every packet sent.

LTX_BRD - Last transmit frame was a broadcast. Set if frame was broadcast. Cleared at the start of every transmit frame.

SQET - Signal Quality Error Test. The transmitter opens a 1.6 us window 0.8 us after transmission is completed and the receiver returns inactive. During this window, the transmitter expects to see the SQET signal from the transceiver. The absence of this signal is a 'Signal Quality Error' and is reported in this status bit. Transmission stops and EPH INT is set if STP_SQET is in the TCR is also set when SQET is set. This bit is cleared by setting TXENA high.

16COL- 16 collisions reached. Set when 16 collisions are detected for a transmit frame. TXENA bit in TCR is reset. Cleared when TXENA is set high.

LTX_MULT - Last transmit frame was a multicast. Set if frame was a multicast. Cleared at the start of every transmit frame.

MULCOL - Multiple collision detected for the last transmit frame. Set when more than one collision was experienced. Cleared when TX_SUC is high at the end of the packet being sent.

SNGLCOL - Single collision detected for the last transmit frame. Set when a collision is detected. Cleared when TX_SUC is high at the end of the packet being sent.

TX_SUC - Last transmit was successful. Set if transmit completes without a fatal error. This bit is cleared by the start of a new frame transmission or when TXENA is set high.

Fatal errors are:

- 16 collisions
- SQET fail and STP_SQET = 1
- FIFO Underrun
- Carrier lost and MON_CSN = 1
- Late collision

I/O SPACE - BANK0

OFFSET	NAME	TYPE	SYMBOL
4	**RECEIVE CONTROL REGISTER**	**READ/WRITE**	**RCR**

SOFT RST	FILT CAR	0	0	0	0	STRIP CRC	RXEN
0	0	0	0	0	0	0	0
					ALMUL	PRMS	RX_ ABORT
0	0	0	0	0	0	0	0

SOFT_RST - Software activated Reset. Active high. Initiated by writing this bit high and terminated by writing the bit low. The LAN91C96I configuration is not preserved, except for Configuration, Base, and IA0-5 Registers. The EEPROM inISAmode is not reloaded after software reset.

FILT_CAR - Filter Carrier. When set filters leading edge of carrier sense for 12 bit times. Otherwise recognizes a receive frame as soon as carrier sense is active.

STRIP_CRC - When set it strips the CRC on received frames. When clear the CRC is stored in memory following the packet. Defaults low.

RXEN - Enables the receiver when set. If cleared, completes receiving current frame and then goes idle. Defaults low on reset.

ALMUL - When set accepts all multicast frames (frames in which the first bit of DA is '1'). When clear accepts only the multicast frames that match the multicast table setting. Defaults low.

PRMS - Promiscuous mode. When set receives all frames.
Change vs. LAN91C92: Does not receive its own transmission when not in full duplex(FDUPLX)!.

RX_ABORT - This bit is set if a receive frame was aborted due to length longer than 1532 bytes. The frame will not be received. The bit is cleared by RESET or by the CPU writing it low.

I/O SPACE - BANK0

OFFSET	NAME	TYPE	SYMBOL
6	**COUNTER REGISTER**	**READ ONLY**	**ECR**

Counts four parameters for MAC statistics. When any counter reaches 15 an interrupt is issued. All counters are cleared when reading the register, and do not wrap around beyond 15.

NUMBER OF EXC. DEFERRED TX				NUMBER OF DEFERRED TX			
0	0	0	0	0	0	0	0
MULTIPLE COLLISION COUNT				SINGLE COLLISION COUNT			
0	0	0	0	0	0	0	0

Each four bit counter is incremented every time the corresponding event, as defined in the EPH STATUS REGISTER bit description, occurs. Note that the counters can only increment once per enqueued transmit packet, never faster, limiting the rate of interrupts that can be generated by the counters. For example if a packet is successfully transmitted after one collision the SINGLE COLLISION COUNT field is incremented by one. If a packet experiences between 2 to 16 collisions, the MULTIPLE COLLISION COUNT field is incremented by one.

If a packet experiences deferral the NUMBER OF DEFERRED TX field is incremented by one, even if the packet experienced multiple deferrals during its collision retries.

The COUNTER REGISTER facilitates maintaining statistics in the AUTO RELEASE mode where no transmit interrupts are generated on successful transmissions.

Reading the register in the transmit service routine will be enough to maintain statistics.

I/O SPACE - BANK0

OFFSET	NAME	TYPE	SYMBOL
8	**MEMORY INFORMATION REGISTER**	**READ ONLY**	**MIR**

For software compatibility with other LAN9000 parts all memory-related information is represented in 256 x M byte units, where the multiplier M is determined by the MCR upper byte. M equals "1" for the LAN91C96I.

FREE MEMORY AVAILABLE (in BYTES* 256* M)							
0	0	0	1	1	0	0	0
MEMORY SIZE (in BYTES* 256* M)							
0	0	0	1	1	0	0	0

FREE MEMORY AVAILABLE - This register can be read at any time to determine the amount of free memory. The register defaults to the MEMORY SIZE upon reset or upon the RESET MMU command.

MEMORY SIZE - This register can be read to determine the total memory size, and will always read 18H (6144 bytes) for the LAN91C96I.

	MEMORY SIZE REGISTER	M	ACTUAL MEMORY
LAN91C90	FFH	1	64 kbytes
LAN91C90	40H	1	16 kbytes
LAN91C92/ LAN91C94	12H	1	4608 bytes
LAN91C95	18H	1	6144 bytes
LAN91C96I	18H	1	6144 bytes
LAN91C100	FFH	2	128 kbytes

I/O SPACE - BANK0

OFFSET	NAME	TYPE	SYMBOL
A	**MEMORY CONFIGURATION REGISTER**	**lower byte READ/WRITE upper byte READ ONLY**	**MCR**

				Memory Size Multiplier "M"			
0	0	1	1	0	0	1	1
Memory Reserved for Transmit (in BYTES * 256 * M)							
0	0	0	0	0	0	0	0

MEMORY RESERVED FOR TRANSMIT -
Programming this value allows the host CPU to reserve memory to be used later for transmit, limiting the amount of memory that receive packets can use up. When programmed for zero, the memory allocation between transmit and receive is completely dynamic. When programmed for a non-zero value, the allocation is dynamic if the free memory exceeds the programmed value, while receive allocation requests are denied if the free memory is less or equal to the programmed value. This register defaults to zero upon reset. It is not affected by the RESET MMU command.

The value written to the MCR is a reserved memory space IN ADDITION TO ANY MEMORY CURRENTLY IN USE. If the memory allocated for transmit plus the reserved space for transmit is required to be constant (rather than grow with transmit allocations) the CPU should update the value of this register after allocating or releasing memory.

The contents of MIR as well as the low byte of MCR are specified in 256* M bytes. The multiplier M is determined by bits 11, 10 and 9 as follows:

DEVICE	BIT 11	BIT 10	BIT 9	M	MAX MEMORY SIZE
FEAST	0	1	0	2	256* 256* 2=128k
LAN91C90	0	0	1	1	256* 256* 1=64k
FUTURE	0	1	1	4	256k
FUTURE	1	0	0	8	512k
FUTURE	1	0	1	16	1M

Note*: Bits 11, 10 and 9 are read only bits used by the software driver to transparently run on different controllers of the LAN9000 family.

I/O SPACE - BANK1

OFFSET	NAME	TYPE	SYMBOL
0	**CONFIGURATION REGISTER**	**READ/WRITE**	**CR**

The Configuration Register holds bits that define the device configuration and are not expected to change during run-time. This register is part of the EEPROM saved setup in ISA mode only.

0			NO WAIT		FULL STEP	SET SQLCH	AUI SELECT
0	X	X	0	X	0	0	0
16BIT	DIS LINK	Reserved			INT SEL1	INT SEL0	
function of EN16* pin	0	1	1	0	0	0	X

NO WAIT - When set, does not request additional wait states. An exception to this are accesses to the Data Register if not ready for a transfer. When clear, negates IOCHRDY for two to three 20MHz clocks on any cycle to the LAN91C96I.

FULL STEP - This bit is used to select the signaling mode for the AUI port. When set the AUI port uses full step signaling. Defaults low to half step signaling. This bit is only meaningful when AUI SELECT is high.

SET SQLCH - When set, the squelch level used for the 10BASE-T receive signal is 240mV. When clear the receive squelch level is 400mV. Defaults low.

AUI SELECT - When set the AUI interface is used, when clear the 10BASE-T interface is used. Defaults low.

16BIT - Used in conjunction with EN16* and IO is 8 to define the width of the system bus. If the EN16* pin is low, this bit is forced high. Otherwise the bit defaults low and can be programmed by the host CPU.

DIS LINK - This bit is used to disable the 10BASE-T link test functions. When this bit is high the LAN91C96I disables link test functions by not generating nor monitoring the network for link pulses. In this mode the LAN91C96I will transmit packets regardless of the link test, the EPHSR LINK_OK bit will be set and the LINK LED will stay on. When low the link test functions are enabled. If the link status indicates FAIL, the EPHSR LINK_OK bit will be low, while transmit packets enqueued will be processed by the LAN91C96I, transmit data will not be sent out to the cable.

INT SEL1-0 - In ISA mode, used to select one out of four interrupt pins. The three unused interrupts are tristated.

INT SEL1	INT SEL0	INTERRUPT PIN USED
0	0	INTR0
0	1	INTR1
1	0	INTR2
1	1	INTR3

I/O SPACE - BANK1

OFFSET	NAME	TYPE	SYMBOL
2	**BASE ADDRESS REGISTER**	**READ/WRITE**	**BAR**

For ISA mode only, this register holds the I/O address decode option chosen for the I/O and ROM space. It is part of the EEPROM saved setup, and is not usually modified during run-time.

A15	A14	A13	A9	A8	A7	A6	A5
0	0	0	1	1	0	0	0
ROM SIZE		RA18	RA17	RA16	RA15	RA14	
0	1	1	0	0	1	1	1

A15 - A13 and A9 - A5 - These bits are compared in ISA mode against the I/O address on the bus to determine the IOBASE for LAN91C96I registers. The 64k I/O space is fully decoded by the LAN91C96I down to a 16 location space, therefore the unspecified address lines A4, A10, A11 and A12 must be all zeros.

ROM SIZE - Determines the ROM decode area in ISA mode memory space as follows:

00 = ROM disable
01 = 16k: RA14-18 define ROM select.

10 = 32k: RA15-18 define ROM select.
11 = 64k: RA16-18 define ROM select.

RA18-RA14 - These bits are compared in ISA mode against the memory address on the bus to determine if the ROM is being accessed, as a function of the ROM SIZE. ROM accesses are read only memory accesses defined by MEMRD* going low.

For a full decode of the address space unspecified upper address lines have to be: A19 = "1", A20-A23 lines are not directly decoded, however ISA systems will only activate SMEMRD* only when A20-A23=0.

All bits in this register are loaded from the serial EEPROM in ISA Mode only.
The I/O base decode defaults to 300h (namely, the high byte defaults to 18h). ROM SIZE defaults to 01. ROM decode defaults to CC000 (namely the low byte defaults to 67h).

I/O SPACE - BANK1

OFFSET	NAME	TYPE	SYMBOL
4 THROUGH 9	**INDIVIDUAL ADDRESS REGISTERS**	**READ/WRITE**	**IAR**

These registers are loaded starting at word location 20h of the EEPROM upon hardware reset or EEPROM reload. The registers can be modified by the software driver, but a STORE operation will not modify the EEPROM Individual Address contents.

Bit 0 of Individual Address 0 register corresponds to the first bit of the address on the cable.

ADDRESS 0							
0	0	0	0	0	0	0	0

ADDRESS 1							
0	0	0	0	0	0	0	0

ADDRESS 2							
0	0	0	0	0	0	0	0

ADDRESS 3							
0	0	0	0	0	0	0	0

ADDRESS 4							
0	0	0	0	0	0	0	0

ADDRESS 5							
0	0	0	0	0	0	0	0

I/O SPACE - BANK1

OFFSET	NAME	TYPE	SYMBOL
A	GENERAL ADDRESS REGISTERS	READ/WRITE	GPR

HIGH DATA BYTE							
0	0	0	0	0	0	0	0
LOW DATA BYTE							
0	0	0	0	0	0	0	0

This register can be used as a way of storing and retrieving non-volatile information in the EEPROM to be used by the software driver. The storage is word oriented, and the EEPROM word address to be read or written is specified using the six lowest bits of the Pointer Register.

This register can also be used to sequentially program the Individual Address area of the EEPROM, that is normally protected from accidental Store operations.

This register will be used for EEPROM read and write only when the EEPROM SELECT bit in the Control Register is set. This allows generic EEPROM read and write routines that do not affect the basic setup of the LAN91C96I.

I/O SPACE - BANK1

OFFSET	NAME	TYPE	SYMBOL
C	CONTROL REGISTER	READ/WRITE	CTR

0	RCV_ BAD	PWRDN	WAKEUP_ EN	AUTO RELEASE			1
0	0	0	0	0	X	X	1
LE ENABLE	CR ENABLE	TE ENABLE			EEPROM SELECT	RELOAD	STORE
0	0	0	X	X	0	0	0

RCV_BAD - When set, bad CRC packets are received. When clear bad CRC packets do not generate interrupts and their memory is released.

PWRDN - Active high bit used to put the Ethernet function in power down mode.

Cleared by:

1. A write to any register in the LAN91C96I I/O space.
2. Hardware reset. This bit is combined with the Pwrdwn bit in ECSR and with the powerdown bit to determine when the function is powered down.

WAKUP_EN - Active high bit used to enable the controller in the appropriate power down modes to power up and set the WAKEUP bit in the EPHSR -> generate an EPH interrupt(if not masked). When clear (0), no “Magic Packet” scanning is done on receive packets.

Note: Setting (1) the bit is meaningful only if the function is enabled (Enable Function bit in COR; offset 8000h)

AUTO RELEASE - When set, transmit pages are released by transmit completion if the transmission was successful (when TX_SUC is set). In that case there is no status word associated with its packet number, and successful packet numbers are not even written into the TX COMPLETION FIFO.

A sequence of transmit packets will only generate an interrupt when the sequence is completely transmitted (TX EMPTY INT will be set), or when a packet in the sequence experiences a fatal error (TX INT will be set). Upon a fatal error TXENA is cleared and the transmission sequence stops. The packet number that failed is the present in the FIFO PORTS register, and its pages are not released, allowing the CPU to restart the sequence after corrective action is taken.

LE ENABLE - Link Error Enable. When set it enables the LINK_OK bit transition as one of the interrupts merged into the EPH INT bit. Defaults low (disabled). Writing this bit also serves as the acknowledge by clearing previous LINK interrupt conditions.

CR ENABLE - Counter Roll over Enable. When set it enables the CTR_ROL bit as one of the interrupts merged into the EPH INT bit. Defaults low (disabled).

TE ENABLE - Transmit Error Enable. When set it enables Transmit Error as one of the interrupts merged into the EPH INT bit. Defaults low (disabled). Transmit Error is any condition that clears TXENA with TX_SUC staying low as described in the EPHSR register.
EEPROM SELECT - This bit allows the CPU to specify which registers the EEPROM RELOAD or STORE refers to. When high, the General Purpose Register is the only register read or written. When low, the RELOAD and STORE functions are enabled.

RELOAD
The LAN91C96I reads the Configuration, Base and Individual Address, and STORE writes the Configuration and Base registers.

Also when set it will read the EEPROM and update relevant registers with its contents. This bit then Clears upon completing the operation.

STORE
The STORE LAN91C96I bit when set, stores the contents of all relevant registers in the serial EEPROM. This bit is cleared upon completing the operation.

Note: When an EEPROM access is in progress the STORE and RELOAD bits will be read back as high. The remaining 14 bits of this register will be invalid. During this time, attempted read/write operations, other than polling the EEPROM status, will NOT have any effect on the internal registers. The CPU can resume accesses to the LAN91C96I after both bits are low. A worst case RELOAD operation initiated by RESET or by software takes less than 750usec in either mode.

I/O SPACE - BANK2

OFFSET	NAME	TYPE	SYMBOL
0	**MMU COMMAND REGISTER**	**WRITE ONLY BUSY bit readable**	**MMUCR**

This register is used by the CPU to control the memory allocation, de-allocation, TX FIFO and RX FIFO control. The three command bits determine the command issued as described below:

COMMAND				0	N2	N1	N0/ BUSY
w	x	y	z				
							0

COMMAND SET:
wxyz

0000 0) - NOOP - NO OPERATION -

0010 2) - ALLOCATE MEMORY FOR TX - N2, N1, N0 defines the amount of memory requested as (value + 1) 256* bytes. Namely N2, N1, N0 = 1 will request 2 256* = 512 bytes. Valid range for N2, N1, N0 is 0 through 5. A shift-based divide by 256 of the packet length yields the appropriate value to be used as N2, N1 and N0. Immediately generates a completion code at the ALLOCATION RESULT REGISTER. Can optionally generate an interrupt on successful completion. The allocation time can take worst case (N2, N1, N0 + 2)* 200µs.

0100 4) - RESET MMU TO INITIAL STATE - Frees all memory allocations, clears relevant interrupts, resets packet FIFO pointers.

0110 6) - REMOVE FRAME FROM TOP OF RX FIFO- To be issued after CPU has completed processing of present receive frame. This command removes the receive packet number from the RX FIFO and brings the next receive frame (if any) to the RX area (output of RX FIFO).

0111 7) - REMOVE FRAME FROM TOP OF TX FIFO- To be issued ONLY after the Host disabled the transmitter and has completed processing of the present transmit frame. Note: Determining Transmit completion is done by polling the TEMPTY bit in the Transmit FIFO Port Register. This command removes the Transmit packet number from the TX FIFO and brings the next Transmit frame (if any) to the TX area (output of TX FIFO).

1000 8) - REMOVE AND RELEASE TOP OF RX FIFO - Like 6) but also releases all memory used by the packet presently at the RX FIFO output.

1010 A) - RELEASE SPECIFIC PACKET - Frees all pages allocated to the packet specified in the PACKET NUMBER REGISTER. Should not be used for frames pending transmission. Typically used to remove transmitted frames, after reading their completion status. Can be used following 6 (to release receive packet memory in a more flexible way than 8).

1100 C) - ENQUEUE PACKET NUMBER INTO TX FIFO - This is the normal method of transmitting a packet just loaded into RAM. The packet number to be enqueued is taken from the PACKET NUMBER REGISTER.

1110 F) - RESET TX FIFOs - This command will reset both TX FIFOs. The TX FIFO holding the packet numbers awaiting transmission and the TX Completion FIFO. This command provides a mechanism for canceling packet transmissions, and reordering or bypassing the transmit queue.

The RESET TX FIFOs command should only be used when the transmitter is disabled. Unlike the RESET MMU command, the RESET TX FIFOs does not release any memory.

Note 1: Only command 2 uses N2, N1 and N0.

Note 2: When using the RESET TX FIFOS command, the CPU is responsible for releasing the memory associated with outstanding packets, or re-enqueuing them. Packet numbers in the completion FIFO can be read via the FIFO ports register before issuing the command.

Note 3: MMU commands releasing memory (commands 8 and A) should only be issued if the corresponding packet number has memory allocated to it.

COMMAND SEQUENCING

A second allocate command (command 2) should not be issued until the present one has completed. Completion is determined by reading the FAILED bit of the allocation result register or through the allocation interrupt. A second release command (commands 8 and A) should not be issued if the previous one is still being processed. The BUSY bit indicates that a release command is in progress. After issuing command A, the contents of the PNR should not be changed until BUSY goes low. After issuing command 8, command 6 should not be issued until BUSY goes low. BUSY BIT - Readable at bit “0” of the MMU command register address. When set indicates that MMU is still processing a release command. When clear, MMU has already completed last release command. BUSY and FAILED bits are set upon the trailing edge of command.

I/O SPACE - BANK2

OFFSET	NAME	TYPE	SYMBOL
1	AUTO TX START REGISTER	READ/WRITE	AUTOTX

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

AUTO TX START REGISTER - This register specifies the value, in 16 byte multiples of when the transmit state machine starts a transmit operation when the associated transmit buffer is enqueued into the transmit FIFO.

The AutoTx bit as well as the ETEN bit must both be set in the pointer register in order for this register to be utilized. Note: This register must be non-zero for the Auto-Tx function to work. A value of ”0” will disable this function. The RCV bit in the Pointer register must be zero (0) as well. The RCV bit must be cleared so that the packet being written and enqueued is being selected by the PNR and not the receive FIFO.

Register Operation: When Early Transmit is enabled via the ETEN bit in the pointer register, the host is able to enqueue a buffer for transmit operation before all of the transmitted data is copied into the LAN91C96I dual ported RAM. In the case of the AutoTx bit being cleared, the host must manually start the transmit operation. When the AutoTx bit is set, the EPH Transmit engine compares the number of bytes moved into the transmit packet buffer with the value of the Auto TX Start Register to start transmit operation. This eliminates the requirement for the host to manually start the transmit.

I/O SPACE - BANK2

OFFSET	NAME	TYPE	SYMBOL
2	**PACKET NUMBER REGISTER**	**READ/WRITE**	**PNR**

RESERVED			PACKET NUMBER AT TX AREA				
0	0	0	0	0	0	0	0

PACKET NUMBER AT TX AREA - The value written into this register determines which packet number is accessible through the TX area. Some MMU commands use the number stored in this register as the packet number parameter. This register is cleared by a RESET or a RESET MMU Command.

RESERVED – This bit is reserved.

I/O SPACE - BANK2

OFFSET	NAME	TYPE	SYMBOL
3	**ALLOCATION RESULT REGISTER**	**READ ONLY**	**ARR**

This register is updated upon an ALLOCATE MEMORY MMU command.

FAILED			ALLOCATED PACKET NUMBER				
1	0	0	0	0	0	0	0

FAILED - A ”0” indicates a successful allocation completion. If the allocation fails the bit is set and only cleared when the pending allocation is satisfied. Defaults high upon reset and reset MMU command. For polling purposes, the ALLOC_INT in the Interrupt Status Register should be used because it is synchronized to the read operation.

Sequence:
1) Allocate Command
2) Poll ALLOC_INT bit until set
3) Read Allocation Result Register

ALLOCATED PACKET NUMBER - Packet number associated with the last memory allocation request. The value is only valid if the FAILED bit is clear.

Note: For software compatibility with future versions, the value read from the ARR after an allocation request is intended to be written into the PNR as is, without masking higher bits (provided FAILED = “0”).

I/O SPACE - BANK2

OFFSET	NAME	TYPE	SYMBOL
4	**FIFO PORTS REGISTER**	**READ ONLY**	**FIFO**

This register provides access to the read ports of the Receive FIFO and the Transmit completion FIFO. The packet numbers to be processed by the interrupt service routines are read from this register.

REMPTY			RX FIFO PACKET NUMBER				
1	0	0	0	0	0	0	0

TEMPTY			TX FIFO/DONE PACKET NUMBER				
1	0	0	0	0	0	0	0

REMPTY - No receive packets queued in the RX FIFO. For polling purposes, uses the RCV_INT bit in the Interrupt Status Register.

TOP OF RX FIFO PACKET NUMBER - Packet number presently at the output of the RX FIFO. Only valid if REMPTY is clear. The packet is removed from the RX FIFO using MMU Commands 3) or 4).

TEMPTY - No transmit packets in completion queue. For polling purposes, uses the TX_INT bit in the Interrupt Status Register.

TX DONE PACKET NUMBER - Packet number presently at the output of the TX Completion FIFO. Only valid if TEMPTY is clear. The packet is removed when a TX INT acknowledge is issued.

Note:

1) For software compatibility with future versions, the value read from each FIFO register is intended to be written into the PNR as is, without masking higher bits (provided TEMPTY and REMPTY = 0 respectively).

I/O SPACE - BANK2

OFFSET	NAME	TYPE	SYMBOL
6	POINTER REGISTER	READ/WRITE	PTR

RCV	AUTO INCR.	READ	ETEN	AutoTx	POINTER HIGH		
0	0	0	0	0	0	0	0
POINTER LOW							
0	0	0	0	0	0	0	0

POINTER REGISTER - The value of this register determines the address to be accessed within the transmit or receive areas. It will auto-increment on accesses to the data register when AUTO INCR. is set. The increment is by one for every byte access, and by two for every word access. When RCV is set the address refers to the receive area and uses the output of RX FIFO as the packet number, when RCV is clear the address refers to the transmit area and uses the packet number at the Packet Number Register.

READ bit - Determines the type of access to follow. If the READ bit is high the operation intended is a read. If the READ bit is low the operation is a write. Loading a new pointer value, with the READ bit high, generates a pre-fetch into the Data Register for read purposes.

Read-back of the pointer will indicate the value of the address last accessed by the CPU (rather than the last pre-fetched). This allows any interrupt routine that uses the pointer, to save it and restore it without affecting the process being interrupted.

The Pointer Register should not be loaded until 400ns after the last write operation to the Data Register to ensure that the Data Register FIFO is empty. On reads, if IOCHRDY is not connected to the host, the Data Register should not be read before 400ns after the pointer was loaded to allow the Data Register FIFO to fill.

If the pointer is loaded using 8 bit writes, the low byte should be loaded first and the high byte last.

ETEN bit - When set enables EARLY Transmit underrun detection. Normal operation when clear.

If TCR bit 14 (ETEN-TYPE) is zero and this bit is set, the Early transmit underrun function will be enabled as it was implemented in the LAN91C94:

"The Early Transmit function allows the CPU to enqueue the first transmit packet before it is fully loaded in packet memory. The loading operation proceeds in parallel with the transmission, and in the case that the transmitter gets ahead of the CPU, the LAN91C94 will prevent the transmission of erroneous data by forcing an Underrun condition. Underruns will be triggered by starving the transmit DMA if the LAN91C96I detects that the DMA TX address exceeds the pointer address."

If TCR bit 14 (ETEN-TYPE) is zero and this bit is set, the Early transmit underrun function defined as follows:

“For underrun detection purposes the RAM logical address and packet numbers of the packet being loaded are compared against the logical address and packet numbers of the packet being transmitted. If the packet numbers match and the logical address of the packet being transmitted exceeds the address being loaded the LAN91C96I will prevent the transmission of erroneous data by forcing an Underrun condition. Underruns will be triggered by starving the transmit DMA if the LAN91C96I detects that the DMA TX address exceeds the pointer address.”

Note: ETEN-TYPE (bit 14) in TCR may be implemented for Rev. ID 6 only. In the absence of ETEN-TYPE in TCR, ETEN will have the definition as ETEN-TYPE were clear only.

AutoTx bit - When set, enables the transmit state machine to Automatically start a transmit operation with no host intervention determined by the number of bytes being copied into the transmit buffer enqueued in the transmit FIFO. The ETEN bit must also be set in order for this function to be enabled and the RCV bit must be cleared (0). When the Auto TX bit is cleared, the transmit state machine must manually be enabled to enqueue a transmit buffer.

If AUTO INCR. is not set, the pointer must be loaded with an even value.

I/O SPACE - BANK2

OFFSET	NAME	TYPE	SYMBOL
8 & A	DATA REGISTER	READ/WRITE	DATA

DATA HIGH

DATA LOW

DATA REGISTER - Used to read or write the data buffer byte/word presently addressed by the pointer register.

This register is mapped into two uni-directional FIFOs that allow moving words to and from the LAN91C96I regardless of whether the pointer address is even or odd. Data goes through the write FIFO into memory, and is pre-fetched from memory into the read FIFO. If byte accesses are used, the appropriate (next) byte can be accessed through the Data Low or Data High registers. The order to and from the FIFO is preserved. Byte and word accesses can be mixed on the fly in any order.

This register is mapped into two consecutive word locations to facilitate the usage of double word move instructions. The DATA register is accessible at any address in the 8 through Ah range, while the number of bytes being transferred are determined by A0 and nSBHE in ISA mode.

I/O SPACE - BANK2

OFFSET	NAME	TYPE	SYMBOL
C	INTERRUPT STATUS REGISTER	READ ONLY	IST

TX IDLE INT	ERCV INT	EPH INT	RX_ OVRN INT	ALLOC INT	TX EMPTY INT	TX INT	RCV INT
0	0	0	0	0	1	0	0

OFFSET	NAME	TYPE	SYMBOL
C	INTERRUPT ACKNOWLEDGE REGISTER	WRITE ONLY	ACK

	ERCV INT		RX_ OVRN INT		TX EMPTY INT	TX INT	

OFFSET	NAME	TYPE	SYMBOL
D	INTERRUPT MASK REGISTER	READ/WRITE	MSK

TX IDLE INT	ERCV INT	EPH INT	RX_ OVRN INT	ALLOC INT	TX EMPTY INT	TX INT	RCV INT
0	0	0	0	0	0	0	0

This register can be read and written as a word or as two individual bytes.

The Interrupt Mask Register bits enable the appropriate bits when high and disable them when low. An enabled bit being set will cause a hardware interrupt.

EPH INT - Set when the Ethernet Protocol Handler section indicates one out of various possible special conditions. This bit merges exception type of interrupt sources, whose service time is not critical to the execution speed of the low level drivers. The exact nature of the interrupt can be obtained from the EPH Status Register (EPHSR), and enabling of these sources can be done via the Control Register.

The possible sources are:

- LINK_OK transition.
- CTR_ROL - Statistics counter roll over.
- TXENA cleared - A fatal transmit error occurred forcing TXENA to be cleared. TX_SUC will be low
- and the specific reason will be reflected by the bits:
- TXUNRN - Transmit underrun.
- SQET - SQE Error.
- LOST CARR - Lost Carrier.
- LATCOL - Late Collision.
- 16COL - 16 collisions.
- WAKE_UP - “Magic Packet” is received if enabled

RX_OVRN INT - Set when the receiver overruns due to a failed memory allocation. The RX_OVRN INT bit latches the overrun condition for the purpose of being polled or generating an interrupt, and will only be cleared by writing the acknowledge register with the RX_OVRN INT bit set.

ALLOC INT - Set when an MMU request for TX pages allocation is completed.

This bit is the complement of the FAILED bit in the ALLOCATION RESULT register. The ALLOC INT ENABLE bit should only be set following an allocation command, and cleared upon servicing the interrupt.
TX EMPTY INT - Set if the TX FIFO goes empty, can be used to generate a single interrupt at the end of a sequence of packets enqueued for transmission. This bit latches the empty condition, and the bit will stay set until it is specifically cleared by writing the acknowledge register with the TX EMPTY INT bit set. If a real time reading of the FIFO empty is desired, the bit should be first cleared and then read.

The TX EMPTY INT ENABLE should only be set after the following steps:

1) A packet is enqueued for transmission.
2) The previous empty condition is cleared (acknowledged).

TX INT - Set when at least one packet transmission was completed. The first packet number to be serviced can be read from the FIFO PORTS register. The TX INT bit is always the logic complement of the TEMPTY bit in the FIFO PORTS register.

After servicing a packet number, its TX INT interrupt is removed by writing the Interrupt Acknowledge Register with the TX INT bit set.

RCV INT - Set when a receive interrupt is generated. The first packet number to be serviced can be read from the FIFO PORTS register. The RCV INT bit is always the logic complement of the REMPTY bit in the FIFO PORTS register.

ERCV INT - Early receive interrupt. Set whenever a receive packet is being received, and the number of bytes received into memory exceeds the value programmed as ERCV THRESHOLD (Bank 3, Offset Ch). ERCV INT stays set until acknowledged by writing the INTERRUPT ACKNOWLEDGE REGISTER with the ERCV INT bit set.

TX IDLE INT - Transmit Idle interrupt. Set when the transmit state machine is not active. This bit is used under the condition where the TX FIFO is still NOT empty, the transmitter is disabled and the host wants to determine when the transmitter is completed with the current transmit packet. This event usually happens when the host wants to insert at the head of the transmit queue a flow control frame for example.

Typical flow of events/Condition:

1) The transmit FIFO is not empty
2) The transmit DONE FIFO is either empty or not empty
3) The transmit engine is either active or not active

Flow of events for an insertion of a transmit packet (Typical Application Example: Flow Control packet):

1) Disable the Transmitter
2) Remove and release any “transmit done” packets in the TX DONE FIFO
3) Via polling or an interrupt driven event, determine status of TX IDLE INT bit and wait until this bit is set. This will determine when the transmitter is truly done with all transmit events.
4) Remove and store (if any, in software) Packet numbers from the transmit FIFO. (These packets will later be restored into the TX FIFO after the control frame is inserted into the front of the TX FIFO).
5) Enable Transmitter
6) En-queue packet into TX FIFO
7) En-queue rest of packets, if any, into TX FIFO (restore TX FIFO)

Note: If the driver uses AUTO RELEASE mode it should enable TX EMPTY INT as well as TX INT. TX EMPTY INT will be set when the complete sequence of packets is transmitted. TX INT will be set if the sequence stops due to a fatal error on any of the packets in the sequence.

Note: For edge triggered systems, the Interrupt Service Routine should clear the Interrupt Mask Register, and only enable the appropriate interrupts after the interrupt source is serviced (acknowledged).

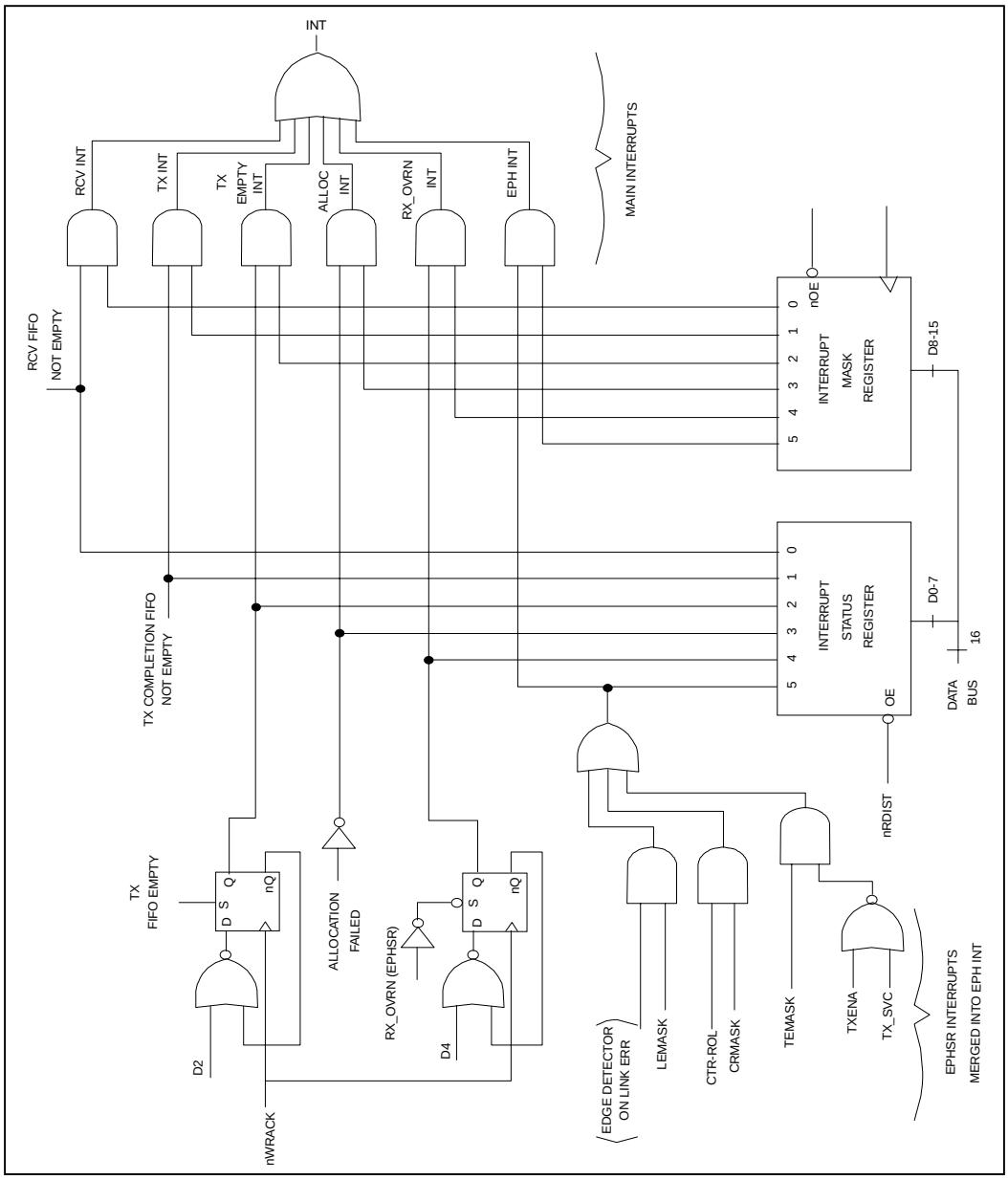


FIGURE 12 - INTERRUPT STRUCTURE

I/O SPACE - BANK 3

OFFSET	NAME	TYPE	SYMBOL
0 THROUGH 7	MULTICAST TABLE	READ/WRITE	MT

Multicast Table 0							
0	0	0	0	0	0	0	0
Multicast Table 1							
0	0	0	0	0	0	0	0
Multicast Table 2							
0	0	0	0	0	0	0	0
Multicast Table 3							
0	0	0	0	0	0	0	0
Multicast Table 4							
0	0	0	0	0	0	0	0
Multicast Table 5							
0	0	0	0	0	0	0	0
Multicast Table 6							
0	0	0	0	0	0	0	0
Multicast Table 7							
0	0	0	0	0	0	0	0

The 64 bit multicast table is used for group address filtering. The hash value is defined as the six most significant bits of the CRC of the destination addresses. The three msb's determine the register to be used (MT0-7), while the other three determine the bit within the register. If the appropriate bit in the table is set, the packet is received.

If the ALMUL bit in the RCR register is set, all multicast addresses are received regardless of the multicast table values. Hashing is for a partial group address filtering scheme. Additional filtering is done in software. But the hash value being a part of the receive status word, the receive routine can reduce the search time significantly. With the proper memory structure, the search is limited to comparing only the multicast addresses that have the actual hash value in question.

I/O SPACE - BANK3

OFFSET	NAME	TYPE	SYMBOL
8	MANAGEMENT INTERFACE	READ/WRITE	MGMT

This register contains status bits and control bits for management of different transceivers modules. Some of the pins are shared with the serial EEPROM interface. Management is software controlled, and does not use the serial EEPROM and the transceiver management functions at the same time.

				nXNDEC	IOS2	IOS1	IOS0
0	0	1	1				

				MDOE	MCLK	MDI	MD0
0	0	1	1	0	0	0	0

nXNDEC - Read only bit reflecting the status of the nXENDEC pin.

IOS0-2 - Read only bits reflecting the status of the IOS0-2 pins.

MDO - The value of this bit drives the EEDO pin when MDOE=1.

MDCLK - The value of this bit drives the EESK pin when MDOE=1.

MDOE - When this bit is high pins EEDO EECS and EESK will be used for transceiver management functions, otherwise the pins assume the EEPROM values.

	MODE=0	MODE=1
EEDO	Serial EEPROM Data Out	Bit MDO
EESK	Serial EEPROM Clock	Bit MCLK
EECS	Serial EEPROM Chip Select	0

I/O SPACE - BANK3

OFFSET	NAME	TYPE	SYMBOL
A	REVISION REGISTER	READ ONLY	REV

0	0	1	1	0	0	1	1
CHIP				REV			
0	1	0	0	0	0	0	0

CHIP ID VALUE	DEVICE
3	LAN91C90/LAN91C92
4	LAN91C94
5	LAN91C95
4*	LAN91C96I
7	LAN91C100
8	LAN91C100FD
9	LAN91C110

CHIP - Chip ID. Can be used by software drivers to identify the device used.

REV - Revision ID. Incremented for each revision of a given device.

Note*: The LAN91C96I shares the same chip ID (#4) as the LAN91C94. The Rev. ID for the LAN91C96I will begin from six (#6).

I/O SPACE - BANK3

OFFSET	NAME	TYPE	SYMBOL
C	EARLY RCV REGISTER	READ/WRITE	ERCV

RCV COUNTER							
0	0	1	1	0	0	1	1
RCV DISCRD			ERCV THRESHOLD				
0	0	0	1	1	1	1	1

RCV DISCRD - Set to discard a packet being received.

ERCV THRESHOLD - Threshold for ERCV interrupt. Specified in 64 byte multiples. Whenever the number of bytes written in memory for the presently received packet exceeds the ERCV THRESHOLD, ERCV INT bit of the INTERRUPT STATUS REGISTER is set.

Rcv Counter - This 8 bit value is the “Real Time” count, in bytes, of the current Receive packet (this includes the 4 bytes of status and packet length). The count is rounded to the nearest Nibble (16 bytes). The Counter is multiplied by 16 decimals to obtain the number of bytes currently received.

Note: The value of the RCV Counter is in real time asynchronous format (i.e. The value is constantly changing). It is recommended that the register be read multiple times to get an accurate reading. Note: The Rcv Counter register will return a value of “0” when no receive event is occurring.

THEORY OF OPERATION

The concept of presenting the shared RAM as a FIFO of packets, with a memory management unit allocating memory on a per packet basis responds to the following needs:

Memory allocation for receive vs. transmit - A fixed partition between receive and transmit area would not be efficient. Being able to dynamically allocate it to transmit and receive represents almost the equivalent of duplicating the memory size for some workstation type of drivers.

Software overhead - By presenting a FIFO of packets, the software driver does not have to waste any time in calculating pointers for the different buffers that make up different packets. The driver usually deals with one packet at a time. With this approach, packets are accessible always at the same fixed address, and access is provided to any byte of the packet.

Headers can be analyzed without reading out the entire packet. The packet can be moved in or out with a block move operation.

Multiple upper layer support - The LAN91C96I facilitates interfacing to multiple upper layer protocols because of the receive packet processing flexibility. A receive lookahead scheme like ODI or NDIS drivers is supported by copying a small part of the received packet and letting the upper layer provide a pointer for the rest of the data. If the upper layer indicates it does not want the packet, it can be removed upon a single command. If the upper layer wants a specific part of the packet, a block move operation starting at any particular offset can be done. Out of order receive processing is also supported: if memory for one packet is not yet available, receive packet processing can continue.

Efficiency - Lacking any level of indirection or linked lists of pointers, virtually all the memory is used for data. There are no descriptors, forward links and pointers at all. This simplicity and memory efficiency is accomplished without giving up the benefits of linked lists which is unlimited back-to-back transmission and reception without CPU intervention for as long as memory is available.

FULL DUPLEX SUPPORT

Full Duplex Ethernet operation refers to the ability of the network (or parts of it) to simultaneously transmit and receive packets. The CSMA/CD protocol used by Ethernet for accessing a shared medium is inherently half duplex , and so is the 10BASE-T physical layer where simultaneous transmit and receive activity is interpreted as a collision.

The LAN91C96I supports two types of Full Duplex operation:

1) Full Duplex mode for diagnostic purposes only, where the received packet is the transmit packet being looped back. This mode is enabled using the FDUPLX bit in the TCR. In this mode the CSMA/CD algorithm is used to gain access to the media.
2) FDSE (Full Duplex Switched Ethernet). Enabled by FDSE bit in TCR bit. When the LAN91C96I is configured for FDSE, its transmit and receive paths will operate independently with Carrier Sense CSMA/CD function disabled.

Note: In FDSE mode the packets are not looped back internally. The loopback (Full Duplex for Diagnostics(FDUPLX)) function of 10BASE-T transceivers is permanently engaged. It presents the transmit pair waveform to the receive circuit internally. This function allows the receiver to see the controller's own transmission, not only to permit diagnostics, but also to ensure sure that the node defers to its own transmission - as specified in 802.3.

Behavior in FDSE mode

A) No deferral - The transmit channel is dedicated and always available - The device transmits whenever it has a packet ready to be sent, while respecting the interframe spacing between transmit packets.

B) No collision detection - There are no collisions in a switched full duplex environment.

MAGIC PACKET SUPPORT

If the WAKEUP_EN bit in the Control Register (Bank1, Offset C) is set, the controller will generate the interrupt If this bit is not set, this functionality is disabled. Setting (1) the bit is meaningful only if the function is enabled.

When a magic packet is received, the Ethernet controller will generate an interrupt causing the host to initiate a service routine to find the source of the event. The Interrupt bit in the ECSR is also set if the host plans on polling the controller for Wakeup status.

TYPICAL FLOW OF EVENTS FOR TRANSMIT

	S/W DRIVER	CSMA/CD SIDE
1	ISSUE ALLOCATE MEMORY FOR TX - N BYTES - the MMU attempts to allocate N bytes of RAM.	
2	WAIT FOR SUCCESSFUL COMPLETION CODE - Poll until the ALLOC INT bit is set or enable its mask bit and wait for the interrupt. The TX packet number is now at the Allocation Result Register.	
3	LOAD TRANSMIT DATA - Copy the TX packet number into the Packet Number Register. Write the Pointer Register, then use a block move operation from the upper layer transmit queue into the Data Register.	
4	ISSUE "ENQUEUE PACKET NUMBER TO TX FIFO" - This command writes the number present in the Packet Number Register into the TX FIFO. The transmission is now enqueued. No further CPU intervention is needed until a transmit interrupt is generated.	
5		The enqueued packet will be transferred to the CSMA/CD block as a function of TXENA (in TCR) bit and of the deferral process state.
6		Upon transmit completion the first word in memory is written with the status word. The packet number is moved from the TX FIFO into the TX completion FIFO. Interrupt is generated by the TX completion FIFO being not empty.
7	SERVICE INTERRUPT - Read Interrupt Status Register. If it is a transmit interrupt, read the TX Done Packet Number from the Fifo Ports Register. Write the packet number into the Packet Number Register. The corresponding status word is now readable from memory. If status word shows successful transmission, issue RELEASE packet number command to free up the memory used by this packet. Remove packet number from completion FIFO by writing TX INT Acknowledge Register.	

TYPICAL FLOW OF EVENTS FOR RECEIVE

	S/W DRIVER	CSMA/CD SIDE
1	ENABLE RECEPTION - By setting the RXEN bit.	
2		A packet is received with matching address. Memory is requested from MMU. A packet number is assigned to it. Additional memory is requested if more pages are needed.
3		The internal DMA logic generates sequential addresses and writes the receive words into memory. The MMU does the sequential to physical address translation. If overrun, packet is dropped and memory is released.
4		When the end of packet is detected, the status word is placed at the beginning of the receive packet in memory. Byte count is placed at the second word. If the CRC checks correctly the packet number is written into the RX FIFO. The RX FIFO being not empty causes RCV INT (interrupt) to be set. If CRC is incorrect the packet memory is released and no interrupt will occur.
5	SERVICE INTERRUPT - Read the Interrupt Status Register and determine if RCV INT is set. The next receive packet is at receive area. (Its packet number can be read from the FIFO Ports Register). The software driver can process the packet by accessing the RX area, and can move it out to system memory if desired. When processing is complete the CPU issues the REMOVE AND RELEASE FROM TOP OF RX command to have the MMU free up the used memory and packet number.	

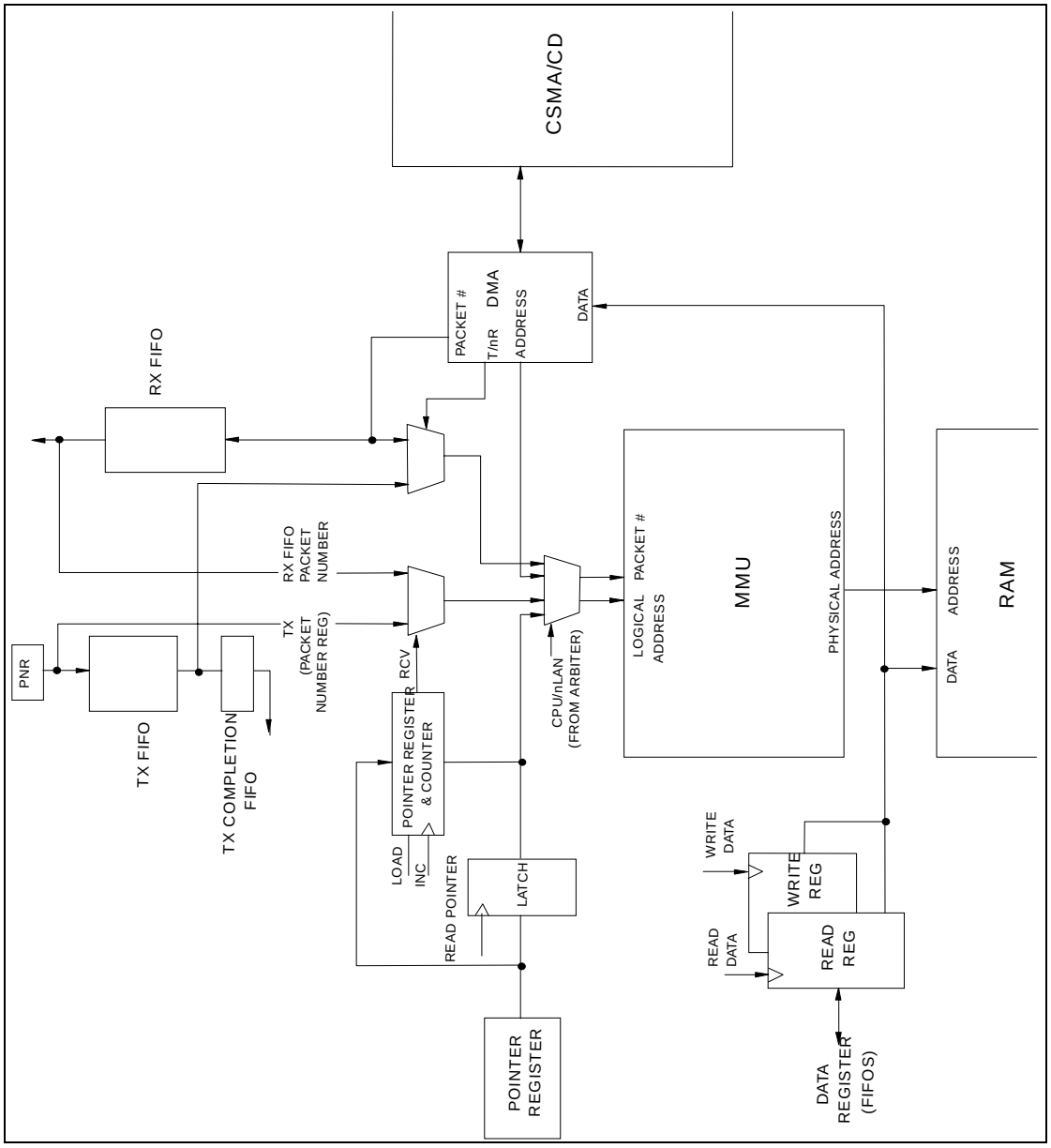


FIGURE 13 - INTERRUPT SERVICE ROUTINE

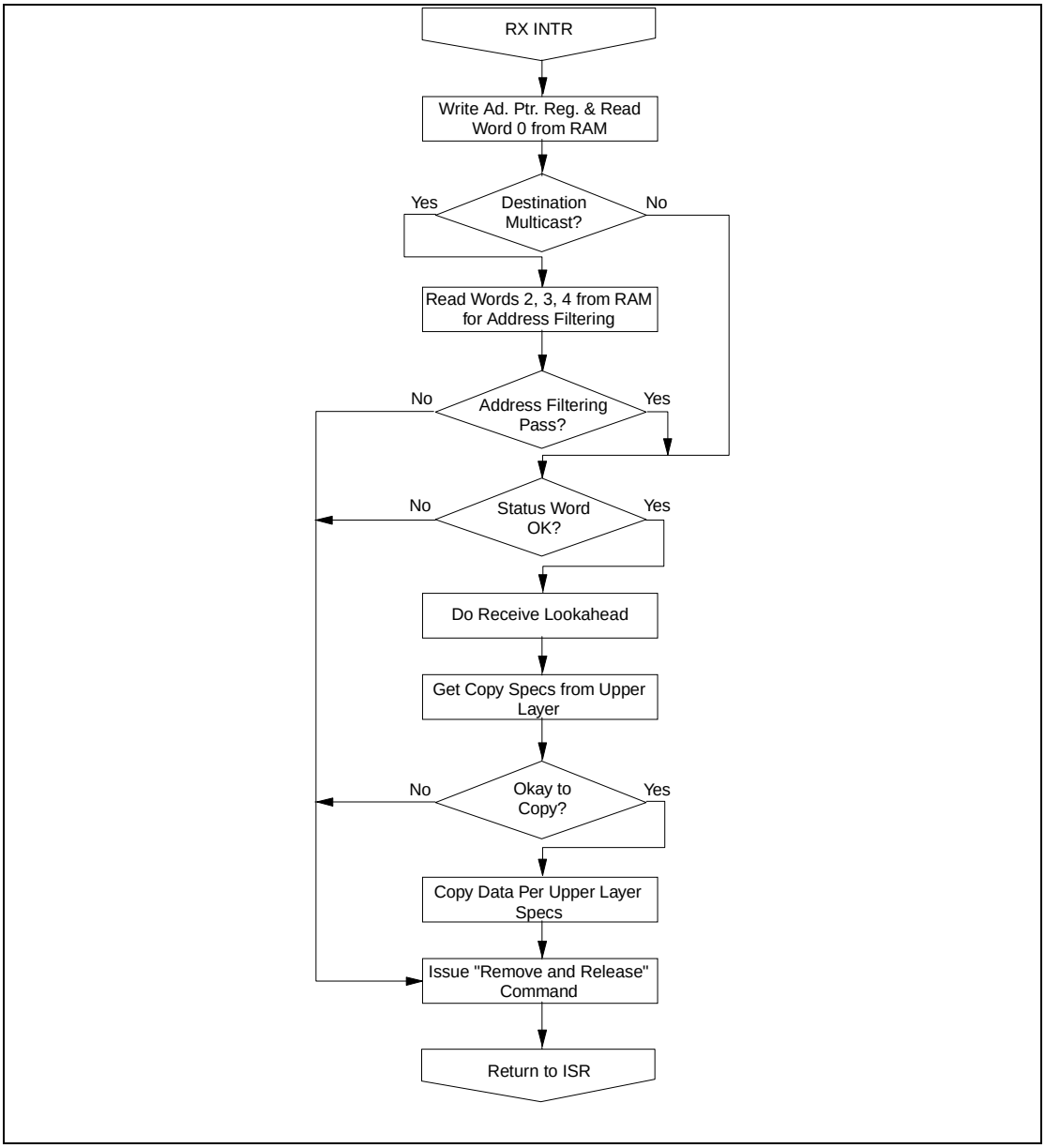


FIGURE 14 – RX INTR

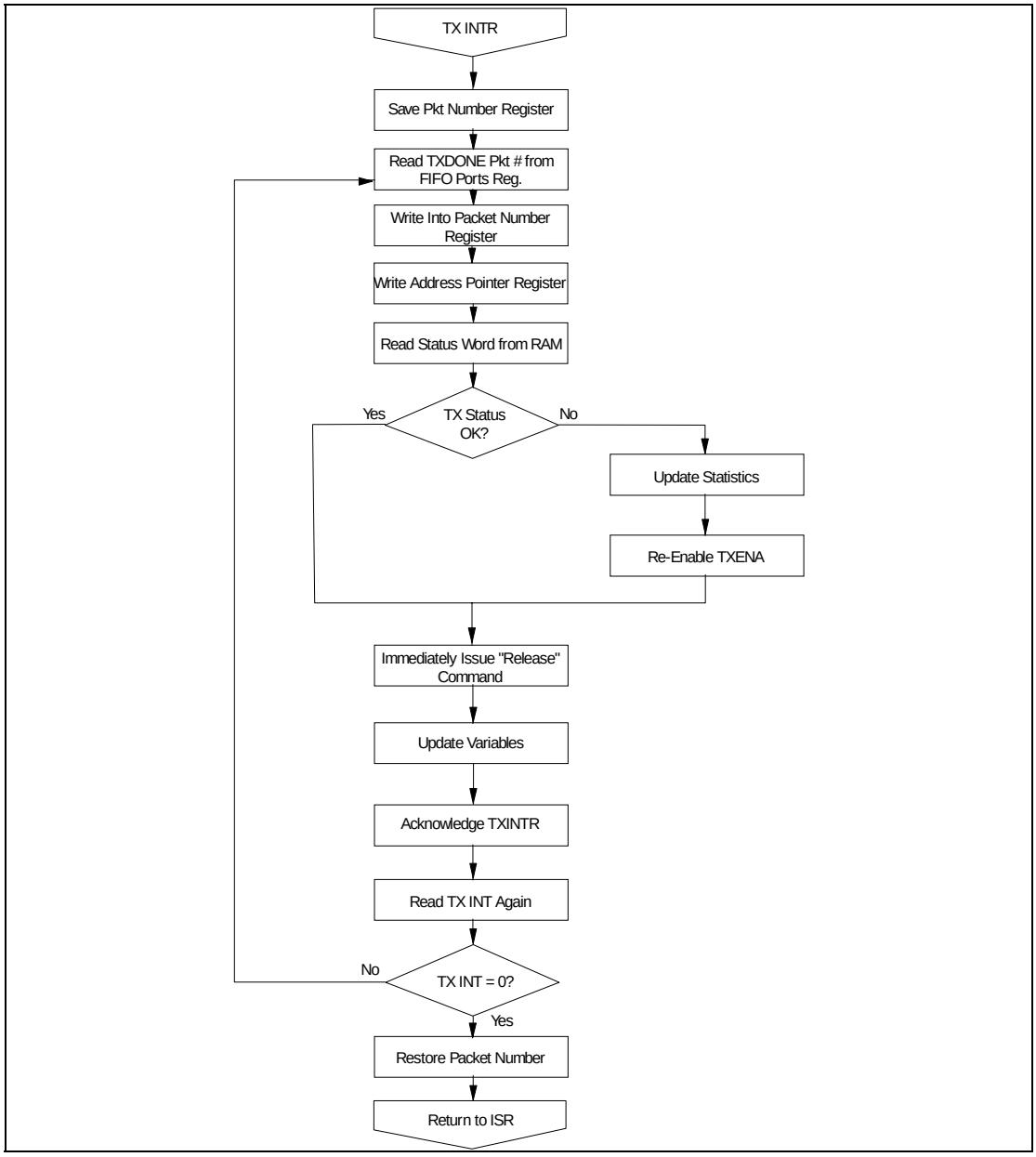


FIGURE 15 – TX INTR

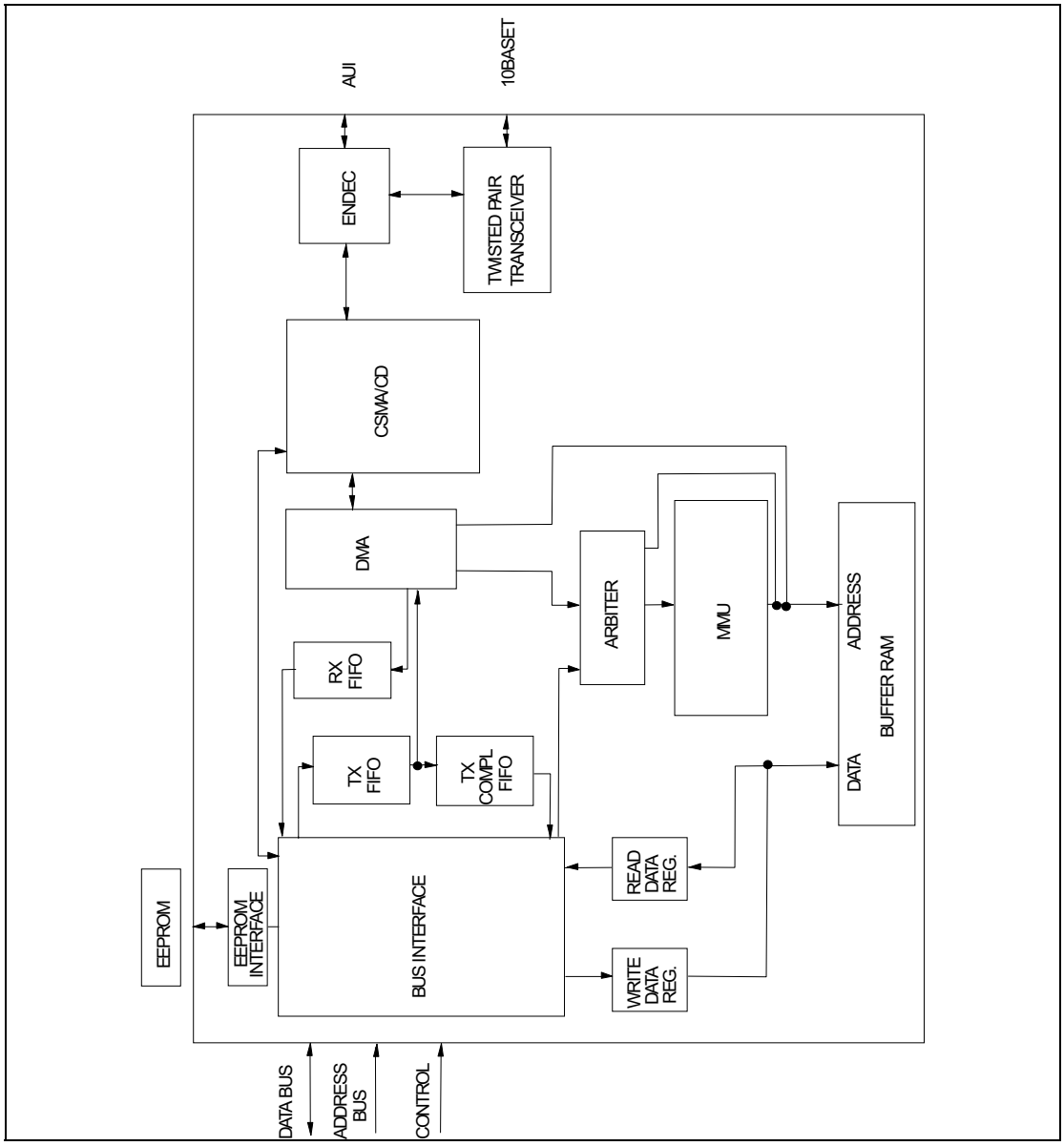


FIGURE 16 – TXEMPTY INTR

(Assumes Auto Release Option Selected)

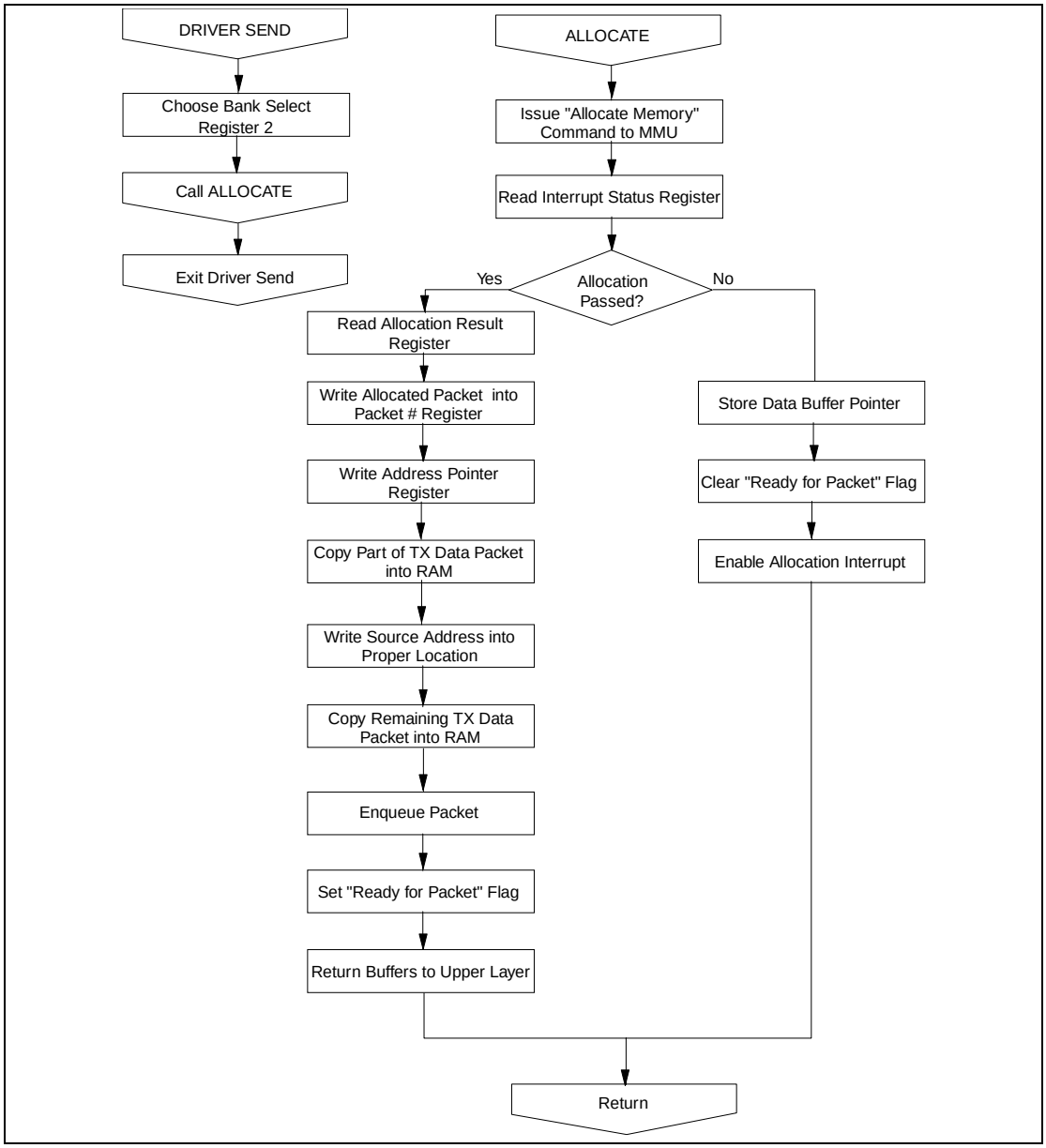


FIGURE 17 – DRIVER SEND AND ALLOCATE ROUTINES

MEMORY PARTITIONING

Unlike other controllers, the LAN91C96I does not require a fixed memory partitioning between transmit and receive resources. The MMU allocates and de-allocates memory upon different events. An additional mechanism allows the CPU to prevent the receive process from starving the transmit memory allocation.

Memory is always requested by the side that needs to write into it, that is: The CPU for transmit or the CSMA/CD for receive. The CPU can control the number of bytes it requests for transmit but it cannot determine the number of bytes the receive process is going to demand. Furthermore, the receive process requests will be dependent on network traffic, in particular on the arrival of broadcast and multicast packets that might not be for the node, and that are not subject to upper layer software flow control.

In order to prevent unwanted traffic from using too much memory, the CPU can program a "memory reserved for transmit" parameter. If the free memory falls below the "memory reserved for transmit" value, MMU requests from the CSMA/CD block will fail and the packets will overrun and be ignored. Whenever enough memory is released, packets can be received again. If the reserved value is too large, the node might lose data which is an abnormal condition. If the value is kept at zero, memory allocation is handled on first-come first-served basis for the entire memory capacity.

Note that with the memory management built into the LAN91C96I, the CPU can dynamically program this parameter. For instance, when the driver does not need to enqueue transmissions, it can allow more memory to be allocated for receive (by reducing the value of the reserved memory). Whenever the driver needs to burst transmissions it can reduce the receive memory allocation. The driver program the parameter as a function of the following variables:

1) Free memory (read only register)
2) Memory size (read only register)

The reserved memory value can be changed on the fly. If the MEMORY RESERVED FOR TX value is increased above the FREE MEMORY, receive packets in progress are still received, but no new packets are accepted until the FREE MEMORY increases above the MEMORY RESERVED value.

INTERRUPT GENERATION

The interrupt strategy for the transmit and receive processes is such that it does not represent the bottleneck in the transmit and receive queue management between the software driver and the controller. For that purpose there is no register reading necessary before the next element in the queue (namely transmit or receive packet) can be handled by the controller. The transmit and receive results are placed in memory.

The receive interrupt will be generated when the receive queue (FIFO of packets) is not empty and receive interrupts are enabled. This allows the interrupt service routine to process many receive packets without exiting, or one at a time if the ISR just returns after processing and removing one.

There are two types of transmit interrupt strategies:

1) One interrupt per packet.
2) One interrupt per sequence of packets.

The strategy is determined by how the transmit interrupt bits and the AUTO RELEASE bit are used.

TX INT bit - Set whenever the TX completion FIFO is not empty.

TX EMPTY INT bit - Set whenever the TX FIFO is empty.

AUTO RELEASE - When set, successful transmit packets are not written into completion FIFO, and their memory is released automatically.

1) One interrupt per packet: enable TX INT, set AUTO RELEASE=0. The software driver can find the completion result in memory and process the interrupt one packet at a time. Depending on the completion code the driver will take different actions. Note that the transmit process is working in parallel and other transmissions might be taking place. The LAN91C96I is virtually queuing the packet numbers and their status words.

In this case, the transmit interrupt service routine can find the next packet number to be serviced by reading the TX DONE PACKET NUMBER at the FIFO PORTS register. This eliminates the need for the driver to keep a list of packet numbers being transmitted. The numbers are queued by the LAN91C96I and provided back to the CPU as their transmission completes.

2) One interrupt per sequence of packets: Enable TX EMPTY INT and TX INT, set AUTO RELEASE=1. TX EMPTY INT is generated only after transmitting the last packet in the FIFO. TX INT will be set on a fatal transmit error allowing the CPU to know that the transmit process has stopped and therefore the FIFO will not be emptied.

This mode has the advantage of a smaller CPU overhead, and faster memory de-allocation. Note that when AUTO RELEASE=1 the CPU is not provided with the packet numbers that completed successfully.

Note: The pointer register is shared by any process accessing the LAN91C96I memory. In order to allow processes to be interruptible, the interrupting process is responsible for reading the pointer value before modifying it, saving it, and restoring it before returning from the interrupt.

Typically there would be three processes using the pointer:

1) Transmit loading (sometimes interrupt driven)
2) Receive unloading (interrupt driven)
3) Transmit Status reading (interrupt driven).

1) and 3) also share the usage of the Packet Number Register. Therefore saving and restoring the PNR is also required from interrupt service routines.

POWER DOWN

The LAN91C96I can enter power down mode by means of the PWRDWN pin (pin 68) or the PWRDN bit (Control Register, bit 13). The power down current is 8 mA. When in power down mode, the LAN91C96I will:

- Stop the crystal oscillator
- Tristate: Data Bus
  Interrupts(only by PWRDN bit)
  nIOCS16
  10BASE-T and AUI outputs
  Turn off analog bias currents
- Drive the EEPROM and ROM outputs inactive
- Preserve contents of registers and memory

The PWRDWN pin is internally gated with the RESET (RESET pin before de-glitching) and with the SRESET bit (COR bit 7). This gating function internally negates power down whenever RESET is high or SRESET is high to allow the oscillator to run during RESET. Except for this gating function, all other uses of the RESET pin use a de-glitched version of the signal as defined in the pin description section.

nXENDEC PIN	PWRDN PIN	PWRDN BIT	
0	X	0	Normal external ENDEC operation
1	0	0	Normal internal ENDEC operation
1	1	0	Powerdown - Normal mode restored by PWRDWN pin going low
X	X	1	Powerdown - Bit is cleared by a write access to any LAN91C96I register or by hardware reset

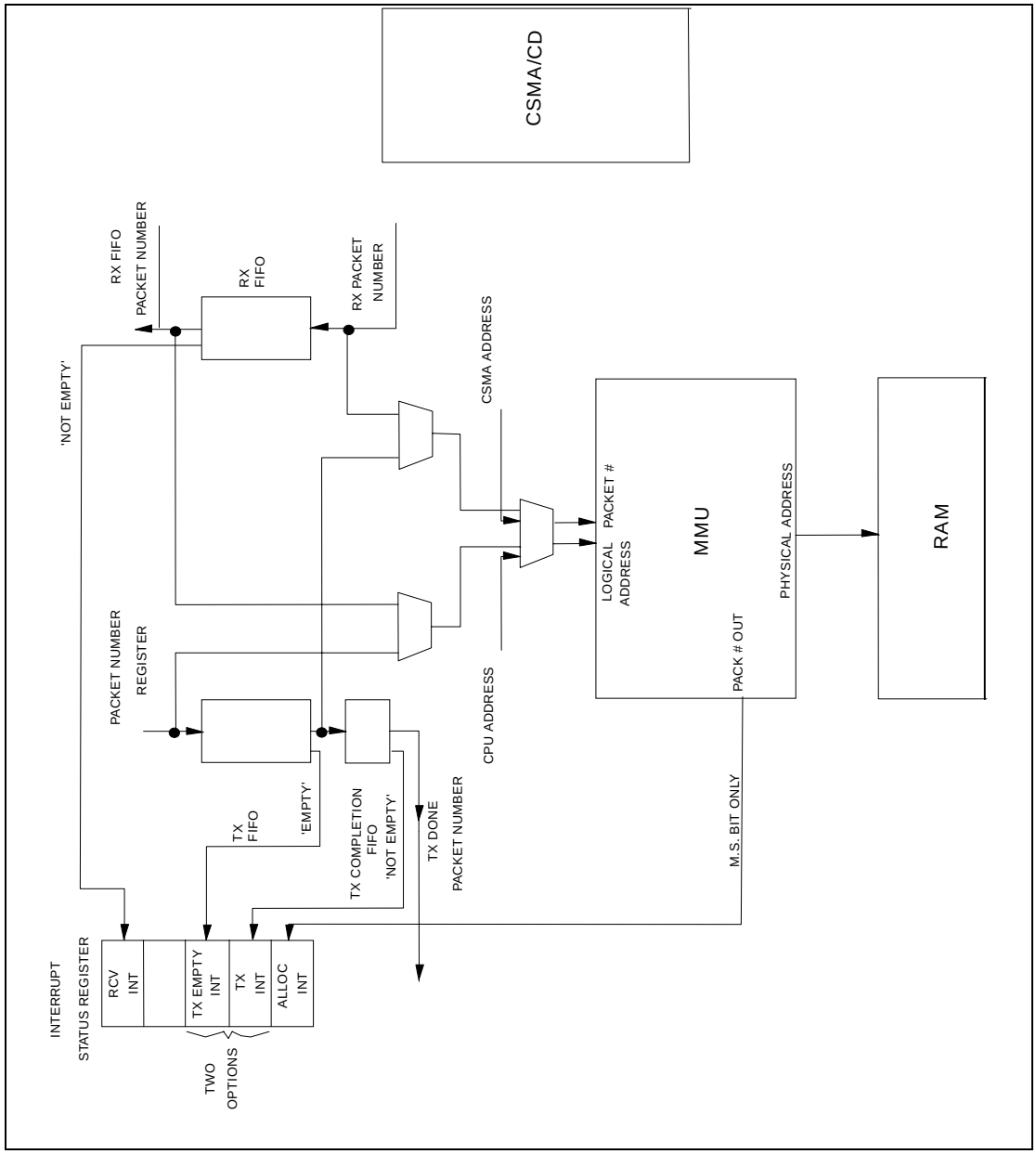


FIGURE 18 - INTERRUPT GENERATION FOR TRANSMIT; RECEIVE, MMU

FUNCTIONAL DESCRIPTION OF THE BLOCKS

MEMORY MANAGEMENT UNIT

The MMU interfaces the on-chip RAM on one side and the arbiter on the other for address and data flow purposes. For allocation and de-allocation, it interfaces the arbiter only.

The MMU deals with a single ported memory and is not aware of the fact that there are two entities requesting allocation and actually accessing memory. The mapping function done by the MMU is only a function of the packet number accessed and of the offset within that packet being accessed. It is not a function of who is requesting the access or the direction of the access.

To accomplish that, memory accesses as well as MMU allocation and de-allocation requests are arbitrated by the arbiter block before reaching the MMU.

Memory allocation could take some time, but the ALLOC INT bit in Interrupt Status Register is negated immediately upon allocation request, allowing the system to poll that register at any time. Memory de-allocation command completion indication is provided via the BUSY bit, readable through the MMU command register.

The mapping and queuing functions of the MMU rely on the uniqueness of the packet number assigned to the requester. For that purpose the packet number assignment is centralized at the MMU, and a number will not be reused until the memory associated with it is released. It is clear that a packet number should not be released while the number is in the TX or RX packet queue.

The TX and RCV FIFOs are deep enough to handle the total number of packets the MMU can allocate, therefore there is no need for the programmer or the hardware to check FIFO full conditions.

ARBITER

The function of the arbiter is to sequence packet RAM accesses as well as MMU requests in such a way that the on-chip single ported RAM and a single MMU can be shared by two parties. One party is the host CPU and the other party is the CSMA/CD block.

The arbiter is address transparent, namely, any address can be accessed at any time. In order to exploit the sequential nature of the access, and minimize the access time on the system side, the CPU cycle is buffered by the Data Register rather than go directly to and from memory. Whenever a write cycle is performed, the data is written into the Data Register and will be written into memory as a result of that operation, allowing the CPU cycle to complete before the arbitration and memory cycle are complete. Whenever a read cycle is performed, the data is provided immediately from the Data Register, without having to arbitrate and complete a memory cycle. The present cycle results in an arbitration request for the next data location. Loading the pointer causes a similar pre-fetch request.

This type of read-ahead and write-behind arbitration allows the controller to have a very fast access time, and would work without wait states for as long as the cycle time specification is satisfied. The values are 40 ns access time, and 185ns cycle time.

By the same token, CSMA/CD cycles might be postponed. The worst case CSMA/CD latency for arbiter service is one memory cycle. The arbiter uses the pointer register as the CPU provided address, and the internal DMA address from the CSMA/CD side as the addresses to be provided to the MMU.

The data path routed by the arbiter goes between memory (the data path does not go through the MMU) on one side and either the CPU side bus or the data path of the CSMA/CD core.

The data path between memory and the Data Register is in fact buffered by a small FIFO in each direction. The FIFOs beneath the Data Register can be read and written as bytes or words, in any sequential combination. The presence of these FIFOs makes sure that word transfers are possible on the system bus even if the address loaded into the pointer is odd.

BUS INTERFACE

The bus interface handles the data, address and control interfaces and is compliant with the ISA.

The functions in this block include address decoding for I/O and ROM memory (including address relocation support) for ISA, data path routing, sequential memory address support, optional wait state generation, boot ROM support, EEPROM setup function, bus transceiver control, and interrupt generation / selection.

For ISA, I/O address decoding is done by comparing A15-A4 to the I/O BASE address determined in part by the upper byte of the BASE ADDRESS REGISTER, and also requiring that AEN be low. If the above address comparison is satisfied and the LAN91C96I is in 16 bit mode, nIOCS16 will be asserted (low).

A valid comparison does not yet indicate a valid I/O cycle is in progress, as the addresses could be used for a memory cycle, or could even glitch through a valid value. For ISA, only when nIORD or nIOWR are activated the I/O cycle begins.

WAIT STATE POLICY

The LAN91C96I can work on most system buses without having to add wait states. The two parameters that determine the memory access profile are the read access time and the cycle time into the Data Register.

The read access time is 40ns and the cycle time is 185ns. If any one of them does not satisfy the application requirements, wait states should be added.

If the access time is the problem, IOCHRDY should be negated for all accesses to the LAN91C96I. This can be achieved by programming the NO WAIT ST bit in the configuration register to “0”. The LAN91C96I will negate IOCHRDY for 100ns to 150ns on every access to any register.

If the cycle time is the problem, programming NO WAIT ST as described before will solve it but at the expense of slowing down all accesses. The alternative is to let the LAN91C96I negate IOCHRDY only when the Data Register FIFOs require so. Namely, if NO WAIT ST is set, IOCHRDY will only be negated if a Data Register read cycle starts and there is less than a full word in the read FIFO, or if a write cycle starts and there is more than two bytes in the write FIFO.

The cycle time is defined as the time between leading edges of read from the Data Register, or equivalently between trailing edges of write to the Data Register. For example, in an ISA system the cycle time of a 16 bit transfer will be at least 2 clocks for the I/O access to the LAN91C96I (+ one clock for the memory cycle) for a total of 3 clocks. In absolute time it means 375ns for an 8MHz bus, and 240ns for a 12.5 MHz bus.

The cycle time will not increase when configured for full duplex mode, because the CSMA/CD memory arbitration requests are sequenced by the DMA logic and never overlap.

ARBITRATION CONSIDERATIONS

The arbiter exploits the sequential nature of the CPU accesses to provide a very fast access time. Memory bandwidth considerations will have an effect on the CPU cycle time but no effect on access time.

For normal 8MHz, 10MHz, and 12.5MHz ISA buses, as well as EISA normal cycles, the LAN91C96I can be accessed without negating ready.

When write operations occur, the data is written into a FIFO. The CPU cycle can complete immediately, and the buffered data will be written into memory later. The memory arbitration request is generated as a function of that FIFO being not empty. The nature of the cycle requested (byte/word) is determined by the LSB of the pointer and the number of bytes in the FIFO.

When read operations occur, words are pre-fetched upon pointer loading in order to have at least a word ready in the FIFO to be read. New pre-fetch cycles are requested as a function of the number of bytes in the FIFO.

For example, if an odd pointer value is loaded, first a byte is pre-fetched into the FIFO, and immediately a full word is pre-fetched completing three bytes into the FIFO. If the CPU reads a word, one byte will be left again a new word is pre-fetched.

In the case of write, if an odd pointer value is loaded, and a full word is written, the FIFO holds two bytes, the first of which is immediately written into an odd memory location. If by that time another byte or word was written, there will be two or three bytes in the FIFO and a full word can be written into the now even memory address.

When a CSMA/CD cycle begins, the arbiter will route the CSMA/CD DMA addresses to the MMU as well as the packet number associated with the operation in progress. In full-duplex mode, receive and transmit requests are alternated in such a way that the CPU arbitration cycle time is not affected.

DMA BLOCK

The DMA block resides between the CSMA/CD block and the arbiter. It can interface both the data path and the control path of the CSMA/CD block for different operations.

Its functions include the following:

- Start transmission process into the CSMA/CD block.
- Generate CSMA/CD side addresses for accessing memory during transmit and receive operations.
- Generate MMU memory requests and verify success.
- Compute byte count and write it in first locations of receive packet.
- Write transmit status word in first locations of transmit packet.
- Determine if enough memory is available for reception.
- De-allocate transmit memory after suitable completion.
- De-allocate receive memory upon error conditions.
- Initiate retransmissions upon collisions (if less than 16 retries).
- Terminate reception and release memory if packet is too long.

The specific nature of each operation and its trigger event are:

1) TX operations will begin if TXENA is set and TX FIFO is not empty. The DMA logic does not need to use the TX PACKET NUMBER, it goes directly from the FIFO to the MMU. However the DMA logic controls the removal of the PACKET NUMBER from the FIFO.
2) Generation of CSMA/CD side addresses into memory: Independent 11-bit counters are kept for transmit and receive in order to allow full-duplex operation.
3) MMU requests for allocation are generated by the DMA logic upon reception. The initial allocation request is issued when the CSMA block indicates an active reception. If allocation succeeds, the DMA block stores the packet number assigned to it, and generates write arbitration requests for as long as the CSMA/CD FIFO is not empty. In parallel the CSMA/CD completes the address filtering and notifies the DMA of an address match. If there is no address match, the DMA logic will release the allocated memory and stop reception.
4) When the CSMA/CD block notifies the DMA logic that a receive packet was completed, if the CRC is OK, the DMA will either write the previously stored packet number into the RX PACKET NUMBER FIFO (to be processed by the CPU), or if the CRC is bad the DMA will just issue a release command to the MMU (and the CPU will never see that packet).
   Packets with bad CRC can be received if the RCV_BAD bit in the configuration register is set.
5) If AUTO_RELEASE is set, a release is issued by the DMA block to the MMU after a successful transmission (TX_SUCC set), and the TX completion FIFO is clocked together with the TX FIFO preventing the packet number from moving into the TX completion FIFO.
6) Based on the RX counter value, if a receive packet exceeds 1532 bytes, reception is stopped by the DMA and the RX ABORT bit in the Receive Control Register is set. The memory allocated to the packet is automatically released.
7) If an allocation fails, the CSMA/CD block will activate RX_OVRN INT upon detecting a FIFO full condition. RXEN will stay active to allow reception of subsequent packets if memory becomes available. The CSMA/CD block will flush the FIFO upon the new frame arrival.

PACKET NUMBER FIFOS

The transmit packet FIFO stores the packet numbers awaiting transmission, in the order they were enqueued. The FIFO is advanced (written) when the CPU issues the "enqueue packet number command", the packet number to be written is provided by the CPU via the Packet Number Register. The number was previously obtained by requesting memory allocation from the MMU. The FIFO is read by the DMA block when the CSMA/CD block is ready to proceed on to the next transmission. By reading the TX EMPTY INT bit the CPU can determine if this FIFO is empty.

The transmit completion FIFO stores the packet numbers that were already transmitted but not yet acknowledged by the CPU. The CPU can read the next packet number in this FIFO from the FIFO Ports Register. The CPU can remove a packet number from this FIFO by issuing a TX INT acknowledge. The CPU can determine if this FIFO is empty by reading the TX INT bit or the FIFO Ports Register.

The receive packet FIFO stores the packet numbers already received into memory, in the order they were received. The FIFO is advanced (written) by the DMA block upon reception of a complete valid packet into memory. The number is determined the moment the DMA block first requests memory from the MMU for that packet. The first receive packet number in the FIFO can be read via the FIFO Ports Register, and the data associated with it can be accessed through the receive area. The packet number can be removed from the FIFO with or without an automatic release of its associated memory.

The FIFO is read out upon CPU command (remove packet from top of RX FIFO, or remove and release command) after processing the receive packet in the receive area.

The width of each FIFO is 5 bits per packet number. The depth of each FIFO equals the number of packets the LAN91C96I can handle (18).

The guideline is software transparency; the software driver should not be aware of different devices or FIFO depths. If the MMU memory allocation succeeded, there will be room in the transmit FIFO for enqueuing the packet. Conversely if there is free memory for receive, there should be room in the receive FIFO for storing the packet number.

Note that the CPU can enqueue a transmit command with a packet number that does not follow the sequence in which the MMU assigned packet numbers. For example, when a transmission failed and it is retried in software, or when a receive packet is modified and sent back to the network.

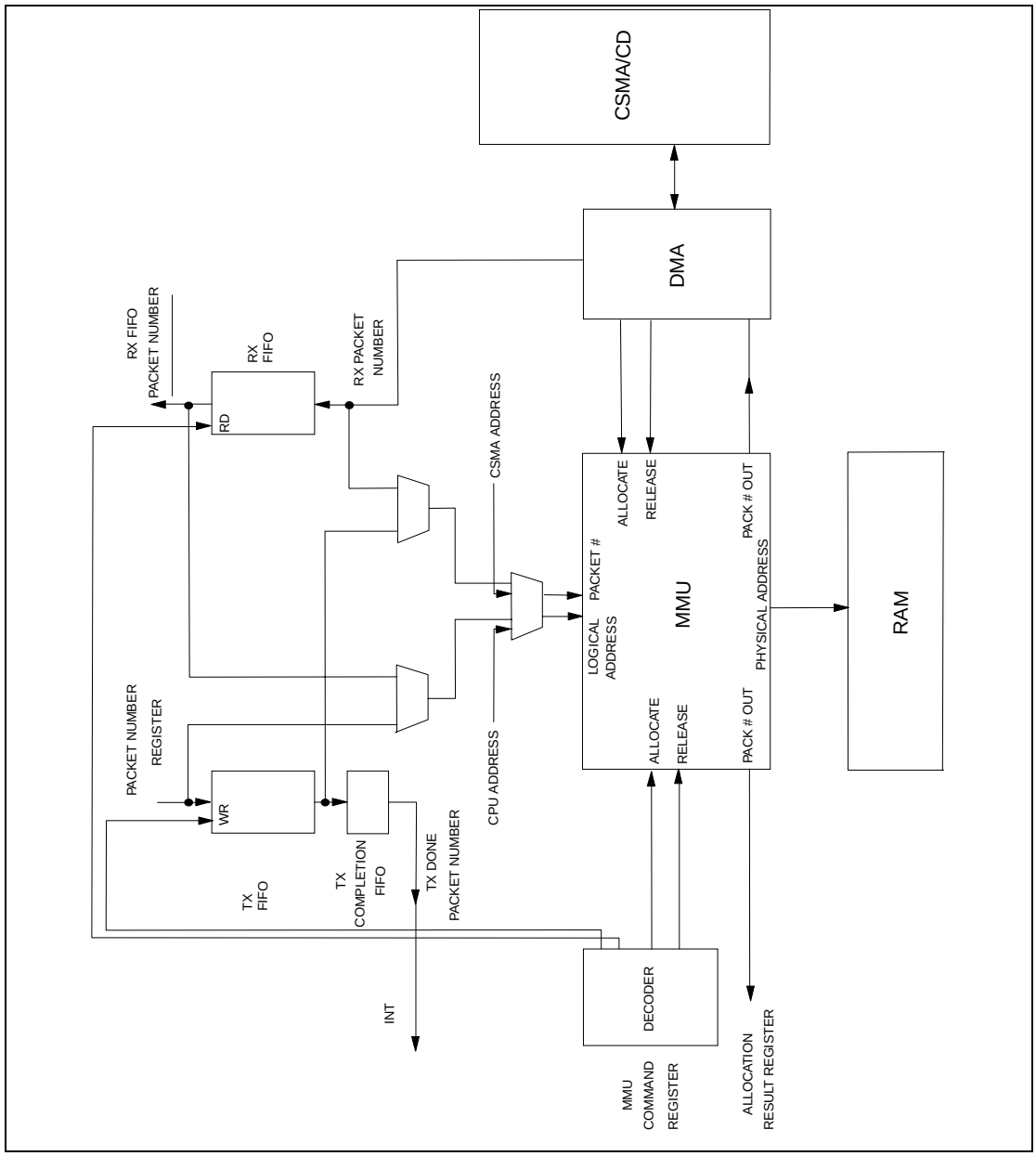


FIGURE 19 - MMU PACKET NUMBER FLOW AND RELEVANT REGISTERS

CSMA BOCK

The CSMA/CD block is first interfaced via its control registers in order to define its operational configuration. From then on, the DMA interface between the CSMA/CD block and memory is used to transfer data to and from its data path interface.

For transmit, the CSMA/CD block will be asked to transmit frames as soon as they are ready in memory. It will continue transmissions until any of the following transmit error occurs:

1) Collisions on same frame
2) Late collision
3) Lost Carrier sense and MON_CSN set
4) Transmit Underrun
5) SQET error and STP_SQET set

In that case TXENA will be cleared and the CPU should restart the transmission by setting it again. If a transmission is successful, TXENA stays set and the CSMA/CD is provided by the DMA block with the next packet to be transmitted.

For receive, the CPU sets RXEN as a way of starting the CSMA/CD block receive process. The CSMA/CD block will send data after address filtering through the data path to the DMA block. Data is transferred into memory as it is received, and the final check on data acceptance is the CRC checking done by the CSMA/CD block. In any case, the DMA takes care of requesting/releasing memory for receive packets, as well as generating the byte count.

The receive status word is provided by the CSMA/CD block and written in the first location of the receive structure by the DMA block. If configured for storing CRC in memory, the CSMA/CD unit will transfer the CRC bytes through the DMA interface, and then will be treated like regular data bytes.
Note that the receive status word of any packet is available only through memory and is not readable through any other register. In order to let the CPU know about receive overruns, the RX_OVRN INT is set and latched in the Interrupt Status Register, which is readable by the CPU at any time.

The address filtering is done inside the CSMA/CD block. A packet will be received if the destination address is broadcast, or if it is addressed to the individual address of the LAN91C96I, or if it is a multicast address and ALMUL bit is set, or if it is a multicast address matching one of the multicast table entries. If the PRMS bit is set, all packets are received.

The CSMA/CD block is a full duplex machine, and when working in full duplex mode, the CSMA/CD block will be simultaneously using its data path transmit and receive interfaces.

Statistical counters are kept by the CSMA/CD block, and are readable through the appropriate register. The counters are four bits each, and can generate an interrupt when reaching their maximum values. Software can use that interrupt to update statistics in memory, or it can keep the counter interrupt disabled, while relying on the transmit interrupt routine reading the counters. Given that the counters can increment only once per transmit, this technique is a good complement for the single interrupt per sequence strategy.

The interface between the CSMA/CD block and memory is word oriented. Two bi-directional FIFOs make the data path interface.

Whenever a normal collision occurs (less than 16 retries), the CSMA/CD will trigger the backoff logic and will indicate the DMA logic of the collision. The DMA is responsible for restarting the data transfer into the CSMA/CD block regardless of whether the collision happened on the preamble or not.

Only when 16 retries are reached, the CSMA/CD block will clear the TXENA bit, and CPU intervention is required. The DMA will not automatically restart data transfer in this case, nor will it transmit the next enqueued packet until TXENA is set by the CPU. The DMA will move the packet number in question from the TX FIFO into the TX completion FIFO.

NETWORK INTERFACE

The LAN91C96I includes both an AUI interface for thick and thin coax applications and a 10BASE-T interface for twisted pair applications. Functions common to both are:

1) Manchester encoder/decoder to convert NRZ data to Manchester encoded data and back.
2) A 32ms jabber timer to prevent inadvertently long transmissions. When 'jabbing' occurs, the transmitter is disabled, automatic loopback is disabled (in 10BASE-T mode), and a collision indication is given to the controller. The interface 'unjabs' when the transmitter has been idle for a minimum of 256 ms.
3) A phase-lock loop to recover data and clock from the Manchester data stream with up to plus or minus 18ns of jitter.

4) Diagnostic loopback capability.
5) LED drivers for collision, transmission, reception, and jabber.

10BASE-T

The 10BASE-T interface conforms to the twisted pair MAU addendum to the 802.3 specification. On the transmission side, it converts the NRZ data from the controller to Manchester data and provides the appropriate signal level for driving the media. Signal are predistorted before transmission to minimize ISI. The collision detection circuitry monitors the simultaneous occurrence of received signals and transmitted data on the media. During transmission, data is automatically looped back to the receiver except during collision periods, in which case the input to the receiver is network data. During collisions, should the receive input go idle prior to the transmitter going idle, input to the receiver switches back to the transmitter within nine bit times. Following transmission, the transmitter performs a SQE test. This test exercises the collision detection circuitry within the 10BASE-T interface.

The receiver monitors the media at all times. It recovers the clock and data and passes it along to the controller. In the absence of any receive activity, the transmitter is looped back to the receiver. In addition, the receiver performs automatic polarity correction. The 10BASE-T interface performs link integrity tests per section 14.2.1.7 of 802.3, using the following values:

1) Link_loss_timer: 64 ms
2) Link_test_min_timer: 4 ms
3) Link_count: 2
4) Link_test_max_timer: 64 ms

The state of the link is reflected in the EPHSR.

AUI

The LAN91C96I also provides a standard six wire AUI interface to a coax transceiver.

PHYSICAL INTERFACE

The internal physical interface (PHY) consists of an encoder/decoder (ENDEC) and an internal 10BASE-T transceiver. The ENDEC also provides a standard 6-pin AUI interface to an external coax transceiver for 10BASE-2 and 10BASE-5 applications. The internal signals between MAC and the PHY can be routed to pins by asserting the nXENDEC pin low. This feature allows the interface to an external ENDEC and transceiver. The PHY functions can be divided into transmit and receive functions.

TRANSMIT FUNCTIONS

Manchester Encoding

The PHY encodes the transmit data received from the MAC. The encoded data is directed internally to the selected output driver for transmission over the twisted-pair network or the AUI cable. Data transmission and encoding is initiated by the Transmit Enable input, TXE, going low.

Transmit Drivers

The encoded transmit data passes through to the transmit driver pair, TPETXP(N), and its complement, TPETXDP(N). Each output of the transmit driver pair has a source resistance of 10 ohms maximum and a current rating of 25 mA maximum. The degree of predistortion is determined by the termination resistors; the equivalent resistance should be 100 ohms.

Jabber Function

This integrated function prevents the DTE from locking into a continuous transmit state. In 10BASE-T mode, if transmission continues beyond the specified time limit, the jabber function inhibits further transmission and asserts the collision indicator nCOLL. The limits for jabber transmission are 20 to 15 ms in 10BASE-T mode. In the AUI mode, the jabber function is performed by the external transceiver.

SQE Function

In the 10BASE-T mode, the PHY supports the signal quality error (SQE) function. At the end of a transmission, the PHY asserts the nCOLL signal for 10+/-5 bit times beginning 0.6 to 1.6ms after the last positive transition of a transmitted frame. In the AUI mode, the SQE function is performed by the external transceiver.

RECEIVE FUNCTIONS

Receive Drivers

Differential signals received off the twisted-pair network or AUI cable are directed to the internal clock recovery circuit prior to being decoded for the MAC.

Manchester Decoder and Clock Recovery

The PHY performs timing recovery and Manchester decoding of incoming differential signals in 10BASE-T or AUI modes, with its built-in phase-lock loop (PLL). The decoded (NRZ) data, RXD, and the recovered clock, RXCLK, becomes available to the MAC, typically within 9 bit times (5 for AUI) after the assertion of nCRS. The receive clock, RXCLK, is phase-locked to the transmit clock in the absence of a received signal (idle).

Squelch Function

The integrated smart squelch circuit employs a combination of amplitude and timing measurements to determine the validity of data received off the network. It prevents noise at the differential inputs from falsely triggering the decoder in the absence of valid data or link test pulses. Signal levels below 300mV (180mV for AUI) or pulse widths less than 15ns at the differential inputs are rejected. Signals above 585mV (300mV for AUI) and pulse widths greater than 30ns will be accepted. When using the extended cable mode with 10BASE-T media which extends beyond the standard limit of 100 meters, the squelch level can optionally be set to reject signals below 180mV and accept signals above 300mV. If the input signal exceeds the squelch requirements, the carrier sense output, nCRS, is asserted.

Reverse Polarity Function

In the 10BASE-T mode, the PHY monitors for receiver polarity reversal due to crossed wires and corrects by reversing the signal internally.

Collision Detection Function

In the 10BASE-T mode, a collision state is indicated when there are simultaneous transmissions and receptions on the twisted pair link. During a collision state, the nCOLL signal is asserted. If the received data ends and the transmit control signal is still active, the transmit data is sent to the MAC within 9 bit times. The nCOLL signal is de-asserted within 9 bit times after the collision terminates. In the AUI mode, the external transceiver sends a 10MHz signal to the PHY upon detection of a collision.

Link Integrity

The PHY test for a faulty twisted-pair link. In the absence of transmit data, link test pulses are transmitted every 16+/-8ms after the end of the last transmission or link pulse on the twisted pair medium. If neither valid data nor link test pulses are received within 10 to 150ms, the link is declared bad and both data transmission as well as the operational loopback function are disabled. The Link Integrity function can be disabled for pre-10BASE-T twisted-pair networks.

BOARD SETUP INFORMATION

The following parameters are obtained from the EEPROM as board setup information:

ETHERNET INDIVIDUAL ADDRESS
I/O BASE ADDRESS
ROM BASE ADDRESS
8/16 BIT ADAPTER
10BASE-T or AUI INTERFACE
INTERRUPT LINE SELECTION

REGISTER	EEPROM WORD ADDRESS
Configuration Register	IOS Value * 4
Base Register	(IOS Value *4) + 1

All the above mentioned values are read from the EEPROM upon hardware reset. Except for the INDIVIDUAL ADDRESS, the value of the IOS switches determines the offset within the EEPROM for these parameters, in such a way that many identical boards can be plugged into the same system by just changing the IOS jumpers.

In order to support a software utility based installation, even if the EEPROM was never programmed, the EEPROM can be written using the LAN91C96I. One of the IOS combination is associated with a fixed default value for the key parameters (I/O BASE, ROM BASE, INTERRUPT) that can always be used regardless of the EEPROM based value being programmed. This value will be used if all IOS pins are left open or pulled high.

The EEPROM is arranged as a 64 x 16 array. The specific target device is the 9346 1024-bit Serial EEPROM. All EEPROM accesses are done in words. All EEPROM addresses shown are specified as word addresses.

INDIVIDUAL ADDRESS 20-22 hex
If IOS2-0 = 7, only the INDIVIDUAL ADDRESS is read from the EEPROM. Currently assigned values are assumed for the other registers. These values are default if the EEPROM read operation follows hardware reset.

The EEPROM SELECT bit is used to determine the type of EEPROM operation: a) normal or b) general purpose register.

a) NORMAL EEPROM OPERATION - EEPROM SELECT bit = 0

On EEPROM read operations (after reset or after setting RELOAD high) the CONFIGURATION REGISTER and BASE REGISTER are updated with the EEPROM values at locations defined by the IOS2-0 pins. The INDIVIDUAL ADDRESS registers are updated with the values stored in the INDIVIDUAL ADDRESS area of the EEPROM.

On EEPROM write operations (after setting the STORE bit) the values of the CONFIGURATION REGISTER and BASE REGISTER are written in the EEPROM locations defined by the IOS2-0 pins.

The three least significant bits of the CONTROL REGISTER (EEPROM SELECT, RELOAD and STORE) are used to control the EEPROM. Their values are not stored nor loaded from the EEPROM.

b) GENERAL PURPOSE REGISTER - EEPROM SELECT bit = 1

On EEPROM read operations (after setting RELOAD high) the EEPROM word address defined by the POINTER REGISTER 6 least significant bits is read into the GENERAL PURPOSE REGISTER.

On EEPROM write operations (after setting the STORE bit) the value of the GENERAL PURPOSE REGISTER is written at the EEPROM word address defined by the POINTER REGISTER 6 least significant bits.

RELOAD and STORE are set by the user to initiate read and write operations respectively. Polling the value until read low is used to determine completion. When an EEPROM access is in progress the STORE and RELOAD bits of CTR will read-back as both bits high. No other bits of the LAN91C96I can be read or written until the EEPROM operation completes and both bits are clear. This mechanism is also valid for reset initiated reloads.

Note: If no EEPROM is connected to the LAN91C96I, the ENEEP pin should be grounded and no accesses to the EEPROM will be attempted. Configuration, Base and Individual Addresses assume their default values upon hardware reset and the CPU is responsible for programming them for their final value.

DIAGNOSTIC LEDs

The following LED drive signals are available for diagnostic and installation aid purposes:

nTXLED - Activated by transmit activity.

nBSELED - Board select LED. Activated when the board space is accessed, namely on accesses to the LAN91C96I register space or the ROM area decoded by the LAN91C96I. The signal is stretched to 125 msec.

nRXLED - Activated by receive activity.

nLINKLED - Reflects the link integrity status.

BUS CLOCK CONSIDERATIONS

The arbiter exploits the sequential nature of the CPU accesses to provide a very fast access time. Memory bandwidth considerations will have an effect on the CPU cycle time but no effect on access time.

For normal 8MHz, 10MHz, and 12.5MHz ISA buses, as well as EISA normal cycles, the LAN91C96I can be accessed without negating ready.

See Arbitration Considerations in Functional Description of the Blocks for more details.

IOS2-0	WORD ADDRESS	16 BITS
000	0h	CONFIGURATION REG.
	1h	BASE REG.
001	4h	CONFIGURATION REG.
	5h	BASE REG.
010	8h	CONFIGURATION REG.
	9h	BASE REG.
011	Ch	CONFIGURATION REG.
	Dh	BASE REG.
100	10h	CONFIGURATION REG.
	11h	BASE REG.
101	14h	CONFIGURATION REG.
	15h	BASE REG.
110	18h	CONFIGURATION REG.
	19h	BASE REG.
XXX	20h	IA0-1
	21h	IA2-3
	22h	IA4-5

FIGURE 20 - 64 X 16 SERIAL EEPROM MAP

OPERATIONAL DESCRIPTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... -40°C to 85°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature Range (soldering, 10 seconds) .....+325°C
Positive Voltage on 3.3V-Only tolerant I/O pin, with respect to Ground ..... V_{CC} + 0.3V
Positive Voltage on 5V tolerant I pin, with respect to ground 5.5V
Negative Voltage on any pin, with respect to Ground ..... -0.3V
Maximum V_{CC} ..... +3.63V

*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS

(T_A =-40°C to °85C, V_{CC} = +3.3 V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.0			V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		165		mV	
I_{CLK} Input Buffer						
Low Input Level	V_{ILCK}			0.3	V	
High Input Level	V_{IHCK}	2.0			V	
Input Leakage (All I and IS buffers except pins with pullups/pulldowns)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = V_{CC}
IP Type Buffers						
Input Current	I_{IL}	-150	-75		µA	V_{IN} = 0
ID Type Buffers						
Input Current	I_{IH}		+75	+150	µA	V_{IN} = V_{CC}
I/O4 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 2 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -1 mA
Output Leakage	I_{LEAK}	-10		+10	µA	V_{IN} = 0 to V_{CC}
I/O24 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 16 mA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
High Output Level	V_{OH}	2.4			V	I_{OH} = -6 mA
Output Leakage	I_{LEAK}	-10		+10	µA	V_{IN} = 0 to V_{CC}
O24 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 12 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6 mA
Output Leakage	I_{LEAK}	-10		+10	µA	V_{IN} = 0 to V_{CC}
O4 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 2 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -1 mA
Output Leakage	I_{LEAK}	-10		+10	µA	V_{IN} = 0 to V_{CC}
OD16 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 8 mA
Output Leakage	I_{LEAK}	-10		+10	µA	V_{IN} = 0 to V_{CC}
O162 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 8 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -1 mA
Output Leakage	I_{LEAK}	-10		+10	µA	V_{IN} = 0 to V_{CC}
OD24 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 12 mA
Output Leakage	I_{LEAK}	-10		+10	µA	V_{IN} = 0 to V_{CC}
Supply Current Active	I_{CC}		40	64	mA	All outputs open.
Supply Current Standby	I_{CSBY}		6		mA	
XTAL2 Output Drive High	*I_{CX2H}*		*-6*		*mA*	*@2.4V*
XTAL2 Output Drive Low	*I_{CX2L}*		*3*		*mA*	*@0.4V*

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{CC} = +3.3V

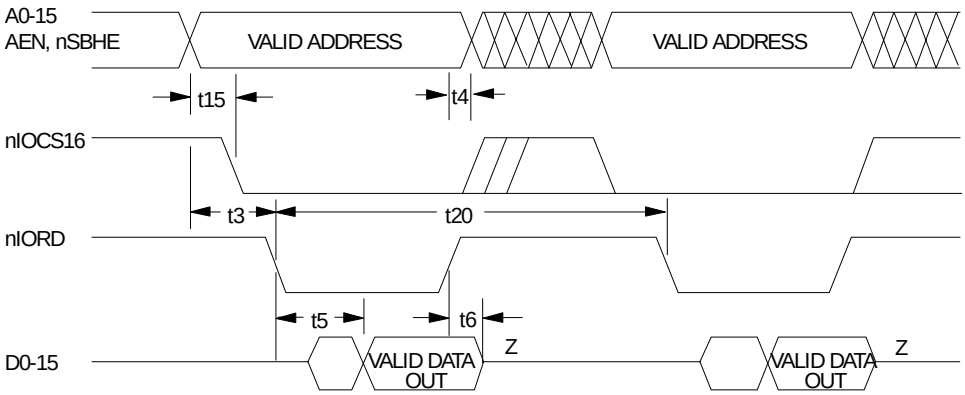
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance (XTAL1)	C_{CIN}		5	6	pF	All pins except pin under test tied to AC ground
Clock Output Capacitance (XTAL2)	C_{COUT}		5	6	pF	
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

V_{CC} = 3.3V +/- 10%

PARAMETER	MIN	TYP	MAX	UNITS
10BASE-T				
Receiver Threshold Voltage		TBD		mV
Receiver Squelch	TBD	TBD	TBD	mV
Receiver Common Mode Range	0		V_{DD}	
Transmitter Output: Voltage Source Resistance	TBD	TBD	TBD	V ohms
Transmitter Output DC Offset			TBD	mV
Transmitter Backswing Voltage to Idle			TBD	mV
Differential Input Voltage	TBD		TBD	V
AUI				
Receiver Threshold Voltage		TBD		mV
Receiver Squelch	TBD	TBD	TBD	mV
Receiver Common Mode Range	0		V_{DD}	
Transmitter Output Voltage (R=78)	TBD	TBD	TBD	V
Transmitter Backswing Voltage to Idle			TBD	mV
Input Differential Voltage	TBD		TBD	V
Output Short Circuit (to V_{CC} or GND) Current			TBD	mA
Differential Idle Voltage (measured 8.0 s after last positive transition of data frame)			TBD	mV

CAPACITIVE LOAD ON OUTPUTS

nIOCS16, IOCHRDY	240 pF
INTR0-3	120 pF
All other outputs	45 pF



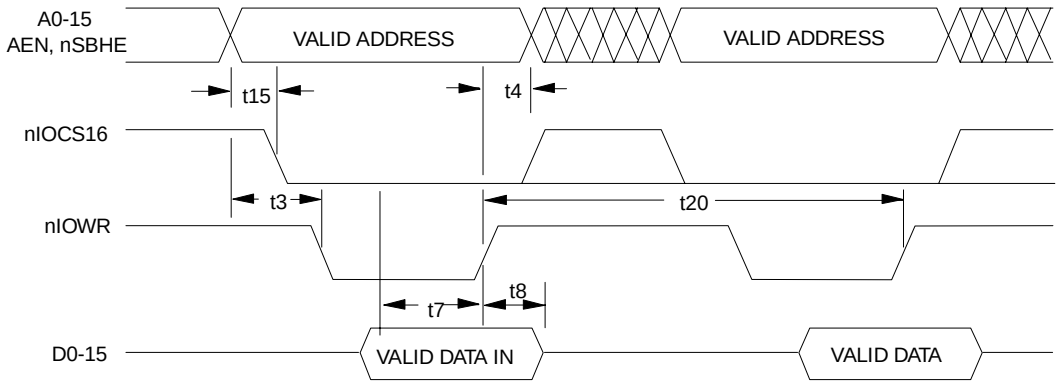
	Parameter	min	typ	max	units
t3	Address, nSBHE, AEN Setup to Control Active	25			ns
t4	Address, nSBHE, AEN Hold after Control Inactive	20			ns
t5	nIORD Low to Valid Data			40	ns
t6	nIORD High to Data Floating			30	ns
t15	A4-A15, AEN Low, BALE High to nIOCS16 Low			25	ns
t20	Cycle time*	185			ns

BALE Tied High

IOCHRDY not used - t20 has to be met

*Note: The cycle time is defined only for consecutive accesses to the Data Register. These values assume that IOCHRDY is not used.

FIGURE 21 - ISA CONSECUTIVE READ CYCLES

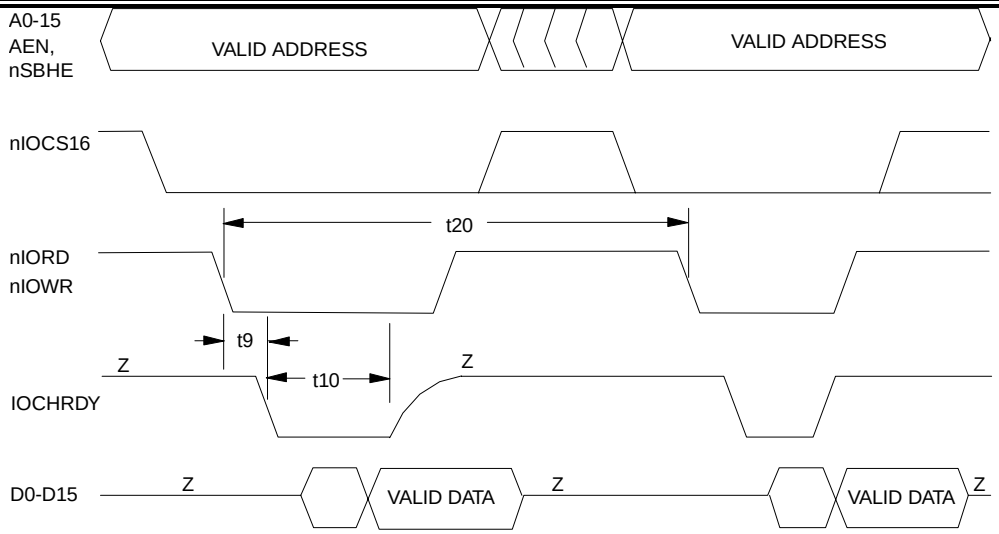


	Parameter	min	typ	max	units
t3	Address, nSBHE, AEN Setup to Control Active	25			ns
t4	Address, nSBHE, AEN Hold after Control Inactive	20			ns
t7	Data Setup to nIOWR Rising	30			ns
t8	Data Hold after nIOWR Rising	9			ns
t15	A4-A15, AEN Low, BALE High to nIOCS16 Low			25	ns
t20	Cycle time*	185			ns

BALE Tied High
IOCHRDY not used - t20 has to be met

*Note: The cycle time is defined only for consecutive accesses to the Data Register. These values assume that IOCHRDY is not used.

FIGURE 22 - ISA CONSECUTIVE WRITE CYCLES



	Parameter	min	typ	max	units
t9	Control Active to IOCHRDY Low			15	ns
t10	IOCHRDY Low Pulse Width*	100		150	ns
t20	Cycle time**	185			ns

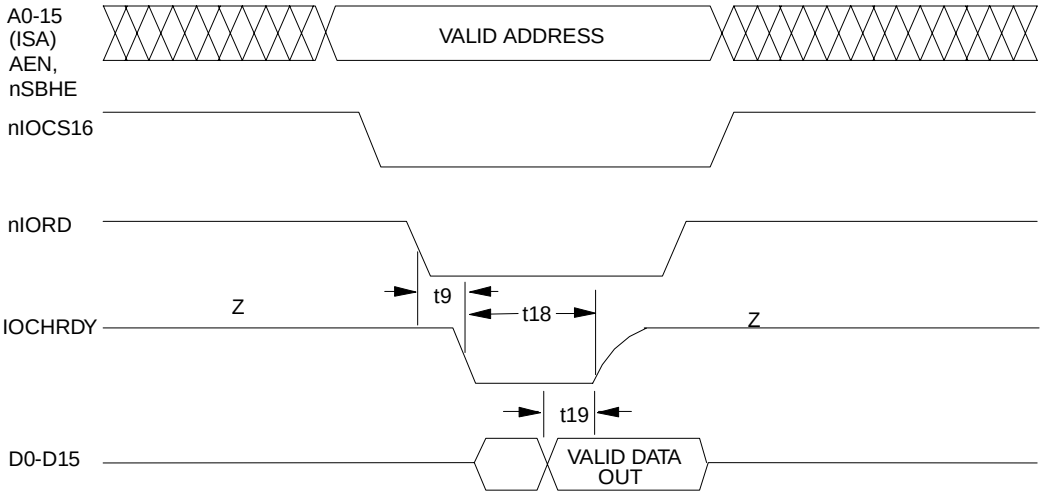
*Note: Assuming NO WAIT ST = 0 in configuration register and cycle time observed.

**Note: The cycle time is defined only for accesses to the Data Register as follows:

For Data Register Read - From nIORD falling to next nIORD falling

For Data Register Write - From nIOWR rising to next nIOWR rising

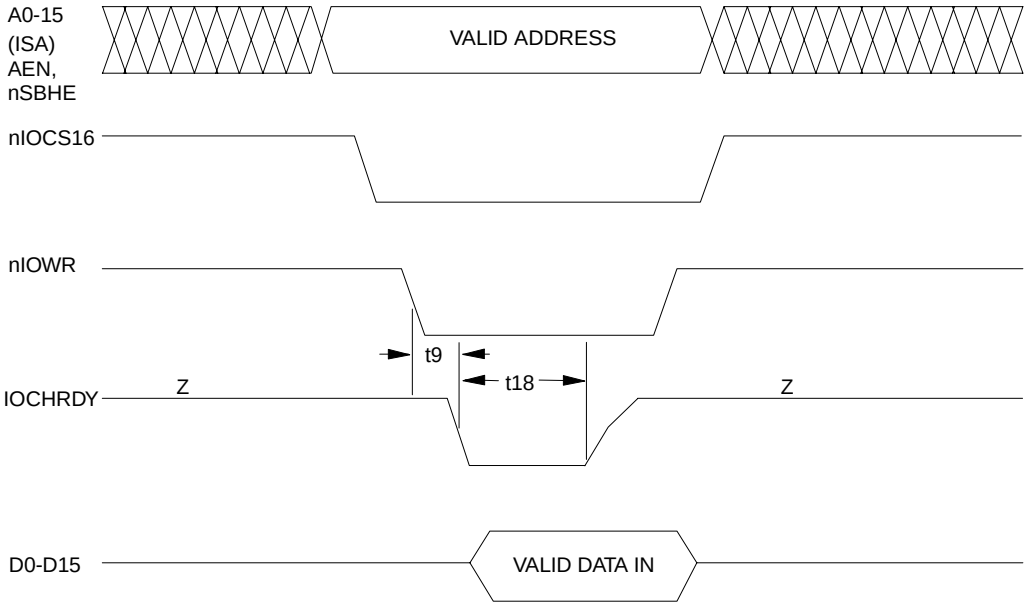
FIGURE 23 - ISA CONSECUTIVE READ AND WRITE CYCLES



	Parameter	min	typ	max	units
t9	Control Active to IOCHRDY Low			15	ns
t18	IOCHRDY Width when Data is Unavailable at Data Register			575	ns
t19	Valid Data to IOCHRDY Inactive			225	ns

IOCHRDY is used instead of meeting t20 and t43.
"No Wait St' bit is 1 - IOCHRDY only negated if needed and only for Data Register access.

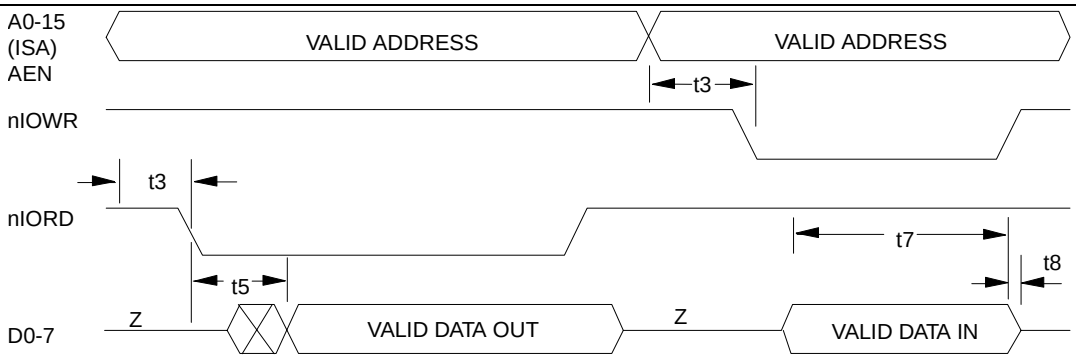
FIGURE 24 - DATA REGISTER SPECIAL READ ACCESS



	Parameter	min	typ	max	units
t9	Control Active to IOCHRDY Low			15	ns
t18	IOCHRDY Width when Data Register is Full			425	ns

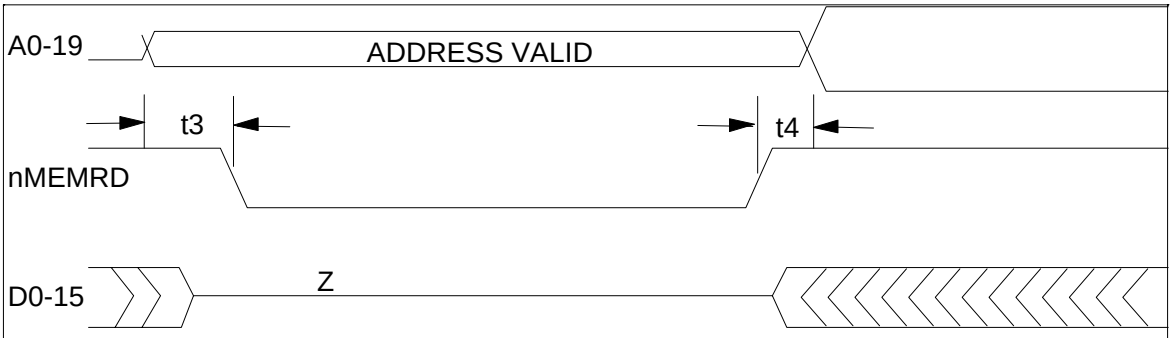
IOCHRDY is used instead of meeting t20 and t44.
'No Wait St' bit is 1 - IOCHRDY only negated if needed and only for Data Register access.

FIGURE 25 - DATA REGISTER SPECIAL WRITE ACCESS



	Parameter	min	typ	max	units
t3	Address, nSBHE, AEN Setup to Control Active	25			ns
t5	nIORD Low to Valid Data			40	ns
t7	Data Setup to nIOWR Rising	30			ns
t8	Data Hold after nIOWR Rising	9			ns

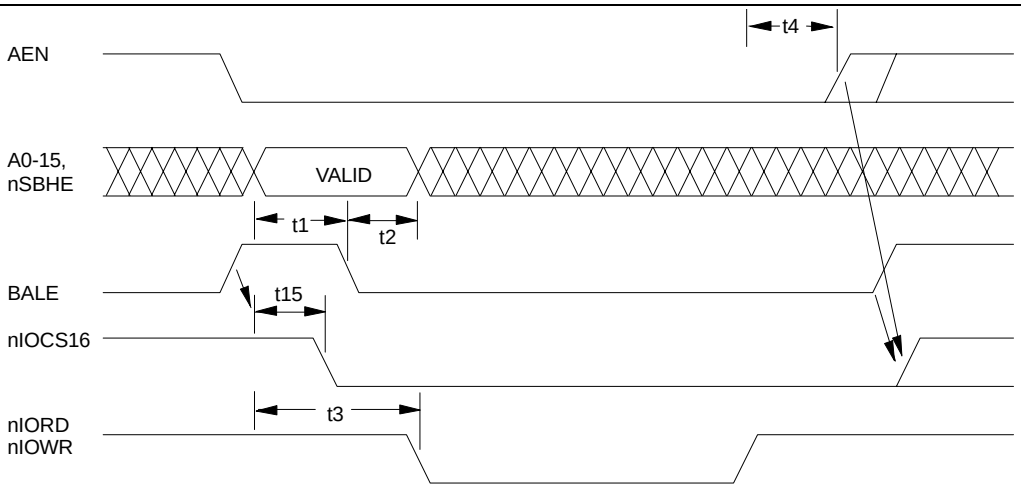
FIGURE 26 - 8-BIT MODE REGISTER CYCLES



	Parameter	min	typ	max	units
t3	Address Setup to Control Active	25			ns
t4	Address Hold after Control Inactive	20			ns
t16	nMEMRD Low to nROM Low	0		25	ns
t17	nMEMRD High to nROM High	0		35	ns

BALE tied high

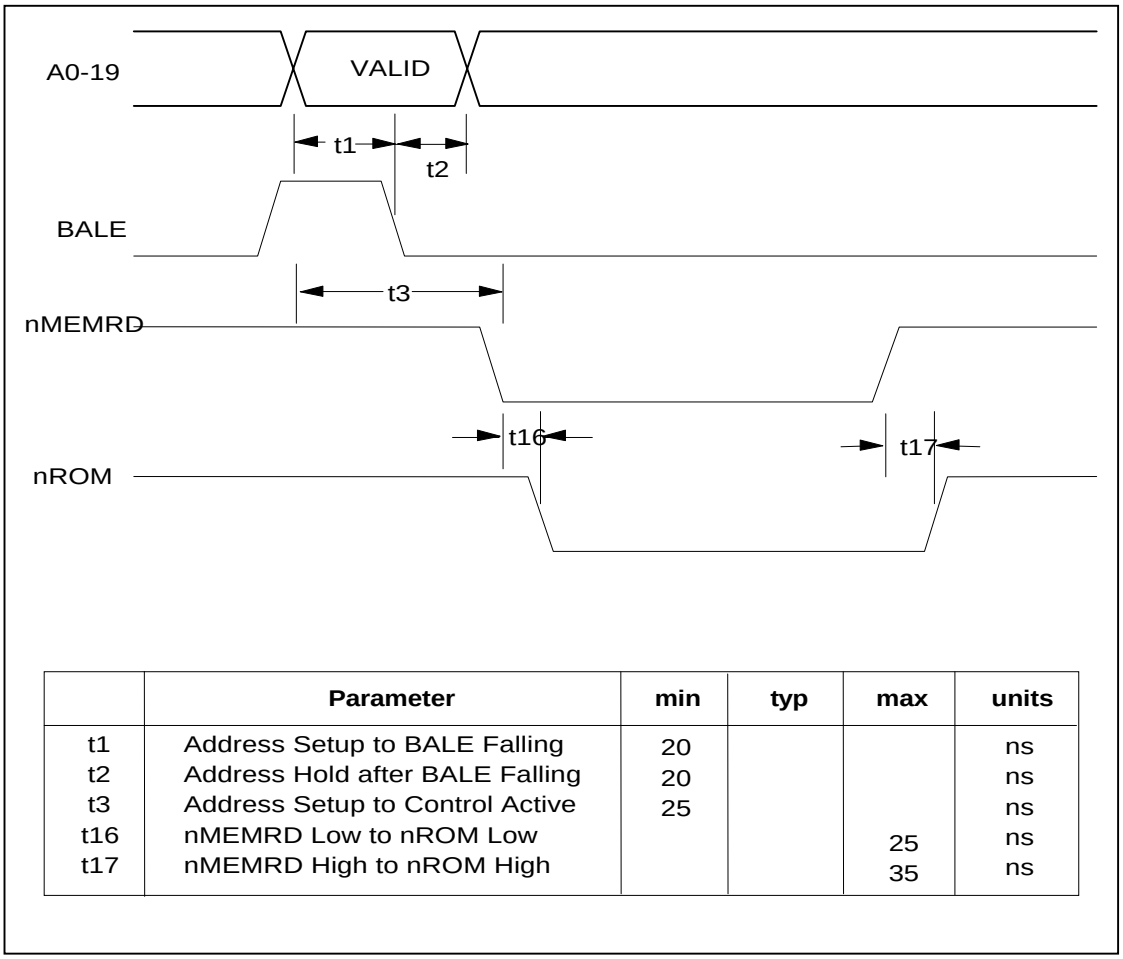
FIGURE 27 - EXTERNAL ROM READ ACCESS



	Parameter	min	typ	max	units
t1	Address, nSBHE Setup to BALE Falling	20			ns
t2	Address, nSBHE Hold after BALE Falling	20			ns
t3	Address, nSBHE, AEN Setup to Control Active	25			ns
t4	AEN Hold after Control Inactive	20			ns
t15	A4-A15, AEN Low, BALE High to nIOCS16 Low			25	ns

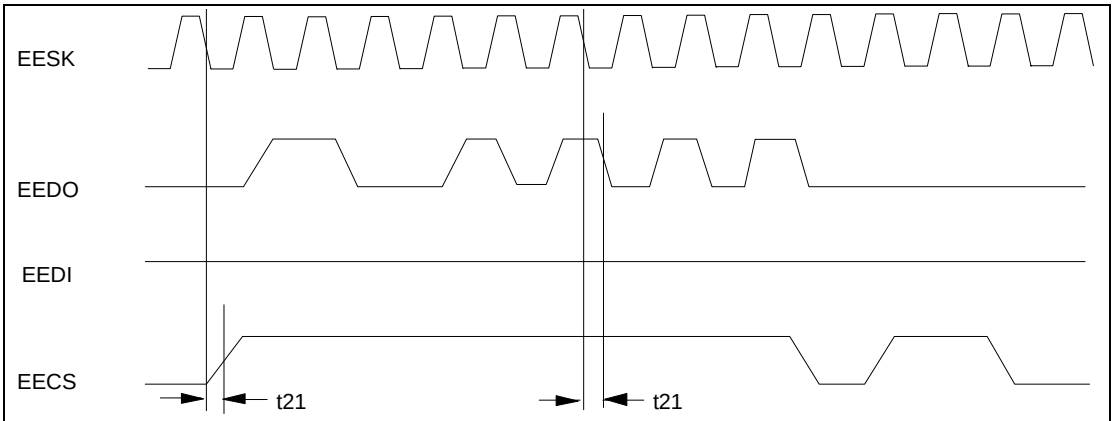
t4 not needed. nIOCS16 not relevant in 8-bit mode.

FIGURE 28 - ISA REGISTER ACCESS WHEN USING BALE



	Parameter	min	typ	max	units
t1	Address Setup to BALE Falling	20			ns
t2	Address Hold after BALE Falling	20			ns
t3	Address Setup to Control Active	25			ns
t16	nMEMRD Low to nROM Low			25	ns
t17	nMEMRD High to nROM High			35	ns

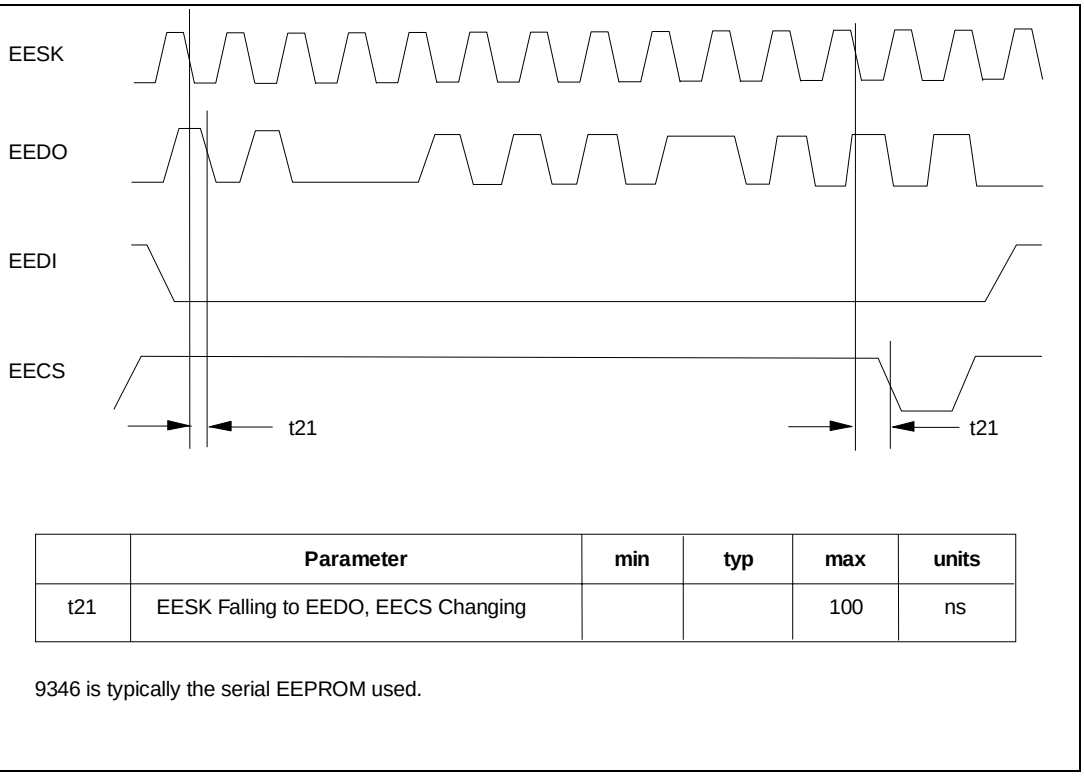
FIGURE 29 - EXTERNAL ROM READ ACCESS USING BALE



	Parameter	min	typ	max	units
t21	EESK Falling to EEDO, EECS Changing	0		100	ns

9346 is typically the serial EEPROM used.

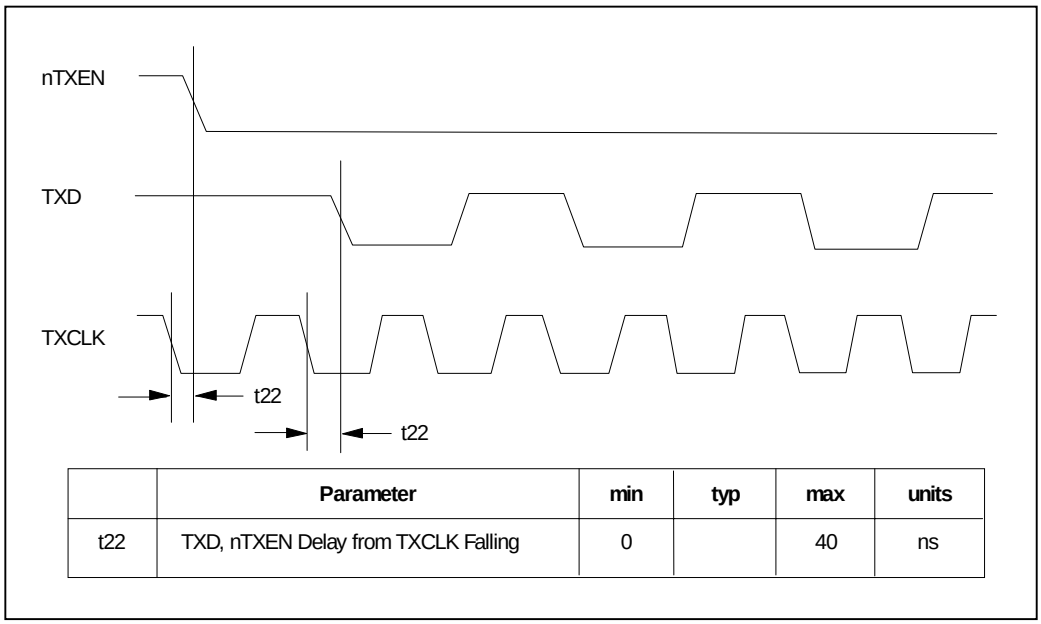
FIGURE 30 - EEPROM READ



	Parameter	min	typ	max	units
t21	EESK Falling to EEDO, EECS Changing			100	ns

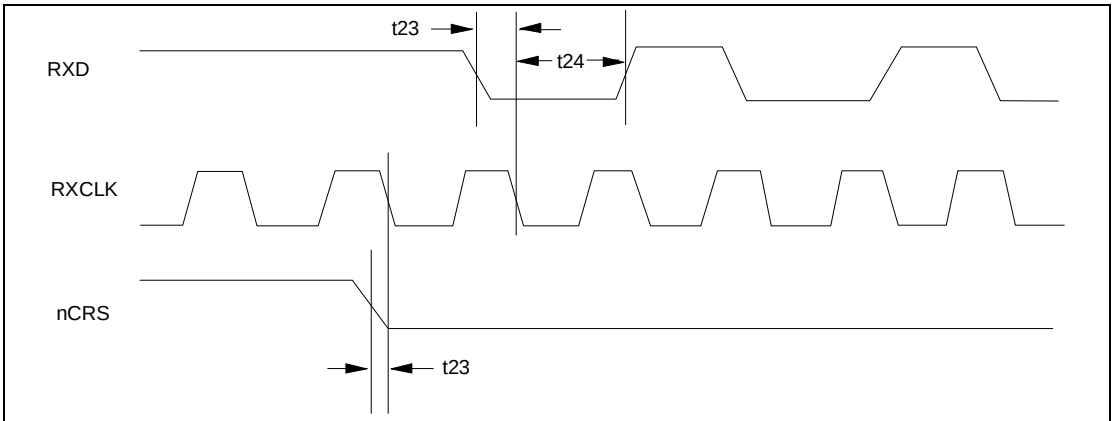
9346 is typically the serial EEPROM used.

FIGURE 31 - EEPROM WRITE



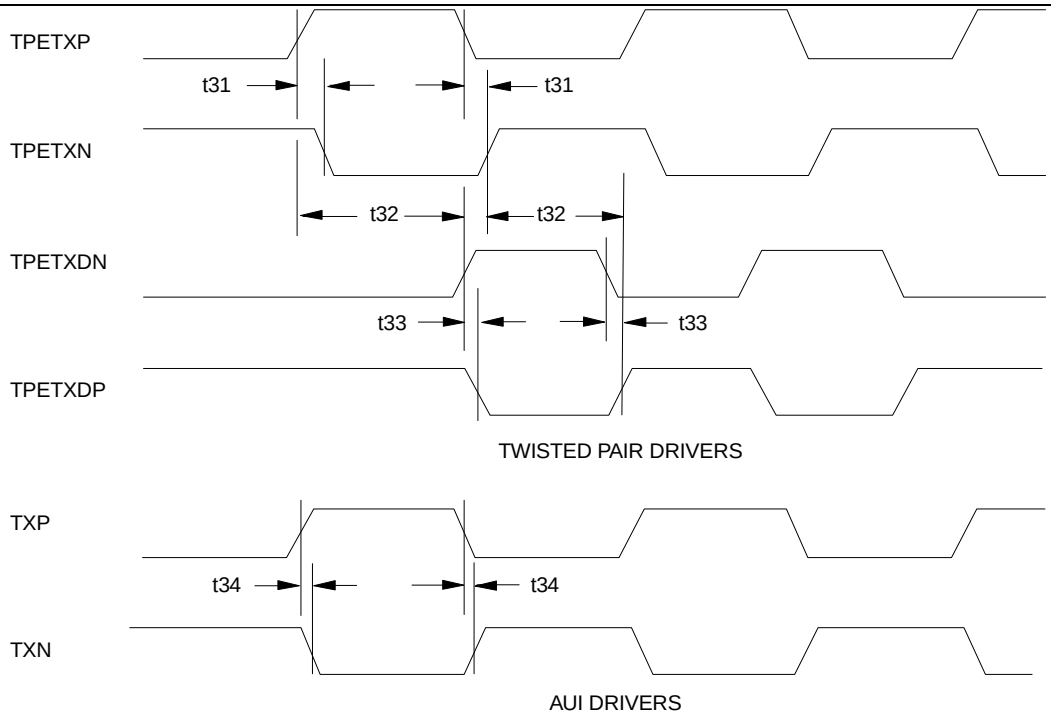
	Parameter	min	typ	max	units
t22	TXD, nTXEN Delay from TXCLK Falling	0		40	ns

FIGURE 32 - EXTERNAL ENDEC INTERFACE - START OF TRANSMIT



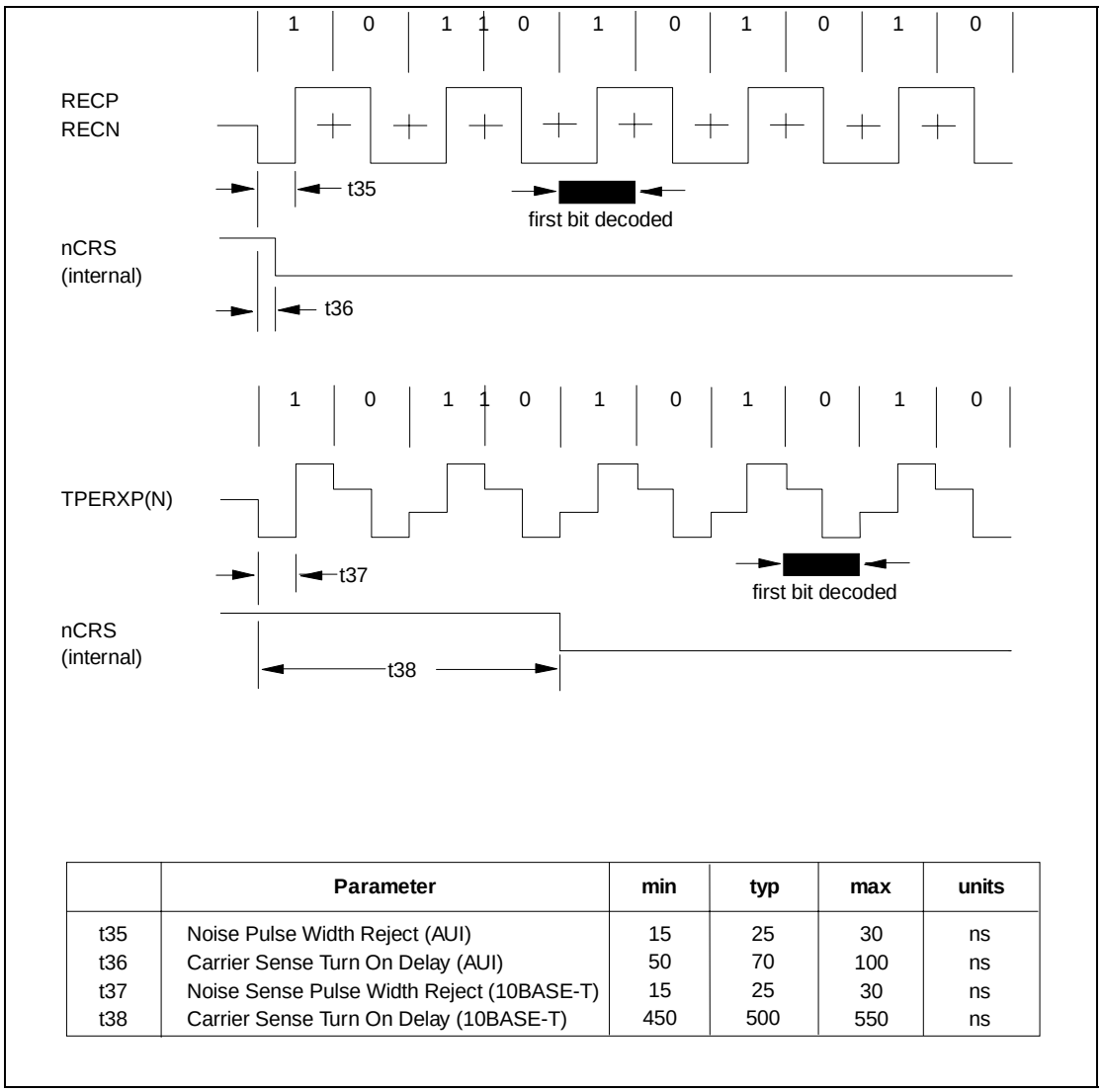
	Parameter	min	typ	max	units
t23	nCRS, RXD Setup to RXCLK Falling	10			ns
t24	nCRS, RXD Hold after RXCLK Falling	30			ns

FIGURE 33 - EXTERNAL ENDEC INTERFACE - RECEIVE DATA (RXD SAMPLED BY FALLING RXCLK)



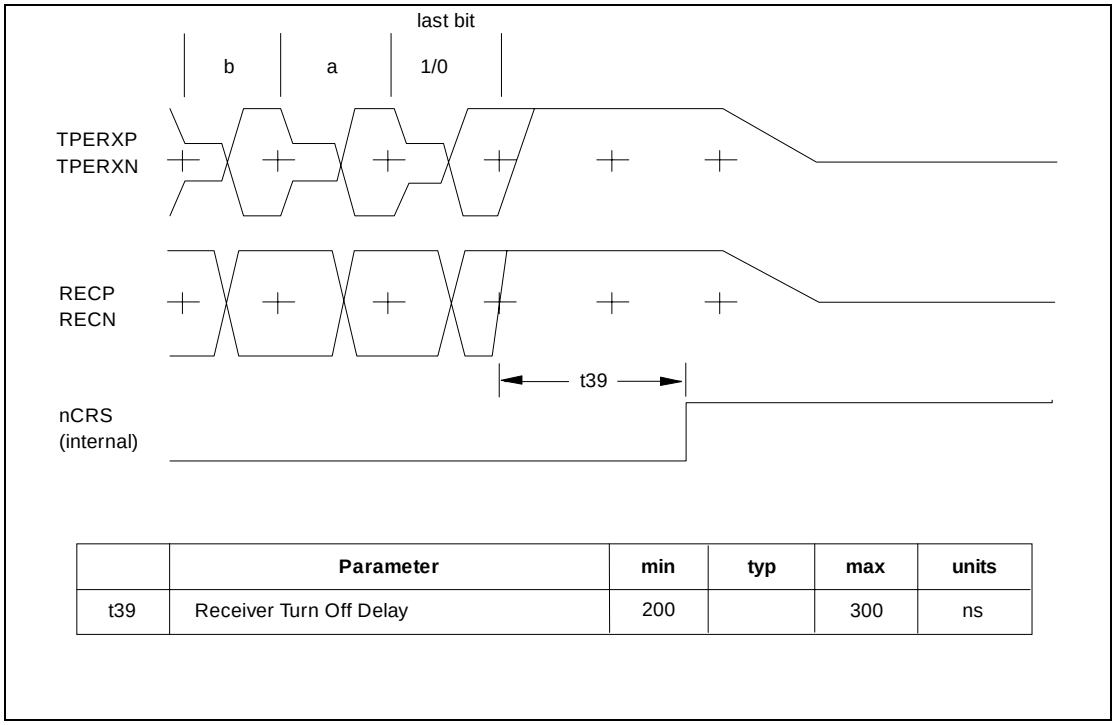
	Parameter	min	typ	max	units
t31	TPETXP to TPETXN Skew	-1		+1	ns
t32	TPETXP(N) to TPETXDP(N) Delay	47		53	ns
t33	TPETXDN to TPETXDP Skew	-1		+1	ns
t34	TXP to TXN Skew	-1.5		1.5	ns

FIGURE 34 - DIFFERENTIAL OUTPUT SIGNAL TIMING (10BASE-T AND AUI)



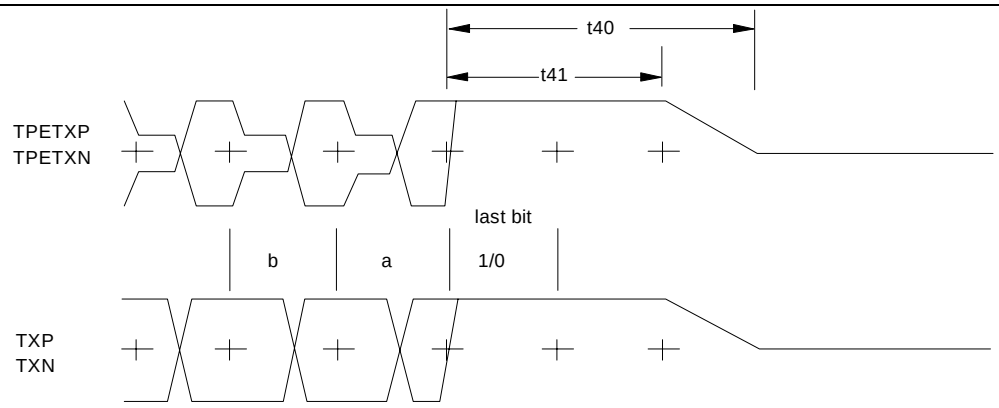
	Parameter	min	typ	max	units
t35	Noise Pulse Width Reject (AUI)	15	25	30	ns
t36	Carrier Sense Turn On Delay (AUI)	50	70	100	ns
t37	Noise Sense Pulse Width Reject (10BASE-T)	15	25	30	ns
t38	Carrier Sense Turn On Delay (10BASE-T)	450	500	550	ns

FIGURE 35 - RECEIVE TIMING - START OF FRAME (AUI AND 10BASE-T)



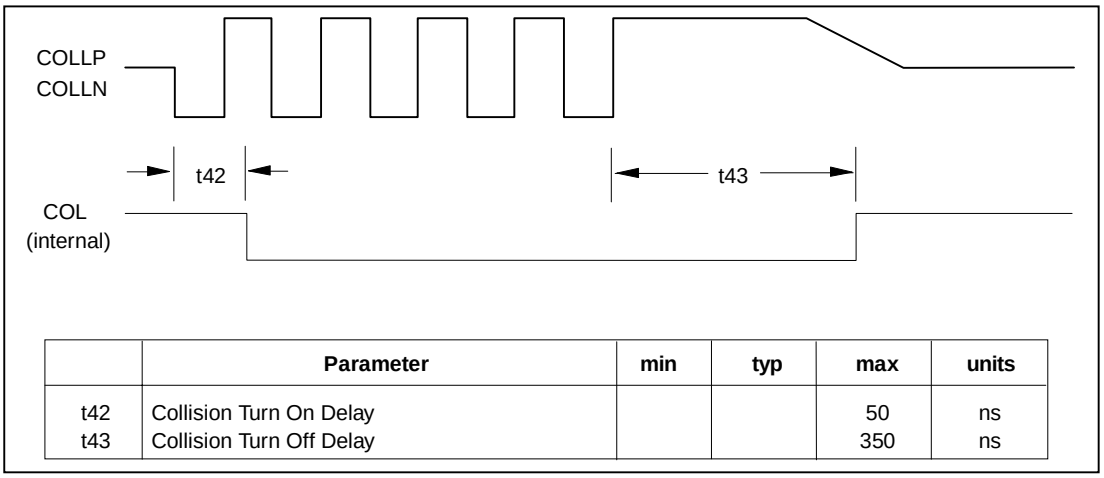
	Parameter	min	typ	max	units
t39	Receiver Turn Off Delay	200		300	ns

FIGURE 36 - RECEIVE TIMING - END OF FRAME (AUI AND 10BASE-T)



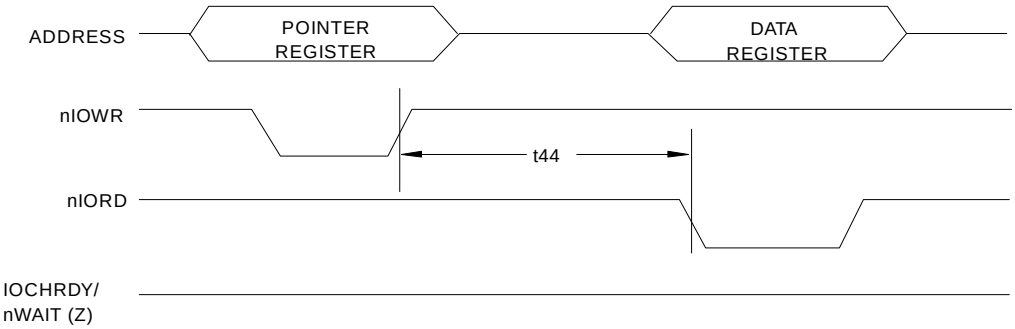
	Parameter	min	typ	max	units
t40	Transmit Output High to Idle in Half-Step Mode			800	ns
t41	Transmit Output High before Idle in Half-Step Mode	200			ns

FIGURE 37 - TRANSMIT TIMING - END OF FRAME (AUI AND 10BASE-T)



	Parameter	min	typ	max	units
t42	Collision Turn On Delay			50	ns
t43	Collision Turn Off Delay			350	ns

FIGURE 38 - COLLISION TIMING (AUI)



	Parameter	min	typ	max	units
t44	Pointer Register Reloaded to a Word of Data Prefetched into Data Register	2 * t20			ns

Note: If t44 is not met, IOCHRDY will be negated for the required time. This parameter can be ignored if IOCHRDY is connected to the system.

FIGURE 39 - MEMORY READ TIMING

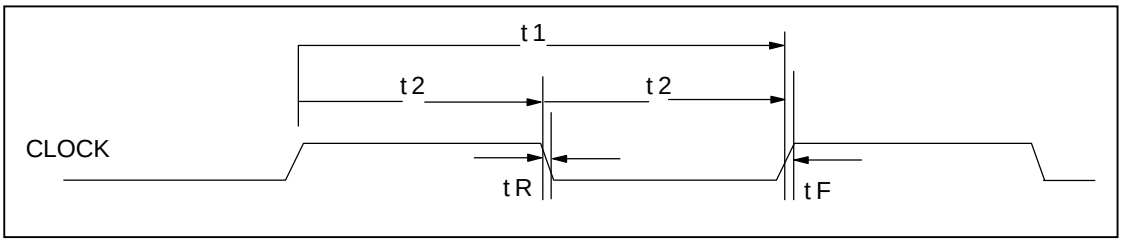
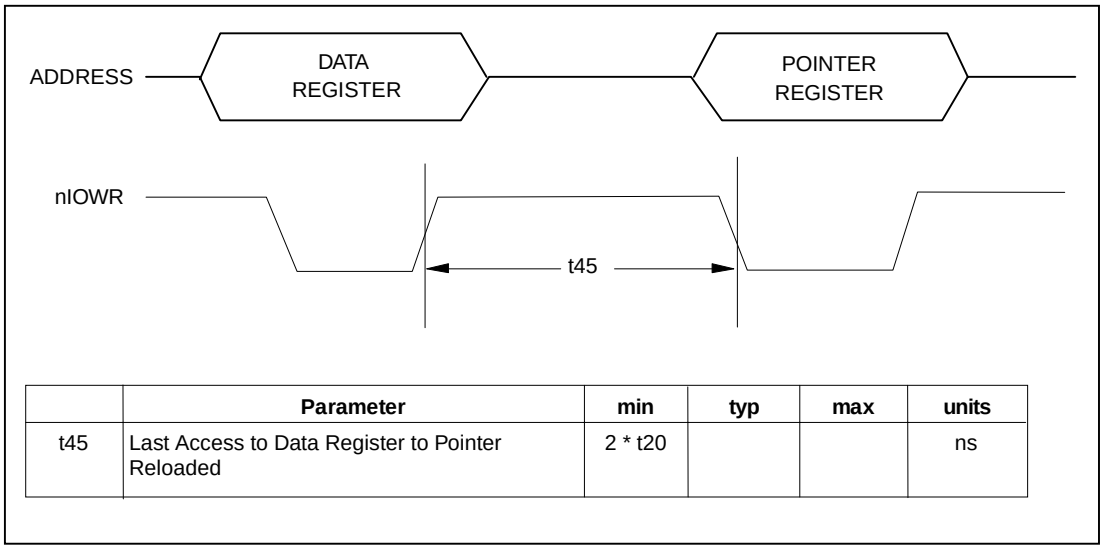


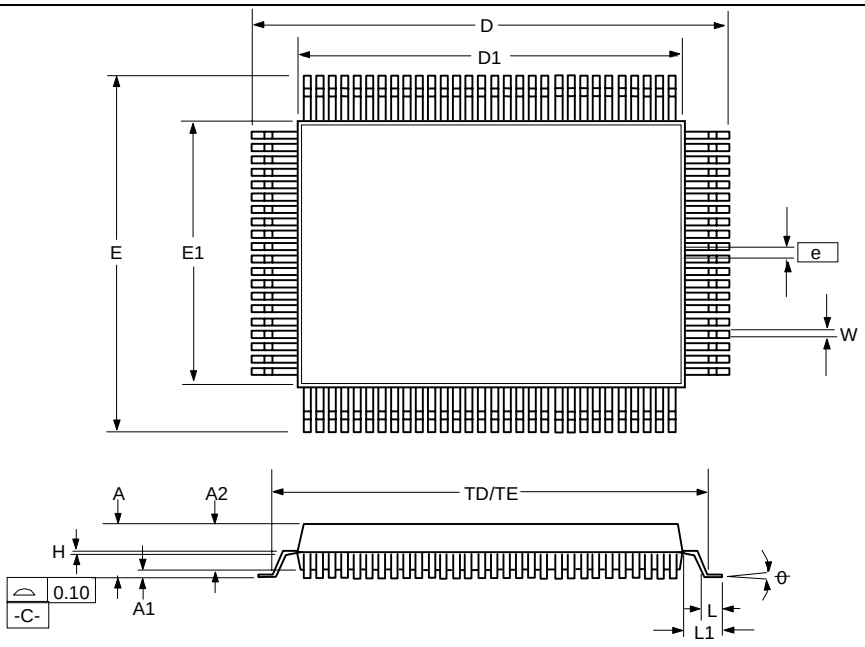
FIGURE 40 - INPUT CLOCK TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Clock Cycle Time for 20 MHz		50		ns
t2	Clock High Time/Low Time for 20 MHz	30/20		20/30	ns
tR, tF	Clock Rise Time/Fall Time			5	ns
	Xtal1 Startup time (from 1.6v of Vcc rising)			50	msec
	Xtal1 Capture Range (Xtal1 frequency variation)	19.7		20.3	MHz
	Xtal Internal feedback resistor	1		3	Meg Ohm



	Parameter	min	typ	max	units
t45	Last Access to Data Register to Pointer Reloaded	2 * t20			ns

FIGURE 41 - MEMORY WRITE TIMING



	Millimeters		Inches	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	2.80	3.15	.110	.124
A1	0.1	0.45	.004	.018
A2	2.57	2.87	.101	.113
D	23.4	24.15	.921	.951
D1	19.9	20.1	.783	.791
E	17.4	18.15	.685	.715
E1	13.9	14.1	.547	.555
H	0.1	0.2	.004	.008
L	0.65	0.95	.026	.037
L1	1.8	2.6	.071	.102
e	0.65 BSC		.0256 BSC	
θ	0°	12°	0°	12°
W	.2	.4	.008	.016
TD(1)	21.8	22.2	.858	.874
TE(1)	15.8	16.2	.622	.638
TD(2)	22.21	22.76	.874	.896
TE(2)	16.27	16.82	.641	.662

Notes:

1) Coplanarity is 0.100mm (.004") maximum.

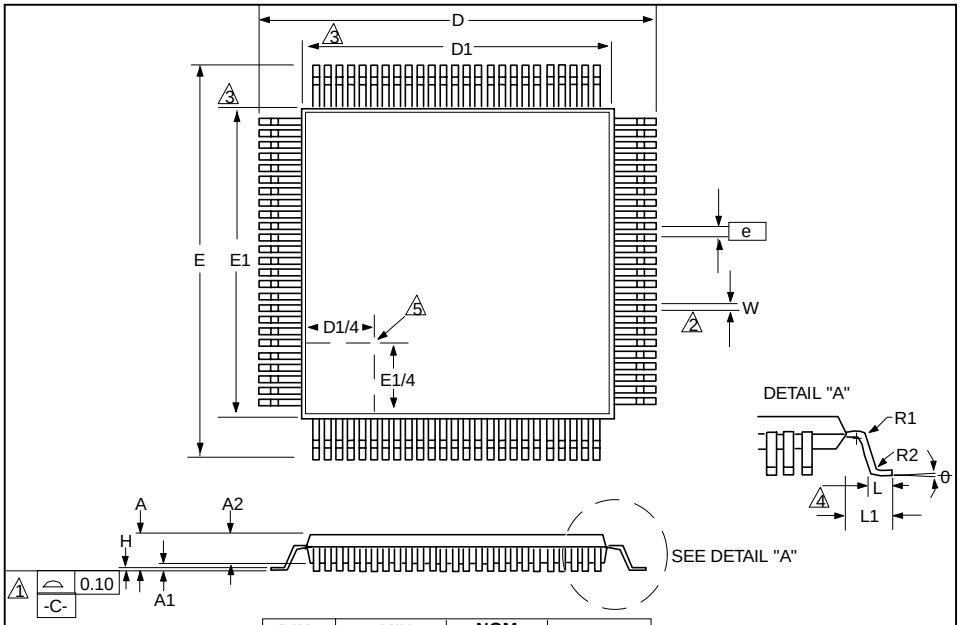
2) Tolerance on the position of the leads is 0.200mm (.008") maximum.

3) Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25mm (.010").

4) Dimensions TD and TE are important for testing by robotic handler. Only above combinations of (1) or (2) are acceptable.

5) Controlling dimension: millimeter. Dimensions in inches for reference only and not necessarily accurate.

FIGURE 42 - 100 PIN QFP PACKAGE



DIM	MIN	NOM	MAX
A			1.20
A1	0.05	0.10	.15
A2	0.95	1.00	1.05
D	15.90	16.00	16.10
D1	13.90	14.00	14.10
E	15.90	16.00	16.10
E1	13.90	14.00	14.10
H	0.09		0.20
L	0.45	0.60	0.75
L1		1.00	
e		0.50 BSC	
~~θ~~	0°		7°
W	0.17	0.22	0.27
ccc			0.08

Notes:
1. Coplanarity is 0.08mm or 3.2 mils maximum.
2. Tolerance on the position of the leads is 0.080mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25mm.
4. Dimension for foot length L are measured at the gauge plane 0.25mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.
6. Controlling dimension: millimeter

FIGURE 43 – 100 PIN TQFP PACKAGE