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Motorola Semiconductor Application Note

AN1282

Board Strategies for Ensuring Optimum Frequency Synthesizer Performance

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Introduction

Microcontroller-based applications can be delayed or jeopardized by reduced phase locked loop (PLL) performance. This poor performance is often associated with the design of the circuit board in which the microcontroller is installed. This application note describes common problems and suggests key practices to avoid PLL problems and performance degradation.

Figure 1 shows the main functional blocks of the MPC505/MPC509 PLL. These blocks include the phase detector, charge pump, loop filter (R_{XFC}, $C1_{XFCP}$), voltage controlled oscillator (VCO) and divider for normal mode operation. These component blocks provide adequate PLL performance. However, PLL performance can be affected by leakage at the XFCP node, capacitor characteristics, phase noise from the reference signal, reference spurs, and board noise.

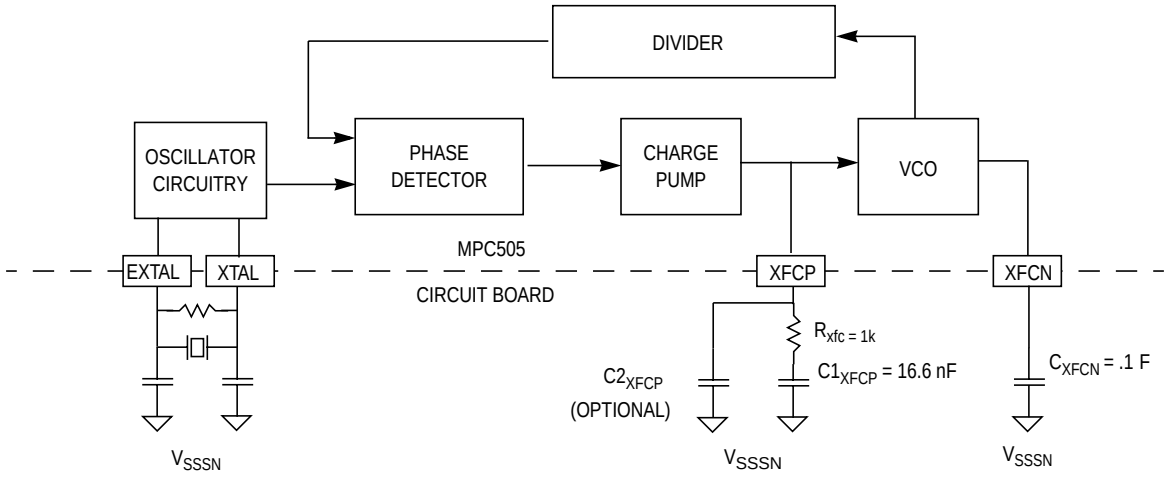

Figure 1. Simplified MPC505 PLL Block Diagram for Normal Mode Operation

Leakage on XFCP Node

The XFCP node is essential to the overall performance of the MPC505/MPC509 PLL. Since it provides a reference voltage to the VCO, any change in voltage at this node causes a proportional frequency deviation determined by the gain of the VCO. Leakage currents are a common source of non-ideal voltage error at the XFCP node. Leakage currents either charge or discharge the $C1_{XFCP}$ capacitor. They are usually a result of a parasitic low impedance path between the XFCP node and V_{DDSN} or V_{SSSN}. If this impedance is maximized, then the leakage current is minimized.

For this reason, it is important to measure the impedance between XFCP and V_{DDSN} as well as between XFCP and V_{SSSN}. These impedances must be greater than 42 MΩ in order for the PLL to operate at maximum performance. If there is less than 42 MΩ of resistance between the XFCP node and V_{SSSN} or V_{DDSN}, refer to **Table 1** to narrow down the source of leakage currents.

Table 1. Common Sources of Board Leakage

Solder resin (flux) on the PC board
Surface contamination of the PC board, occasionally in the form of a very thin film which may not be easily removed even with TF freon solvent
Fingerprints and humidity
Leaky capacitors
Unacceptable variation in solder resist mask

If high leakage currents persist, one possible solution is to employ a guard ring around the loop filter components. **Figure 2** illustrates this approach. The voltages at nodes 1, 2, 3, and 5 are approximately equal because the voltage at XFCN is a buffered version of the voltage at XFCP. There is a parasitic resistance between nodes 3 and 4. This resistance is composed of two series resistors between nodes 3 and 5 (R1) and nodes 5 and 4 (R2). Because the guard band is present and the voltage at node 3 and 5 are approximately equal, the leakage current, i_{leak1}, from node 3 to node 4 is approximately zero. From a qualitative standpoint, the leakage current may be considerably higher if guard banding is not performed, although it is still dependent upon the voltage of node 3 and the impedance between nodes 3 and 4.

Capacitor Characteristics

The board designer must choose a dielectric that minimizes undesirable capacitor characteristics. This may require a trade-off between cost and performance. The main capacitor characteristics that affect PLL performance are leakage, capacitance change over temperature, series inductance, and dielectric absorption.

As mentioned earlier, leakage associated with the XFCP node affects jitter performance by changing the voltage across the filter during PLL operation. Large capacitance changes due to changes in temperature can also reduce PLL stability. The XFCN and XFCP capacitances should have less than ± 25% capacitance variation over the MPC505/MPC509 operating temperature range.

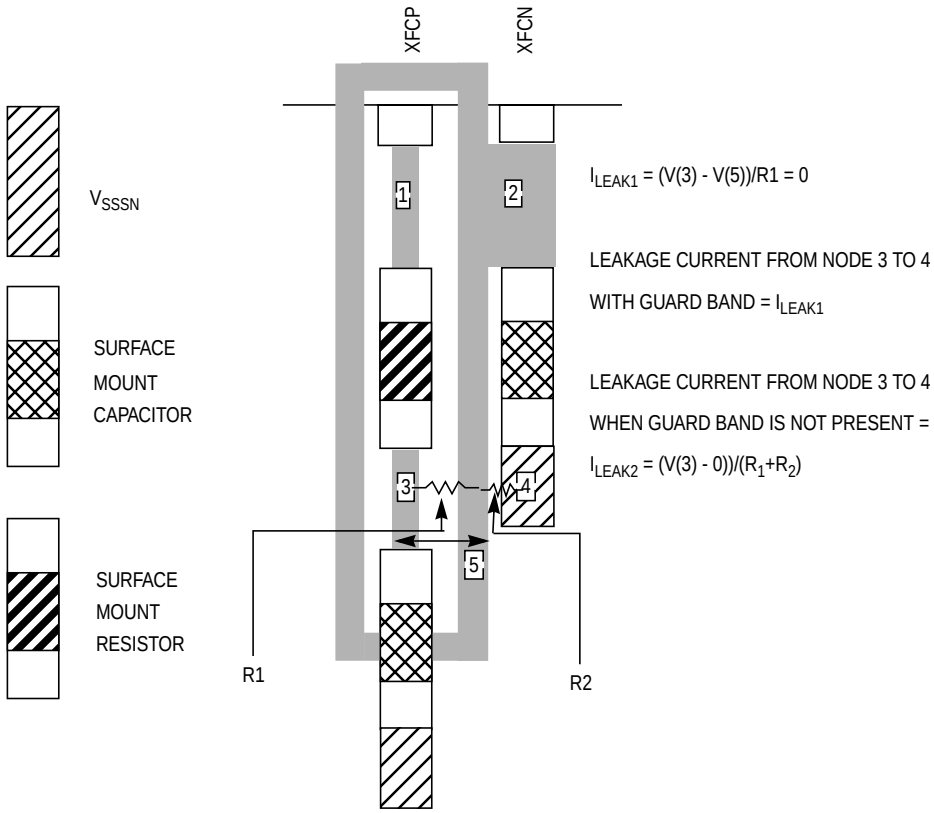

Figure 2. Guard Banding to Reduce Leakage

Inductance and resistance associated with traces of the XFCP and XFCN node degrade PLL performance by supplying Ldi/dt and Rdi/dt noise to the VCO, which causes jitter to increase. This noise can be attenuated by minimizing trace lengths and maximizing trace widths associated with the XFCN and XFCP pins.

Dielectric absorption is due to “memory” of the dielectric. When the MF divider value changes, control voltage to the VCO also changes. The capacitors respond with 99% of the voltage in a normal fashion, but, as the dielectric relaxes, the remaining 1% of settling can last as much as 10 times longer than the first 99%. In other words, dielectric absorption lengthens the time the PLL needs to acquire frequency errors of less than 1%. **Table 2** shows characteristics of various dielectrics and their effect on MPC505/MPC509 PLL performance.

Table 2. Common Ceramic Capacitor Dielectrics

Suggestions	Dielectric	Dielectric Attributes
Use	NPO	+ low temperature dependence (± 30ppm/ °C) + doesn’t suffer from dielectric absorption (less than 0.6%) + large insulation resistance (10,000 MΩ) or low leakage
Use	X7R	+ tolerable temperature dependence (± 15%) – suffers from dielectric absorption + large insulation resistance (10,000 MΩ) or low leakage
Do Not Use	Z5U	– very temperature dependent (+22% to –56%) + large insulation resistance (10,000 MΩ) or low leakage
Do Not Use	Y5V	– very temperature dependent (+22% to –82%) + large insulation resistance (10,000 MΩ) or low leakage

Phase Noise from Reference Signal

A clean reference signal is essential because the PLL tends to track reference phase noise or frequency jitter. Phase noise commonly appears as a frequency that modulates or rides upon the reference frequency. The PLL rejects the high frequency components and passes the low frequency components (<40 kHz) of the signal. The low frequency component modulates VCO output frequency and worsens PLL jitter.

If a crystal oscillator is used for the reference frequency, take care to design oscillator circuitry so that frequency jitter is minimized. **Figure 3** is an example of good layout. Minimize feedback between the EXTAL and XTAL lengths by routing them a distance from each other. Route V_{SSSN} to isolate oscillator input from oscillator output and from adjacent circuitry. Avoid ground loops around oscillator components, and keep leads to a minimum length.

Power supply noise affects oscillator frequency performance in the same way it affects the VCO. Consequently, power supply noise and noise coupling must be minimized. These topics are discussed under **Noise** and **Noise Coupling**.

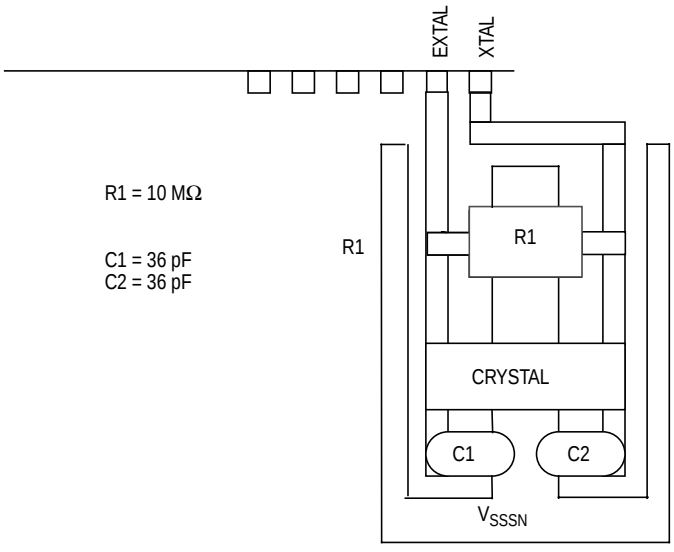

Figure 3. Suggested Crystal Oscillator Layout

Reference Spurs

Most analog PLLs produce reference spurs, which apply a noise voltage directly to the VCO input at the same frequency as the PLL reference signal. This noise voltage limits the minimum phase error that can be maintained between the reference signal and the VCO output or CLKOUT. Placing a bypass capacitor between the XFCP node and V_{SSSN}, as shown in **Figure 4**, may attenuate the noise. Thus, it is strongly recommended that all boards be designed so that this capacitor can be added if jitter improvements are needed.

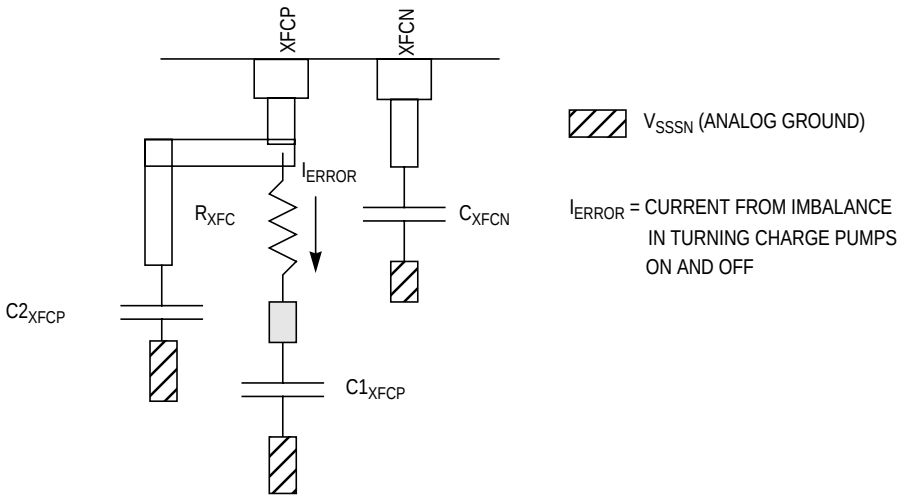

Figure 4. Bypass Capacitor ($C2_{XFCP}$) for Improved Jitter Performance

Noise

Noise is probably the biggest obstacle to jitter performance. Analog PLLs must produce a low jitter clock in an electrically noisy environment. This section discusses how to minimize board level noise on the V_{SSSN}, V_{DDSN}, V_{DDKAP1}, XFCP, and XFCN pins.

One common source of power supply noise is a result of directly connecting analog and digital supplies, as shown in **Figure 5**.

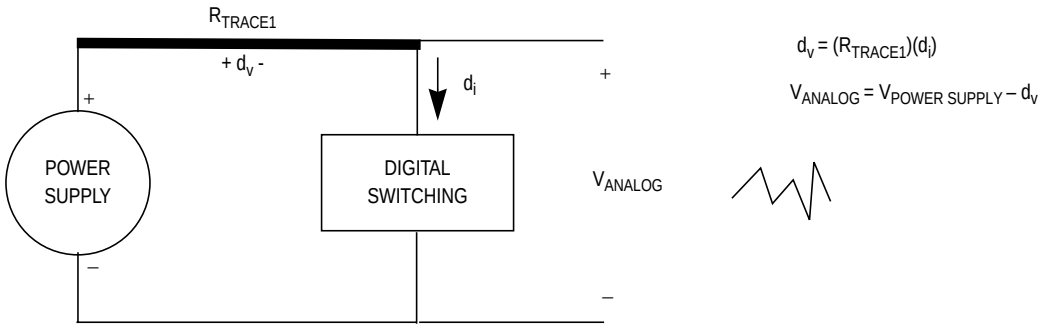

Figure 5. Impact of Digital Switching Noise on Analog Supply

In accordance with Kirchhoff's voltage law, the analog supply is modulated by d_V, which is a result of current being switched through the inherent resistance of the board traces. VCO output frequency is modulated by the power supplies, and jitter increases.

Now that a major source of noise has been identified, it is possible to see how the noise can be attenuated. **Figure 6** and **Figure 7** show two approaches to power supply decoupling. Both figures include a power supply (which is not a switching voltage regulator), digital logic, oscillator, and PLL block. The power supply lines connected to the digital logic block represent supplies for all digital logic on the board, including the MPC505/MPC509. In this Star Point configuration, the oscillator and the PLL are connected to the power supply by separate traces, and have little exposure to digital switching noise.

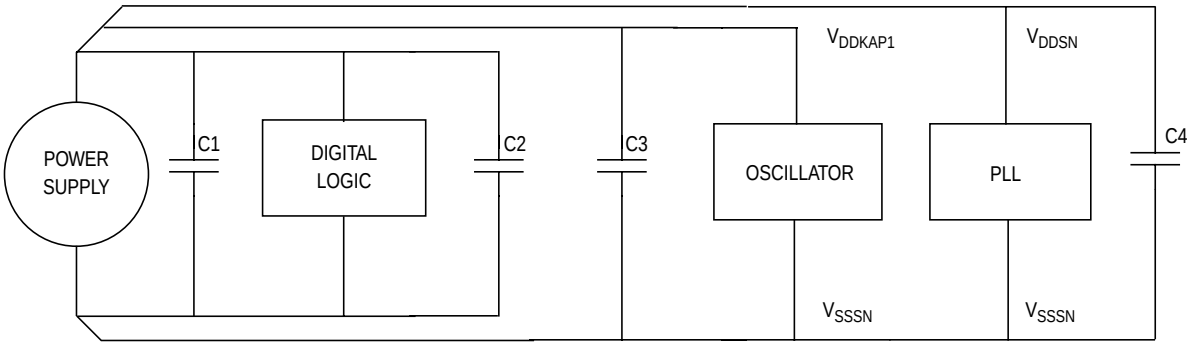

Figure 6. Star Point Power Supply Connection

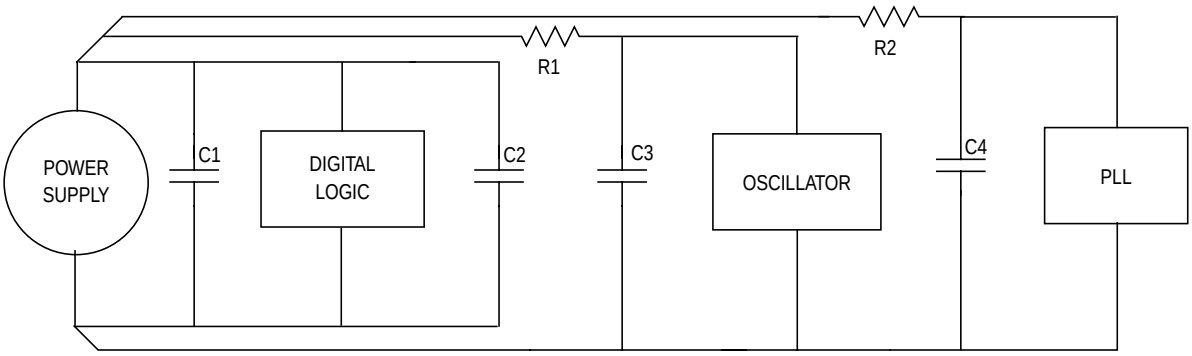

Figure 7. Star Point Power Supply Connection Strategy with First Order Filters

Bypass capacitors (C1, C2, C3, and C4) are used to further attenuate power supply noise. C1 is a large capacitor (47 F) that inhibits low frequency noise from the supplies. C2 represents bypass capacitors (0.01 F – 0.1 F) needed to reduce high frequency noise on MPC505/MPC509 digital power supplies and other digital circuitry. C3 and C4 are bypass capacitors (0.01 – 0.1 F) for the oscillator and the PLL. It is important to place bypass capacitors as close to the supply pins as possible; otherwise, inductance from the circuit traces will limit the capacitors' ability to filter high frequency noise.

In **Figure 7** a greater level of power supply isolation is achieved by means of RC filters. The filter capacitors must have values between 0.01 μF to 0.1 μF. The filter resistors must be sized so that no more than a 100 mV drop occurs across them at the highest MPC505/MPC509 system frequency used.

Exercise great care in the signal routing style for board layouts of this type. All corners associated with power supply traces should be made in two 45 degree turn segments to reduce power supply routing resistance and noise. Power supply traces should be made as wide as possible to further reduce resistance and inductance. Because the ground lines cannot be filtered easily, it is also important to minimize the inductance and resistance associated with the ground — a V_{SSSN} ground plane should be utilized when possible.

Noise Coupling

Noise is commonly coupled to analog nodes via routing. When digital traces run parallel or even overlap analog signals on a multi-layer board, the digital signals may be inductively or capacitively coupled to the analog signals. As a result, the XFCN, XFCP, V_{DDKAP1}, V_{DDSN}, and V_{SSSN} traces must be separated from the digital traces. No digital logic signals should cross above or below the analog signal traces. In addition, digital signals must be routed away from analog signals at a 90 degree angle with respect to the analog signals, to limit inductive coupling

PLL Check List and Summary

PLL Specific

- Measure resistance between pins XFCP and V_{DDSN} as well as between pins XFCP and V_{SSSN}. The resistances must be greater than 42 MΩ to insure proper PLL operation.
- Ensure flux is properly washed off board
- Minimize all lead lengths associated with the XFCP and XFCN lines
- Attempt to either use NPO or X7R dielectrics for C_{XFCP} and C_{XFCN}
- Ensure that a low jitter reference signal is provided to the PLL
- Take care in laying out the oscillator traces
- Minimize capacitor lead lengths associated with crystal oscillator capacitors
- Add traces for $C2_{XFCP}$ between pins XFCP and V_{SSSN} in case a bypass capacitor needs to be added to improve jitter performance
- Don’t use a switching voltage regulator in conjunction with the oscillator or PLL supplies
- Connect oscillator and PLL power traces directly to the power source

Noise

Suppressing the Noise Source

- Keep clock signal loop as close to zero as possible
- Use 45-degree angle trace turns for power supply instead of 90-degree angle trace turns

Reduce Noise Coupling

- Separate circuits on a PCB according to their frequency and current switching level
- Place chips for short clock runs
- Confine high speed logic to specific functions
- If possible, use a multi-layer board with separate analog and digital ground planes to minimize power and ground inductance
- Use wide traces for power and ground, especially if a multi-layer board is not used.
- Keep digital signal lines as far away from the PLL and oscillator as possible
- Minimize length of traces associated with the PLL
- Don’t run digital signals under or near the traces associated with the oscillator and PLL

Suggested Loop Filter Component Values

Normal mode:

$C1_{XFCP}$ = 16.6 nF R_{XFC} = 960

1 to 1 Mode:

$C1_{XFCP}$ = 100 nF R_{XFC} = 160

Glossary

These terms are used in a variety of ways within the frequency synthesizer community. The following definitions are used in this note.

Stability means that the PLL will eventually achieve a minimum phase error with the reference signal. A stable PLL reference signal and output signal should always phase lock when there is no significant noise within the system.

Phase error is the time difference between the falling edge of the reference clock and the falling edge of the feedback clock, CLKOUT. This difference should equate to less than 3% of the feedback clock.

Phase noise and **jitter** are used interchangeably. Since phase is equal to the integral of frequency, any frequency variation over time (jitter) will cause a variation in phase (phase noise).

References

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