APPENDIX A
MPC555 INTERNAL MEMORY MAP

The tables below use the following notations.

In the Access column:

S = Supervisor Access Only
U = User Access
T = Test Access

In the Reset column:

S = $\overline{\text{SRESET}}$
H = $\overline{\text{HRESET}}$
M = $\overline{\text{Module Reset}}$
POR = $\overline{\text{Power-On Reset}}$
U = Unchanged
X = Unknown

The codes in the Reset column indicate which reset has an effect on register values.

INDEX of MEMORY MAP TABLES

Table A-1 SPR (Special Purpose Registers)

Address	Access	Symbol	Register	Size	Reset
MSR	S	MSR	Machine State Register. See **Table 3-12** for bit descriptions	32	S
SPR 1	U	XER	Integer Exception Register. See **Table 3-10** for bit descriptions	32	U
SPR 8	U	LR	Link Register. See **3.7.6 Link Register (LR)** for bit descriptions.	32	U
SPR 9	U	CTR	Count Register. See **3.7.7 Count Register (CTR)** for bit descriptions.	32	U
SPR 18	S	DSISR	DAE/Source Instruction Service Register. See **3.9.2 DAE/Source Instruction Service Register (DSISR)** for bit descriptions.	32	U
SPR 19	S	DAR	Data Address Register. See **3.9.3 Data Address Register (DAR)** for bit descriptions.	32	U
SPR 22	S	DEC	Decrementer Register. See **3.9.5 Decrementer Register (DEC)** for bit descriptions.	32	U
SPR 26	S	SRR0	Machine Status Save/Restore Register 0. See **3.9.6 Machine Status Save/Restore Register 0 (SRR0)** for bit descriptions.	32	U
SPR 27	S	SRR1	Machine Status Save/Restore Register 1. See **3.9.7 Machine Status Save/Restore Register 1 (SRR1)** for bit descriptions.	32	U
SPR 80	S	EIE	External Interrupt Enable Register See **3.9.10.1 EIE, EID, and NRI Special-Purpose Registers** for bit descriptions.	32	—
SPR 81	S	EID	External Interrupt Disable Register See **3.9.10.1 EIE, EID, and NRI Special-Purpose Registers** for bit descriptions.	32	—
SPR 82	S	NRI	Non-Recoverable Interrupt Register See **3.9.10.1 EIE, EID, and NRI Special-Purpose Registers** for bit descriptions.	32	—
SPR 144	S	CMPA	Comparator A Value Register. See **Table 21-17** for bit descriptions.	32	U
SPR 145	S	CMPB	Comparator B Value Register. See **Table 21-17** for bit descriptions.	32	U
SPR 146	S	CMPC	Comparator C Value Register. See **Table 21-17** for bit descriptions.	32	U
SPR 147	S	CMPD	Comparator D Value Register. See **Table 21-17** for bit descriptions.	32	U
SPR 148	S	ECR	Exception Cause Register See **Table 21-26** for bit descriptions.	32	S
SPR 149	S	DER	Debug Enable Register See **Table 21-27** for bit descriptions.	32	S
SPR 150	S	COUNTA	Breakpoint Counter A Value and Control Register See **Table 21-24** for bit descriptions.	32	U
SPR 151	S	COUNTB	Breakpoint Counter B Value and Control Register See **Table 21-25** for bit descriptions.	32	U
SPR 152	S	CMPE	Comparator G Value Register. See **Table 21-20** for bit descriptions.	32	U

Table A-1 SPR (Special Purpose Registers) (Continued)

Address	Access	Symbol	Register	Size	Reset
SPR 153	S	CMPF	Comparator H Value Register. See **Table 21-20** for bit descriptions.	32	U
SPR 154	S	CMPG	Comparator E Value Register. See **Table 21-18** for bit descriptions.	32	U
SPR 155	S	CMPH	Comparator F Value Register. See **Table 21-18** for bit descriptions.	32	U
SPR 156	S	LCTRL1	L-Bus Support Control Register 1 See **Table 21-22** for bit descriptions.	32	S
SPR 157	S	LCTRL2	L-Bus Support Control Register 2 See **Table 21-23** for bit descriptions.	32	S
SPR 158	S	ICTRL	I-Bus Support Control Register. See **Table 21-21** for bit descriptions.	32	S
SPR 159	S	BAR	Breakpoint Address Register. See **Table 21-19** for bit descriptions.	32	U
SPR 268, 269	U read only	TB	Time Base (Read Only). See **Table 3-11** for bit descriptions.	64	U
SPR 272	S	SPRG0	General Special Purpose Registers. See **3.9.8 General SPRs (SPRG0–SPRG3)** for bit descriptions.	32	U
SPR 273	S	SPRG1	General Special Purpose Registers. See **3.9.8 General SPRs (SPRG0–SPRG3)** for bit descriptions.	32	U
SPR 274	S	SPRG2	General Special Purpose Registers. See **3.9.8 General SPRs (SPRG0–SPRG3)** for bit descriptions.	32	U
SPR 275	S	SPRG3	General Special Purpose Registers. See **3.9.8 General SPRs (SPRG0–SPRG3)** for bit descriptions.	32	U
SPR 284, 285	S write only	TB	Time Base Register (Write Only). See **Table 3-14** for bit descriptions.	64	U
SPR 287	S read only	PVR	Processor Version Registers. See **Table 3-16** for bit descriptions.	32	U
SPR 528	S	MI_GRA	Global Region Attribute Register. See **Table 4-7** for bit descriptions.	32	H
SPR 536	S	L2U_GRA	L2U Global Region Attribute Register. See **Table 11-10** for bit descriptions.	32	POR, H
SPR 560	S	BBCMCR	BBC Module Configuration Register. See **Table 4-8** for bit descriptions.	32	U
SPR 568	U	L2U_MCR	L2U Module Configuration Register. See **Table 11-7** for bit descriptions.	32	POR, H
SPR 630	S	DPDR	Development Port Data Register.	32	U
SPR 638	S	IMMR	Internal Memory Mapping Register. See **Table 6-11** for bit descriptions.	32	H
SPR 784	S	MI_RBA0	Region Address Register 0. See **Table 4-5** for bit descriptions.	32	U
SPR 785	S	MI_RBA1	Region Address Register 1. See **Table 4-5** for bit descriptions.	32	U
SPR 786	S	MI_RBA2	Region Address Register 2. See **Table 4-5** for bit descriptions.	32	U
SPR 787	S	MI_RBA3	Region Address Register 3. See **Table 4-5** for bit descriptions.	32	U
SPR 792	S	L2U_RBA0	L2U Region 0 Address Register. See **Table 11-8** for bit descriptions.	32	POR, H

Table A-1 SPR (Special Purpose Registers) (Continued)

Address	Access	Symbol	Register	Size	Reset
SPR 793	S	L2U_RBA1	L2U Region 1 Address Register. See **Table 11-8** for bit descriptions.	32	POR, H
SPR 794	S	L2U_RBA2	L2U Region 2 Address Register. See **Table 11-8** for bit descriptions.	32	POR, H
SPR 795	S	L2U_RBA3	L2U Region 3Address Register. See **Table 11-8** for bit descriptions.	32	POR, H
SPR 816	S	MI_RA0	Region Attribute Register 0. See **Table 4-6** for bit descriptions.	32	U
SPR 817	S	MI_RA1	Region Attribute Register 1. See **Table 4-6** for bit descriptions.	32	U
SPR 818	S	MI_RA2	Region Attribute Register 2. See **Table 4-6** for bit descriptions.	32	U
SPR 819	S	MI_RA3	Region Attribute Register 3. See **Table 4-6** for bit descriptions.	32	U
SPR 824	S	L2U_RA0	L2U Region 0 Attribute Register. See **Table 11-9** for bit descriptions.	32	POR, H
SPR 825	S	L2U_RA1	L2U Region 1 Attribute Register. See **Table 11-9** for bit descriptions.	32	POR, H
SPR 826	S	L2U_RA2	L2U Region 2 Attribute Register. See **Table 11-9** for bit descriptions.	32	POR, H
SPR 827	S	L2U_RA3	L2U Region 3 Attribute Register. See **Table 11-9** for bit descriptions.	32	POR, H
SPR 1022	S	FPECR	Floating-Point Exception Cause Register. See **3.9.10.2 Floating-Point Exception Cause Register (FPECR)** for bit descriptions.	32	S

Table A-2 CMF (CDR MoneT Flash EEPROM) Flash Array

Address	Access	Symbol	Register	Size	Reset
0x00 0000 – 0x03 FFFF			CMF_A Flash Array	8, 16, 32	—
0x04 0000 – 0x06 FFFF			CMF_B Flash Array	8, 16, 32	—

Table A-3 USIU (Unified System Interface Unit)

Address	Access	Symbol	Register	Size	Reset
0x2F C000	U[1]	SIUMCR	SIU Module Configuration Register. See **Table 6-5** for bit descriptions.	32	H
0x2F C004	U[2]	SYPCR	System Protection Control Register. See **Table 6-13** for bit descriptions.	32	H
0x2F C008	—	—	Reserved	—	—
0x2F C00E	U, write only	SWSR	Software Service Register. See **Table 6-14** for bit descriptions.	16	S
0x2F C010	U	SIPEND	Interrupt Pending Register. See **6.13.2.1 SIPEND Register** for bit descriptions.	32	S
0x2F C014	U	SIMASK	Interrupt Mask Register. See **6.13.2.2 SIU Interrupt Mask Register (SIMASK)** for bit descriptions.	32	S

Table A-3 USIU (Unified System Interface Unit) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x2F C018	U	SIEL	Interrupt Edge Level Mask. See **6.13.2.3 SIU Interrupt Edge Level Register (SIEL)** for bit descriptions.	32	H
0x2F C01C	U, read only	SIVEC	Interrupt Vector. See **6.13.2.4 SIU Interrupt Vector Register** for bit descriptions.	32	—
0x2F C020	U	TESR	Transfer Error Status Register. See **Table 6-15** for bit descriptions.	32	S
0x2F C024	U	SGPIODT1	USIU General-Purpose I/O Data Register 1. See **Table 6-21** for bit descriptions.	32	H
0x2F C028	U	SGPIODT2	USIU General-Purpose I/O Data Register 2. See **Table 6-22** for bit descriptions.	32	H
0x2F C02C	U	SGPIOCR	USIU General-Purpose I/O Control Register. See **Table 6-23** for bit descriptions.	32	H
0x2F C030	U	EMCR	External Master Mode Control Register. See **Table 6-12** for bit descriptions.	32	H
0x2F C03C	U	PDMCR	Pads Module Configuration Register. See **Table 2-3** for bit descriptions.	32	H
0x2F C040 – 0x2F C0FC	—	—	Reserved	—	—
Memory Controller Registers					
0x2F C100	U	BR0	Base Register 0. See **Table 10-7** for bit descriptions.	32	H
0x2F C104	U	OR0	Option Register 0. See **Table 10-8** for bit descriptions.	32	H
0x2F C108	U	BR1	Base Register 1. See **Table 10-7** for bit descriptions.	32	H
0x2F C10C	U	OR1	Option Register 1. See **Table 10-8** for bit descriptions.	32	H
0x2F C110	U	BR2	Base Register 2. See **Table 10-7** for bit descriptions.	32	H
0x2F C114	U	OR2	Option Register 2. See **Table 10-8** for bit descriptions.	32	H
0x2F C118	U	BR3	Base Register 3. See **Table 10-7** for bit descriptions.	32	H
0x2F C11C	U	OR3	Option Register 3. See **Table 10-8** for bit descriptions.	32	H
0x2F C120 – 0x2F C13C	—	—	Reserved	—	—
0x2F C140	U	DMBR	Dual-Mapping Base Register. See **Table 10-9** for bit descriptions.	32	H
0x2F C144	U	DMOR	Dual-Mapping Option Register. See **Table 10-10** for bit descriptions.	32	H
0x2F C148 – 0x2F C174	—	—	Reserved	—	—
0x2F C178	U	MSTAT	Memory Status. See **Table 10-6** for bit descriptions.	16	H
System Integration Timers					
0x2F C200	U[3]	TBSCR	Time Base Status and Control. See **Table 6-16** for bit descriptions.	16	H
0x2F C204	U[3]	TBREF0	Time Base Reference 0. See **6.13.4.3 Time Base Reference Registers** for bit descriptions.	32	U

Table A-3 USIU (Unified System Interface Unit) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x2F C208	U[3]	TBREF1	Time Base Reference 1. See **6.13.4.3 Time Base Reference Registers** for bit descriptions.	32	U
0x2F C20C – 0x2F C21C	—	—	Reserved	—	—
0x2F C220	U[4]	RTCSC	Real Time Clock Status and Control. See **Table 6-17** for bit descriptions.	16	H
0x2F C224	U[4]	RTC	Real Time Clock. See **6.13.4.6 Real-Time Clock Register (RTC)** for bit descriptions.	32	U
0x2F C228	T[4]	RTSEC	Real Time Alarm Seconds, reserved.	32	—
0x2F C22C	U[4]	RTCAL	Real Time Alarm. See **6.13.4.7 Real-Time Clock Alarm Register (RTCAL)** for bit descriptions.	32	U
0x2F C230 – 0x2F C23C	—	—	Reserved	—	—
0x2F C240	U[3]	PISCR	PIT Status and Control. See **Table 6-18** for bit descriptions.	16	H
0x2F C244	U[3]	PITC	PIT Count. See **Table 6-19** for bit descriptions.	32 (half reserved)	U
0x2F C248	U, read only	PITR	PIT Register. See **Table 6-20** for bit descriptions.	32 (half reserved)	U
0x2F C24C – 0x2F C27C		—	Reserved	—	—
Clocks and Reset					
0x2F C280	U[2]	SCCR	System Clock Control Register. See **Table 8-9** for bit descriptions.	32	H
0x2F C284	U[3,5,6]	PLPRCR	PLL Low Power and Reset Control Register. See **Table 8-10** for bit descriptions.	32	H
0x2F C288	U[3]	RSR	Reset Status Register. See **Table 7-3** for bit descriptions.	16	POR
0x2F C28C	U	COLIR	Change of Lock Interrupt Register. See **Table 8-11** for bit descriptions.	16	U
0x2F C290	U	VSRMCR	VDDSRM Control Register. See **Table 8-12** for bit descriptions.	16	U
0x2F C294 – 0x2F C2FC	—	—	Reserved	—	—
System Integration Timer Keys					
0x2F C300	U	TBSCRK	Time Base Status and Control Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C304	U	TBREF0K	Time Base Reference 0 Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C308	U	TBREF1K	Time Base Reference 1 Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C30C	U	TBK	Time Base and Decrementer Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C310 – 0x2F C31C	—	—	Reserved	—	—
0x2F C320	U	RTCSCK	Real-Time Clock Status and Control Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C324	U	RTCK	Real-Time Clock Key. See **Table 8-8** for bit descriptions.	32	POR

Table A-3 USIU (Unified System Interface Unit) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x2F C328	U	RTSECK	Real-Time Alarm Seconds Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C32C	U	RTCALK	Real-Time Alarm Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C330 – 0x2F C33C	—	—	Reserved	—	—
0x2F C340	U	PISCRIK	PIT Status and Control Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C344	U	PITCK	PIT Count Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C348 – 0x2F C37C	—	—	Reserved	—	—
Clocks and Reset Keys					
0x2F C380	U	SCCRK	System Clock Control Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C384	U	PLPRCRK	PLL Low-Power and Reset Control Register Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C388	U	RSRK	Reset Status Register Key. See **Table 8-8** for bit descriptions.	32	POR
0x2F C38C – 0x2F C3FC		—	Reserved	—	—

NOTES:

1. Entire register is locked if bit 15 (DLK) is set.
2. Write once after power on reset (POR).
3. Must use the key register to unlock if it has been locked by a key register, see **8.9.3.2 Keep Alive Power Registers Lock Mechanism**.
4. Locked after Power on Reset (POR). A write of 0x55CCAA33 must performed to the key register to unlock. See **8.9.3.2 Keep Alive Power Registers Lock Mechanism**.
5. Can have bits 0:11 (MF bits) write-protected by setting bit 4 (MFPDL) in the SCCR register to 1. Bit 21 (CSRC) and bits 22:23 (LPM) can be locked by setting bit 5 (LPML) of the SCCR register to 1.
6. Bit 24 (CSR) is write-once after soft reset.

Table A-4 CMF (CDR MoneT Flash EEPROM)

Address	Access	Symbol	Register	Size	Reset
CMF_A					
0x2F C800	S[1]	CMFMCR	CMF_A EEPROM Configuration Register. See **Table 19-2** for bit descriptions.	32	POR, H
0x2F C804	S	CMFTST	CMF_A EEPROM Test Register. See **Table 19-3** for bit descriptions.	32	POR, H
0x2F C808	S	CMFCTL	CMF_A EEPROM High Voltage Control Register. See **Table 19-5** for bit descriptions.	32	POR, H
CMF_B					
0x2F C840	S[1]	CMFMCR	CMF_B EEPROM Configuration Register. See **Table 19-2** for bit descriptions.	32	POR, H
0x2F C844	S	CMFTST	CMF_B EEPROM Test Register. See **Table 19-3** for bit descriptions.	32	POR, H
0x2F C848	S	CMFCTL	CMF_B EEPROM High Voltage Control Register. See **Table 19-5** for bit descriptions.	32	POR, H

NOTES:

1. Bit 3 (FIC) is write-once. Bit 0 ($\overline{\text{LOCK}}$) is write-once unless in freeze or test mode.

Table A-5 DPTRAM (Dual-Port TPU RAM)

Address	Access	Symbol	Register	Size	Reset
0x30 0000	S	DPTMCR	DPT Module Configuration Register. See **Table 18-2** for bit descriptions.	16	S
0x30 0002	T	RAMTST	Test register, factory test only.	16	S
0x30 0004	S[1]	RAMBAR	RAM Array Address Register. See **Table 18-3** for bit descriptions.	16	S
0x30 0006	S, read only	MISRH	Multiple Input Signature Register High. See **18.3.4 MISR High (MISRH) and MISR Low (MISRL)** for bit descriptions.	16	S
0x30 0008	S, read only	MISRL	Multiple Input Signature Register Low. See **18.3.4 MISR High (MISRH) and MISR Low (MISRL)** for bit descriptions.	16	S
0x30 000A	S, read only	MISCNT	MISC Counter. See **18.3.5 MISC Counter (MISCNT)** for bit descriptions.	16	S

NOTES:
1. Entire register is write-once.

Table A-6 DPTRAM Array

Address	Access	Symbol	Register	Size	Reset
0x30 2000 – 0x30 37FF	U, S[1]		DPTRAM Array	—	—

NOTES:
1. Access to the DPTRAM array through the IMB3 bus is disabled once bit 5 (EMU) of either TPUMCR is set.

Table A-7 TPU3 (Time Processor Unit)

Address	Access	Symbol	Register	Size	Reset
TPU_A (Note: Bit descriptions apply to TPU_B as well)					
0x30 4000	S[1]	TPUMCR_A	TPU3_A Module Configuration Register. See **Table 17-6** for bit descriptions.	16 only	S, M
0x30 4002	T	TCR_A	TPU3_A Test Configuration Register.	16	S, M
0x30 4004	S	DSCR_A	TPU3_A Development Support Control Register. See **Table 17-7** for bit descriptions.	16[2]	S, M
0x30 4006	S	DSSR_A	TPU3_A Development Support Status Register. See **Table 17-8** for bit descriptions.	16[2]	S, M
0x30 4008	S	TICR_A	TPU3_A Interrupt Configuration Register. See **Table 17-9** for bit descriptions.	16[2]	S, M
0x30 400A	S	CIER_A	TPU3_A Channel Interrupt Enable Register. See **Table 17-10** for bit descriptions.	16[2]	S, M
0x30 400C	S	CFSR0_A	TPU3_A Channel Function Selection Register 0. See **Table 17-11** for bit descriptions.	16[2]	S, M
0x30 400E	S	CFSR1_A	TPU3_A Channel Function Selection Register 1. See **Table 17-11** for bit descriptions.	16[2]	S, M
0x30 4010	S	CFSR2_A	TPU3_A Channel Function Selection Register 2. See **Table 17-11** for bit descriptions.	16[2]	S, M
0x30 4012	S	CFSR3_A	TPU_A Channel Function Selection Register 3. See **Table 17-11** for bit descriptions.	16[2]	S, M

Table A-7 TPU3 (Time Processor Unit) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 4014	S/U[3]	HSQR0_A	TPU_A Host Sequence Register 0. See **Table 17-12** for bit descriptions.	16[2]	S, M
0x30 4016	S/U[3]	HSQR1_A	TPU_A Host Sequence Register 1. See **Table 17-12** for bit descriptions.	16[2]	S, M
0x30 4018	S/U[3]	HSRR0_A	TPU_A Host Service Request Register 0. See **Table 17-13** for bit descriptions.	16[2]	S, M
0x30 401A	S/U[3]	HSRR1_A	TPU_A Host Service Request Register 1. See **Table 17-13** for bit descriptions.	16[2]	S, M
0x30 401C	S	CPR0_A	TPU_A Channel Priority Register 0. See **Table 17-14** for bit descriptions.	16[2]	S, M
0x30 401E	S	CPR1_A	TPU_A Channel Priority Register 1. See **Table 17-14** for bit descriptions.	16[2]	S, M
0x30 4020	S	CISR_A	TPU_A Channel Interrupt Status Register. See **Table 17-16** for bit descriptions.	16	S, M
0x30 4022	T	LR_A	TPU_A Link Register	16[2]	S, M
0x30 4024	T	SGLR_A	TPU_A Service Grant Latch Register	16[2]	S, M
0x30 4026	T	DCNR_A	TPU_A Decoded Channel Number Register	16[2]	S, M
0x30 4028	S[4]	TPUMCR2_A	TPU_A Module Configuration Register 2. See **Table 17-17** for bit descriptions.	16[2]	S, M
0x30 402A	S	TPUMCR3_A	TPU_A Module Configuration Register 3. See **Table 17-20** for bit descriptions.	16[2]	S, M
0x30 402C	T	ISDR_A	TPU_A Internal Scan Data Register	16, 32[2]	
0x30 402E	T	ISCR_A	TPU_A Internal Scan Control Register	16, 32[2]	
0x30 4100 – 0x30 410F	S/U[3]	—	TPU_A Channel 0 Parameter Registers	16, 32[2]	
0x30 4110 – 0x30 411F	S/U[3]	—	TPU_A Channel 1 Parameter Registers	16, 32[2]	
0x30 4120 – 0x30 412F	S/U[3]	—	TPU_A Channel 2 Parameter Registers.	16, 32[2]	
0x30 4130 – 0x30 413F	S/U[3]	—	TPU_A Channel 3 Parameter Registers.	16, 32[2]	
0x30 4140 – 0x30 414F	S/U[3]	—	TPU_A Channel 4 Parameter Registers	16, 32[2]	
0x30 4150 – 0x30 415F	S/U[3]	—	TPU_A Channel 5 Parameter Registers	16, 32[2]	
0x30 4160 – 0x30 416F	S/U[3]	—	TPU_A Channel 6 Parameter Registers	16, 32[2]	
0x30 4170 – 0x30 417F	S/U[3]	—	TPU_A Channel 7 Parameter Registers	16, 32[2]	
0x30 4180 – 0x30 418F	S/U[3]	—	TPU_A Channel 8 Parameter Registers	16, 32[2]	
0x30 4190 – 0x30 419F	S/U[3]	—	TPU_A Channel 9 Parameter Registers	16, 32[2]	
0x30 41A0 – 0x30 41AF	S/U[3]	—	TPU_A Channel 10 Parameter Registers	16, 32[2]	
0x30 41B0 – 0x30 41BF	S/U[3]	—	TPU_A Channel 11 Parameter Registers	16, 32[2]	
0x30 41C0 – 0x30 41CF	S/U[3]	—	TPU_A Channel 11 Parameter Registers	16, 32[2]	
0x30 41D0 – 0x30 41DF	S/U[3]	—	TPU_A Channel 11 Parameter Registers	16, 32[2]	

Table A-7 TPU3 (Time Processor Unit) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 41E0 – 0x30 41EF	S/U[3]	—	TPU_A Channel 14 Parameter Registers	16, 32[2]	
0x30 41F0 – 0x30 41FF	S/U[3]	—	TPU_A Channel 15 Parameter Registers	16, 32[2]	
TPU_B					
0x30 4400[1]	S[1]	TPUMCR_B	TPU3_B Module Configuration Register	16 only	S, M
0x30 4402	T	TCR_B	TPU3_B Test Configuration Register	16	S, M
0x30 4404	S	DSCR_B	TPU3_B Development Support Control Register	16[2]	S, M
0x30 4406	S	DSSR_B	TPU3_B Development Support Status Register	16[2]	S, M
0x30 4408	S	TICR_B	TPU3_B Interrupt Configuration Register	16[2]	S, M
0x30 440A	S	CIER_B	TPU3_B Channel Interrupt Enable Register	16[2]	S, M
0x30 440C	S	CFSR0_B	TPU3_B Channel Function Selection Register 0	16[2]	S, M
0x30 440E	S	CFSR1_B	TPU3_B Channel Function Selection Register 1	16[2]	S, M
0x30 4410	S	CFSR2_B	TPU3_B Channel Function Selection Register 2	16[2]	S, M
0x30 4412	S	CFSR3_B	TPU_B Channel Function Selection Register 3	16[2]	S, M
0x30 4414	S/U[3]	HSQR0_B	TPU_B Host Sequence Register 0	16[2]	S, M
0x30 4416	S/U[3]	HSQR1_B	TPU_B Host Sequence Register 1	16[2]	S, M
0x30 4418	S/U[3]	HSRR0_B	TPU_B Host Service Request Register 0	16[2]	S, M
0x30 441A	S/U[3]	HSRR1_B	TPU_B Host Service Request Register 1	16[2]	S, M
0x30 441C	S	CPR0_B	TPU_B Channel Priority Register 0	16[2]	S, M
0x30 441E	S	CPR1_B	TPU_B Channel Priority Register 1	16[2]	S, M
0x30 4420	S	CISR_B	TPU_B Channel Interrupt Status Register	16	S, M
0x30 4422	T	LR_B	TPU_B Link Register	16[2]	S, M
0x30 4424	T	SGLR_B	TPU_B Service Grant Latch Register	16[2]	S, M
0x30 4426	T	DCNR_B	TPU_B Decoded Channel Number Register	16[2]	S, M
0x30 4428	S[4]	TPUMCR2_B	TPU_B Module Configuration Register 2	16[2]	S, M
0x30 442A	S	TPUMCR3_B	TPU_B Module Configuration Register 3	16, 32[2]	S, M
0x30 442C	T	ISDR_B	TPU_B Internal Scan Data Register	16, 32[2]	
0x30 442E	T	ISCR_B	TPU_B Internal Scan Control Register	16, 32[2]	
0x30 4500 – 0x30 450E	S/U[3]	—	TPU_B Channel 0 Parameter Registers	16, 32[2]	
0x30 4510 – 0x30 451E	S/U[3]	—	TPU_B Channel 1 Parameter Registers	16, 32[2]	
0x30 4520 – 0x30 452E	S/U[3]	—	TPU_B Channel 2 Parameter Registers	16, 32[2]	
0x30 4530 – 0x30 453E	S/U[3]	—	TPU_B Channel 3 Parameter Registers	16, 32[2]	
0x30 4540 – 0x30 454E	S/U[3]	—	TPU_B Channel 4 Parameter Registers	16, 32[2]	
0x30 4550 – 0x30 455E	S/U[3]	—	TPU_B Channel 5 Parameter Registers	16, 32[2]	
0x30 4560 – 0x30 456E	S/U[3]	—	TPU_B Channel 6 Parameter Registers	16, 32[2]	
0x30 4570 – 0x30 457E	S/U[3]	—	TPU_B Channel 7 Parameter Registers	16, 32[2]	

Table A-7 TPU3 (Time Processor Unit) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 4580 – 0x30 458E	S/U[3]	—	TPU_B Channel 8 Parameter Registers	16, 32[2]	
0x30 4590 – 0x30 459E	S/U[3]	—	TPU_B Channel 9 Parameter Registers	16, 32[2]	
0x30 45A0 – 0x30 45AE	S/U[3]	—	TPU_B Channel 10 Parameter Registers	16, 32[2]	
0x30 45B0 – 0x30 45BF	S/U[3]	—	TPU_B Channel 11 Parameter Registers	16, 32[2]	
0x30 45C0 – 0x30 45CF	S/U[3]	—	TPU_B Channel 11 Parameter Registers	16, 32[2]	
0x30 45D0 – 0x30 45DF	S/U[3]	—	TPU_B Channel 11 Parameter Registers	16, 32[2]	
0x30 45E0 – 0x30 45EF	S/U[3]	—	TPU_B Channel 14 Parameter Registers	16, 32[2]	
0x30 45F0 – 0x30 45FF	S/U[3]	—	TPU_B Channel 15 Parameter Registers	16[2]	

NOTES:

1. Bit 10 (TPU3) and bit 11 (T2CSL) are write-once. Bits 1:2 (TCR1P) and bits 3:4 (TCR2P) are write-once if PWOD is not set in the TPUMCR3 register. This register cannot be accessed with a 32-bit read. It can only be accessed with an 8- or 16-bit read.
2. Some TPU registers can only be read or written with 16- or 32-bit accesses. 8-bit accesses are not allowed.
3. S/U = Supervisor accessible only if SUPV = 1 or unrestricted if SUPV = 0. Unrestricted registers allow both user and supervisor access. The SUPV bit is in the TPUMCR register.
4. Bits 9:10 (ETBANK), 14 (T2CF), and 15 (DTPU) are write-once.

Table A-8 QADC64 (Queued Analog-to-Digital Converter)

Address	Access	Symbol	Register	Size	Reset
QADC_A (Note: Bit descriptions apply to QADC_B as well)					
0x30 4800	S	QADC64MCR_A	QADC64 Module Configuration Register. See **Table 13-7** for bit descriptions.	16	S
0x30 4802	T	QADC64TEST_A	QADC64 Test Register	16	—
0x30 4804	S	QADC64INT_A	Interrupt Register. See **Table 13-8** for bit descriptions.	16	S
0x30 4806	S/U	PORTQA_A/ PORTQB_A	Port A and Port B Data. See **Table 13-9** for bit descriptions.	16	U
0x30 4808	S/U	DDRQA_A/ DDRQB_A	Port A Data and Port B Direction Register. See **Table 13-10** for bit descriptions.	16	S
0x30 480A	S/U	QACR0_A	QADC64 Control Register 0. See **Table 13-11** for bit descriptions.	16	S
0x30 480C	S/U[1]	QACR1_A	QADC64 Control Register 1. See **Table 13-12** for bit descriptions.	16	S
0x30 480E	S/U[1]	QACR2_A	QADC64 Control Register 2. See **Table 13-14** for bit descriptions.	16	S
0x30 4810	S/U	QASR0_A	QADC64 Status Register 0. See **Table 13-16** for bit descriptions.	16	S
0x30 4812	S/U	QASR1_A	QADC64 Status Register 1. See **Table 13-18** for bit descriptions.	16	S
0x30 4814 – 0x30 49FE	—	—	Reserved	—	—

Table A-8 QADC64 (Queued Analog-to-Digital Converter) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 4A00 – 0x30 4A7E	S/U	CCW_A	Conversion Command Word Table. See **Table 13-19** for bit descriptions.	16	U
0x30 4A80 – 0x30 4AFE	S/U	RJURR_A	Result Word Table Right-Justified, Unsigned Result Register. See **13.12.12** for bit descriptions.	16	X
0x30 4B00 – 0x30 4B7E	S/U	LJSRR_A	Result Word Table Left-Justified, Signed Result Register. See **13.12.12** for bit descriptions.	16	X
0x30 4B80 – 0x30 4BFE	S/U	LJURR_A	Result Word Table Left-Justified, Unsigned Result Register. See **13.12.12** for bit descriptions.	16	X
QADC_B					
0x30 4C00	S	QADC64MCR_B	QADC64 Module Configuration Register	16	S
0x30 4C02	T	QADC64TEST_B	QADC64 Test Register	16	—
0x30 4C04	S	QADC64INT_B	Interrupt Register	16	S
0x30 4C06	S/U	PORTQA_B/ PORTQB_B	Port A and Port B Data	16	U
0x30 4C08	S/U	DDRQA_B/ DDRQB_B	Port A Data and Port B Direction Register	16	S
0x30 4C0A	S/U	QACR0_B	QADC64 Control Register 0	16	S
0x30 4C0C	S/U[1]	QACR1_B	QADC64 Control Register 1	16	S
0x30 4C0E	S/U[1]	QACR2_B	QADC64 Control Register 2	16	S
0x30 4C10	S/U	QASR0_B	QADC64 Status Register 0	16	S
0x30 4C12	S/U	QASR1_B	QADC64 Status Register 1	16	S
0x30 4C14 – 0x30 4DFE	—	—	Reserved	—	—
0x30 4E00 – 0x30 4E7E	S/U	CCW_B	Conversion Command Word Table	16	U
0x30 4E80 – 0x30 4EFE	S/U	RJURR_B	Result Word Table. Right-Justified, Unsigned Result Register.	16	X
0x30 4F00 – 0x30 4F7E	S/U	LJSRR_B	Result Word Table. Left-Justified, Signed Result Register.	16	X
0x30 4F80 – 0x30 4FFE	S/U	LJURR_B	Result Word Table. Left-Justified, Unsigned Result Register.	16	X

NOTES:
1. Bit 3 (SSEx) is readable in test mode only.

Table A-9 QSMCM (Queued Serial Multi-Channel Module)

Address	Access	Symbol	Register	Size	Reset
0x30 5000	S	QSMCMMCR	QSMCM Module Configuration Register. See **Table 14-4** for bit descriptions.	16	S
0x30 5002	T	QTEST	QSMCM Test Register	16	S
0x30 5004	S	QDSCI_IL	Dual SCI Interrupt Level. See **Table 14-5** for bit descriptions.	16	S
0x30 5006	S	QSPI_IL	Queued SPI Interrupt Level. See **Table 14-6** for bit descriptions.	16	S
0x30 5008	S/U	SCC1R0	SCI1Control Register 0. See **Table 14-23** for bit descriptions.	16	S
0x30 500A	S/U	SCC1R1	SCI1Control Register 1. See **Table 14-24** for bit descriptions.	16	S

Table A-9 QSMCM (Queued Serial Multi-Channel Module) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 500C	S/U	SC1SR	SCI1 Status Register. See **Table 14-25** for bit descriptions.	16	S
0x30 500E	S/U	SC1DR	SCI1 Data Register. See **Table 14-26** for bit descriptions.	16	S
0x30 5010 — 0x30 5012	—	—	Reserved	—	—
0x30 5014	S/U	PORTQS	QSMCM Port QS Data Register. See **14.6.1 Port QS Data Register (PORTQS)** for bit descriptions.	16	S
0x30 5016	S/U	PQSPAR/ DDRQST	QSMCM Port QS PIn Assignment Register/ QSMCM Port QS Data Direction Register. See **Table 14-11** for bit descriptions.	16	S
0x30 5018	S/U	SPCR0	QSPI Control Register 0. See **Table 14-13** for bit descriptions.	16	S
0x30 501A	S/U	SPCR1	QSPI Control Register 1. See **Table 14-15** for bit descriptions.	16	S
0x30 501C	S/U	SPCR2	QSPI Control Register 2. See **Table 14-16** for bit descriptions.	16	S
0x30 501E	S/U	SPCR3	QSPI Control Register 3. See **Table 14-17** for bit descriptions.	8	S
0x30 501F	S/U	SPSR	QSPI Status Register 3. See **Table 14-18** for bit descriptions.	8	S
0x30 5020	S/U	SCC2R0	SCI2 Control Register 0	16	S
0x30 5022	S/U	SCC2R1	SCI2 Control Register 1	16	S
0x30 5024	S/U	SC2SR	SCI2 Status Register	16	S
0x30 5026	S/U	SC2DR	SCI2 Data Register	16	S
0x30 5028	S/U[1]	QSCI1CR	QSCI1 Control Register. See **Table 14-33** for bit descriptions.	16	S
0x30 502A	S/U[2]	QSCI1SR	QSCI1 Status Register. See **Table 14-34** for bit descriptions.	16	S
0x30 502C – 0x30 504A	S/U	SCTQ	Transmit Queue Locations	16	S
0x30 504C – 0x30 506A	S/U	SCRQ	Receive Queue Locations	16	S
0x30 506C – 0x30 5013F	—	—	Reserved	—	—
0x30 5140 – 0x30 517F	S/U	RECRAM	Receive Data RAM	16	S
0x30 5180 – 0x30 51BF	S/U	TRAN.RAM	Transmit Data RAM	16	S
0x30 51C0 – 0x30 51DF	S/U	COMD.RAM	Command RAM	16	S

NOTES:
1. Bits 0–3 writeable only in test mode, otherwise read only.
2. Bits 3–11 writeable only in test mode, otherwise read only.

Table A-10 MIOS1 (Modular Input/Output Subsystem)

Address	Access	Symbol	Register	Size	Reset
MPWMSM0 (MIOS Pulse Width Modulation Submodule 0)					
0x30 6000	S/U	MPWMSMPERR	MPWMSM0 Period Register. See **Table 15-20** for bit descriptions.	16	X
0x30 6002	S/U	MPWMSMPULR	MPWMSM0 Pulse Register. See **Table 15-21** for bit descriptions.	16	X
0x30 6004	S/U	MPWMSMCNTR	MPWMSM0 Count Register. See **Table 15-22** for bit descriptions.	16	X
0x30 6006	S/U	MPWMSMSCR	MPWMSM0 Status/Control Register. See **Table 15-23** for bit descriptions.	16	S
MPWMSM1 (MIOS Pulse Width Modulation Submodule 1)					
0x30 6008	S/U	MPWMSMPERR	MPWMSM1 Period Register. See **Table 15-20** for bit descriptions.	16	X
0x30 600A	S/U	MPWMSMPULR	MPWMSM1 Pulse Register. See **Table 15-21** for bit descriptions.	16	X
0x30 600C	S/U	MPWMSMCNTR	MPWMSM1 Count Register. See **Table 15-22** for bit descriptions.	16	X
0x30 600E	S/U	MPWMSMSCR	MPWMSM1 Status/Control Register. See **Table 15-23** for bit descriptions.	16	S
MPWMSM2 (MIOS Pulse Width Modulation Submodule 2)					
0x30 6010	S/U	MPWMSMPERR	MPWMSM2 Period Register. See **Table 15-20** for bit descriptions.	16	X
0x30 6012	S/U	MPWMSMPULR	MPWMSM2 Pulse Register. See **Table 15-21** for bit descriptions.	16	X
0x30 6014	S/U	MPWMSMCNTR	MPWMSM2 Count Register. See **Table 15-22** for bit descriptions.	16	X
0x30 6016	S/U	MPWMSMSCR	MPWMSM2 Status/Control Register. See **Table 15-23** for bit descriptions.	16	S
MPWMSM3 (MIOS Pulse Width Modulation Submodule 3)					
0x30 6018	S/U	MPWMSMPERR	MPWMSM3 Period Register. See **Table 15-20** for bit descriptions.	16	X
0x30 601A	S/U	MPWMSMPULR	MPWMSM3 Pulse Register. See **Table 15-21** for bit descriptions.	16	X
0x30 601C	S/U	MPWMSMCNTR	MPWMSM3 Count Register. See **Table 15-22** for bit descriptions.	16	X
0x30 601E	S/U	MPWMSMSCR	MPWMSM3 Status/Control Register. See **Table 15-23** for bit descriptions.	16	S
MMCSM6 (MIOS Modulus Counter Submodule 6)					
0x30 6030	S/U	MMCSMCNT	MMCSM6 Up-Counter Register. See **Table 15-12** for bit descriptions.	16	X
0x30 6032	S/U	MMCSMML	MMCSM6 Modulus Latch Register. See **Table 15-13** for bit descriptions.	16	X
0x30 6034	S/U	MMCSMSCRD	MMCSM6 Status/Control Register Duplicated. See **15.10.1.3 MMCSM Status/Control Register (Duplicated)** for bit descriptions.	16	S
0x30 6036	S/U	MMCSMSCR	MMCSM6 Status/Control Register. See **Table 15-14** for bit descriptions.	16	S
MDASM11 (MIOS Double Action Submodule 11)					
0x30 6058	S/U	MDASMAR	MDASM11 Data A Register. See **15.11.1.1 MDASM Data A Register** for bit descriptions.	16	X

Table A-10 MIOS1 (Modular Input/Output Subsystem) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 605A	S/U	MDASMBR	MDASM11 Data B Register. See **15.11.1.2 MDASM Data B Register (MDASMBR)** for bit descriptions.	16	X
0x30 605C	S/U	MDASMSCRD	MDASM11 Status/Control Register Duplicated. See **15.11.1.3 MDASM Status/Control Register (Duplicated)** for bit descriptions.	16	S
0x30 605E	S/U	MDASMSCR	MDASM11 Status/Control Register. See **Table 15-17** for bit descriptions.	16	S
MDASM12 (MIOS Double Action Submodule 12)					
0x30 6060	S/U	MDASMAR	MDASM12 Data A Register. See **15.11.1.1 MDASM Data A Register** for bit descriptions.	16	X
0x30 6062	S/U	MDASMBR	MDASM12 Data B Register. See **15.11.1.2 MDASM Data B Register (MDASMBR)** for bit descriptions.	16	X
0x30 6064	S/U	MDASMSCRD	MDASM12 Status/Control Register Duplicated. See **15.11.1.3 MDASM Status/Control Register (Duplicated)** for bit descriptions.	16	S
0x30 6066	S/U	MDASMSCR	MDASM12 Status/Control Register. See **Table 15-17** for bit descriptions.	16	S
MDASM13 (MIOS Double Action Submodule 13)					
0x30 6068	S/U	MDASMAR	MDASM13 Data A Register. See **15.11.1.1 MDASM Data A Register** for bit descriptions.	16	X
0x30 606A	S/U	MDASMBR	MDASM13 Data B Register. See **15.11.1.2 MDASM Data B Register (MDASMBR)** for bit descriptions.	16	X
0x30 606C	S/U	MDASMSCRD	MDASM13 Status/Control Register Duplicated. See **15.11.1.3 MDASM Status/Control Register (Duplicated)** for bit descriptions.	16	S
0x30 606E	S/U	MDASMSCR	MDASM13 Status/Control Register. See **Table 15-17** for bit descriptions.	16	S
MDASM14 (MIOS Double Action Submodule 14)					
0x30 6070	S/U	MDASMAR	MDASM14 Data A Register. See **15.11.1.1 MDASM Data A Register** for bit descriptions.	16	X
0x30 6072	S/U	MDASMBR	MDASM14 Data B Register. See **15.11.1.2 MDASM Data B Register (MDASMBR)** for bit descriptions.	16	X
0x30 6074	S/U	MDASMSCRD	MDASM14 Status/Control Register Duplicated. See **15.11.1.3 MDASM Status/Control Register (Duplicated)** for bit descriptions.	16	S
0x30 6076	S/U	MDASMSCR	MDASM14 Status/Control Register. See **Table 15-17** for bit descriptions.	16	S
MDASM15 (MIOS Double Action Submodule 15)					
0x30 6078	S/U	MDASMAR	MDASM15 Data A Register. See **15.11.1.1 MDASM Data A Register** for bit descriptions.	16	X
0x30 607A	S/U	MDASMBR	MDASM15 Data B Register. See **15.11.1.2 MDASM Data B Register (MDASMBR)** for bit descriptions.	16	X
0x30 607C	S/U	MDASMSCRD	MDASM15 Status/Control Register Duplicated. See **15.11.1.3 MDASM Status/Control Register (Duplicated)** for bit descriptions.	16	S

Table A-10 MIOS1 (Modular Input/Output Subsystem) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 607E	S/U	MDASMSCR	MDASM15 Status/Control Register. See **Table 15-17** for bit descriptions.	16	S
MPWMSM16 (MIOS Pulse Width Modulation Submodule 16)					
0x30 6080	S/U	MPWMSMPERR	MPWMSM16 Period Register. See **Table 15-20** for bit descriptions.	16	X
0x30 6082	S/U	MPWMSMPULR	MPWMSM16 Pulse Register. See **Table 15-21** for bit descriptions.	16	X
0x30 6084	S/U	MPWMSMCNTR	MPWMSM16 Count Register. See **Table 15-22** for bit descriptions.	16	X
0x30 6086	S/U	MPWMSMSCR	MPWMSM16 Status/Control Register. See **Table 15-23** for bit descriptions.	16	S
MPWMSM17 (MIOS Pulse Width Modulation Submodule 17)					
0x30 6088	S/U	MPWMSMPERR	MPWMSM17 Period Register. See **Table 15-20** for bit descriptions.	16	X
0x30 608A	S/U	MPWMSMPULR	MPWMSM17 Pulse Register. See **Table 15-21** for bit descriptions.	16	X
0x30 608C	S/U	MPWMSMCNTR	MPWMSM17 Count Register. See **Table 15-22** for bit descriptions.	16	X
0x30 608E	S/U	MPWMSMSCR	MPWMSM17 Status/Control Register. See **Table 15-23** for bit descriptions.	16	S
MPWMSM18 (MIOS Pulse Width Modulation Submodule 18)					
0x30 6090	S/U	MPWMSMPERR	MPWMSM18 Period Register. See **Table 15-20** for bit descriptions.	16	X
0x30 6092	S/U	MPWMSMPULR	MPWMSM18 Pulse Register. See **Table 15-21** for bit descriptions.	16	X
0x30 6094	S/U	MPWMSMCNTR	MPWMSM18 Count Register. See **Table 15-22** for bit descriptions.	16	X
0x30 6096	S/U	MPWMSMSCR	MPWMSM18 Status/Control Register. See **Table 15-23** for bit descriptions.	16	S
MPWMSM19 (MIOS Pulse Width Modulation Submodule 19)					
0x30 6098	S/U	MPWMSMPERR	MPWMSM19 Period Register. See **Table 15-20** for bit descriptions.	16	X
0x30 609A	S/U	MPWMSMPULR	MPWMSM19 Pulse Register. See **Table 15-21** for bit descriptions.	16	X
0x30 609C	S/U	MPWMSMCNTR	MPWMSM19 Count Register. See **Table 15-22** for bit descriptions.	16	X
0x30 609E	S/U	MPWMSMSCR	MPWMSM19 Status/Control Register. See **Table 15-23** for bit descriptions.	16	S
MMCSM22 (MIOS Modulus Counter Submodule 22)					
0x30 60B0	S/U	MMCSMCNT	MMCSM Up-Counter Register. See **Table 15-12** for bit descriptions.	16	X
0x30 60B2	S/U	MMCSMML	MMCSM Modulus Latch Register. See **Table 15-12** for bit descriptions.	16	X
0x30 60B4	S/U	MMCSMSCRD	MMCSM Status/Control Register Duplicated. See **15.10.1.3 MMCSM Status/Control Register (Duplicated)** for bit descriptions.	16	S
0x30 60B6	S/U	MMCSMSCR	MMCSM Status/Control Register. See **Table 15-14** for bit descriptions.	16	S
MDASM27 (MIOS Double Action Submodule 27)					
0x30 60D8	S/U	MDASMAR	MDASM27 Data A Register. See **15.11.1.1 MDASM Data A Register** for bit descriptions.	16	X

Table A-10 MIOS1 (Modular Input/Output Subsystem) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 60DA	S/U	MDASMBR	MDASM27 Data B Register. See **15.11.1.2 MDASM Data B Register (MDASMBR)** for bit descriptions.	16	X
0x30 60DC	S/U	MDASMSCRD	MDASM27 Status/Control Register Duplicated. See **15.11.1.3 MDASM Status/Control Register (Duplicated)** for bit descriptions.	16	S
0x30 60DE	S/U	MDASMSCR	MDASM27 Status/Control Register. See **Table 15-17** for bit descriptions.	16	S
MDASM28 (MIOS Double Action Submodule 28)					
0x30 60E0	S/U	MDASMAR	MDASM28 Data A Register. See **15.11.1.1 MDASM Data A Register** for bit descriptions.	16	X
0x30 60E2	S/U	MDASMBR	MDASM28 Data B Register. See **15.11.1.2 MDASM Data B Register (MDASMBR)** for bit descriptions.	16	X
0x30 60E4	S/U	MDASMSCRD	MDASM28 Status/Control Register Duplicated. See **15.11.1.3 MDASM Status/Control Register (Duplicated)** for bit descriptions.	16	S
0x30 60E6	S/U	MDASMSCR	MDASM28 Status/Control Register. See **Table 15-17** for bit descriptions.	16	S
MDASM29 (MIOS Double Action Submodule 29)					
0x30 60E8	S/U	MDASMAR	MDASM29 Data A Register. See **15.11.1.1 MDASM Data A Register** for bit descriptions.	16	X
0x30 60EA	S/U	MDASMBR	MDASM29 Data B Register. See **15.11.1.2 MDASM Data B Register (MDASMBR)** for bit descriptions.	16	X
0x30 60EC	S/U	MDASMSCRD	MDASM29 Status/Control Register Duplicated. See **15.11.1.3 MDASM Status/Control Register (Duplicated)** for bit descriptions.	16	S
0x30 60EE	S/U	MDASMSCR	MDASM29 Status/Control Register. See **Table 15-17** for bit descriptions.	16	S
MDASM30 (MIOS Double Action Submodule 30)					
0x30 60F0	S/U	MDASMAR	MDASM30 Data A Register. See **15.11.1.1 MDASM Data A Register** for bit descriptions.	16	X
0x30 60F2	S/U	MDASMBR	MDASM30 Data B Register. See **15.11.1.2 MDASM Data B Register (MDASMBR)** for bit descriptions.	16	X
0x30 60F4	S/U	MDASMSCRD	MDASM30 Status/Control Register Duplicated. See **15.11.1.3 MDASM Status/Control Register (Duplicated)** for bit descriptions.	16	S
0x30 60F6	S/U	MDASMSCR	MDASM30 Status/Control Register. See **Table 15-17** for bit descriptions.	16	S
MDASM31 (MIOS Double Action Submodule 31)					
0x30 60F8	S/U	MDASMAR	MDASM31 Data A Register. See **15.11.1.1 MDASM Data A Register** for bit descriptions.	16	X
0x30 60FA	S/U	MDASMBR	MDASM31 Data B Register. See **15.11.1.2 MDASM Data B Register (MDASMBR)** for bit descriptions.	16	X
0x30 60FC	S/U	MDASMSCRD	MDASM31 Status/Control Register Duplicated. See **15.11.1.3 MDASM Status/Control Register (Duplicated)** for bit descriptions.	16	S

Table A-10 MIOS1 (Modular Input/Output Subsystem) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 60FE	S/U	MDASMSCR	MDASM31 Status/Control Register. See **Table 15-17** for bit descriptions.	16	S
MPIOSM (MIOS 16-bit Parallel Port I/O Submodule)					
0x30 6100	S/U	MPIOSMDR	MPIOSM Data Register. See **Table 15-26** for bit descriptions.	16	X
0x30 6102	S/U	MPIOSMDDR	MPIOSM Data Direction Register. See **Table 15-27** for bit descriptions.	16	S
0x30 6104 — 0x30 6106	S/U	—	Reserved	—	—
MBISM (MIOS Bus Interface Submodule)					
0x30 6800	S[1]	MIOS1TPCR	MIOS1 Test and Pin Control Register. See **Table 15-3** for bit descriptions.	16	S
0x30 6802	S	—	Reserved	—	—
0x30 6804	S, read only	MIOS1VNR	MIOS1 Module Version Number Register. See **Table 15-4** for bit descriptions.	16	X
0x30 6806	S	MIOS1MCR	MIOS1 Module Control Register. See **Table 15-4** for bit descriptions.	16	S
0x30 6808 – 0x30 680E	S	—	Reserved	—	—
MCPSM (MIOS Counter Prescaler Submodule)					
0x30 6810 – 0x30 6814	S	—	Reserved	—	S
0x30 6816	S	MCPSMSCR	MCPSM Status/Control Register. See **Table 15-10** for bit descriptions.	16	S
MIRSM0 (MIOS Interrupt Request Submodule 0)					
0x30 6C00	S	MIOS1SR0	MIRSM0 Interrupt Status Register. See **Table 15-29** for bit descriptions.	16	X
0x30 6C02	S	—	Reserved	—	—
0x30 6C04	S	MIOS1ER0	MIRSM0 Interrupt Enable Register. See **Table 15-30** for bit descriptions.	16	S
0x30 6C06	S, read only	MIOS1RPR0	MIRSM0 Request Pending Register. See **Table 15-31** for bit descriptions.	16	S
MIRSM (MIOS Interrupt Request Submodule)					
0x30 6C30	S	MIOS1LVL0	MIOS1 Interrupt Level Register 0. See **Table 15-7** for bit descriptions.	16	S
MIRSM1 (MIOS Interrupt Request Submodule 1)					
0x30 6C40	S	MIOS1SR1	MIRSM1 Interrupt Status Register. See **Table 15-33** for bit descriptions.	16	X
0x30 6C42	S	—	Reserved	—	—
0x30 6C44	S	MIOS1ER1	MIRSM1 Interrupt Enable Register. See **Table 15-34** for bit descriptions.	16	S
0x30 6C46	S, read only	MIOS1RPR1	MIRSM1 Request Pending Register. See **Table 15-35** for bit descriptions.	16	S
MIRSM (MIOS Interrupt Request Submodule)					
0x30 6C70	S	MIOS1LVL1	MIOS1 Interrupt Level Register 1. See **Table 15-8** for bit descriptions.	16	S

NOTES:
1. Bit 0 (TEST) is reserved for factory testing.

Table A-11 TouCAN (CAN 2.0B Controller)

Address	Access	Symbol	Register	Size	Reset
TouCAN_A (Note: Bit descriptions apply to TouCAN_B as well)					
0x30 7080	S	TCNMCR_A	TouCAN_A Module Configuration Register. See **Table 16-11** for bit descriptions.	16	S
0x30 7082	T	TTR_A	TouCAN_A Test Register	16	S
0x30 7084	S	CANICR_A	TouCAN_A Interrupt Configuration Register. See **Table 16-12** for bit descriptions.	16	S
0x30 7086	S/U	CANCTRL0_A/ CANCTRL1_A	TouCAN_A Control Register 0/ TouCAN_A Control Register 1. See **Table 16-13** and **Table 16-16** for bit descriptions.	16	S
0x30 7088	S/U	PRESDIV_A/ CTRL2_A	TouCAN_A Control and Prescaler Divider Register/ TouCAN_A Control Register 2. See **Table 16-17** and **Table 16-18** for bit descriptions.	16	S
0x30 708A	S/U	TIMER_A	TouCAN_A Free-Running Timer Register. See **Table 16-19** for bit descriptions.		S
0x30 708C — 0x30 708E	—	—	Reserved	—	—
0x30 7090	S/U	RXGMASKHI_A	TouCAN_A Receive Global Mask High. See **Table 16-20** for bit descriptions.	16	S
0x30 7092	S/U	RXGMASKLO_A	TouCAN_A Receive Global Mask Low. See **Table 16-20** for bit descriptions.	16	S
0x30 7094	S/U	RX14MASKHI_A	TouCAN_A Receive Buffer 14 Mask High. See **16.7.10 Receive Buffer 14 Mask Registers** for bit descriptions.	16	S
0x30 7096	S/U	RX14MASKLO_A	TouCAN_A Receive Buffer 14 Mask Low. See **16.7.10 Receive Buffer 14 Mask Registers** for bit descriptions.	16	S
0x30 7098	S/U	RX15MASKHI_A	TouCAN_A Receive Buffer 15 Mask High. See **16.7.11 Receive Buffer 15 Mask Registers** for bit descriptions.	16	S
0x30 709A	S/U	RX15MASKLO_A	TouCAN_A Receive Buffer 15 Mask Low. See **16.7.11 Receive Buffer 15 Mask Registers** for bit descriptions.	16	S
0x30 709C — 0x30 709E	—	—	Reserved	—	—
0x30 70A0	S/U	ESTAT_A	TouCAN_A Error and Status Register. See **Table 16-21** for bit descriptions.	16	S
0x30 70A2	S/U	IMASK_A	TouCAN_A Interrupt Masks. See **Table 16-24** for bit descriptions.	16	S
0x30 70A4	S/U	IFLAG_A	TouCAN_A Interrupt Flags. See **Table 16-25** for bit descriptions.	16	S
0x30 70A6	S/U	RXECTR_A/ TXECTR_A	TouCAN_A Receive Error Counter/ TouCAN_A Transmit Error Counter. See **Table 16-26** for bit descriptions.	16	S
0x307100 — 0x30710F	S/U	MBUFF0_A	TouCAN_A Message Buffer 0. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x307110 — 0x30711F	S/U	MBUFF1_A	TouCAN_A Message Buffer 1. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U

Table A-11 TouCAN (CAN 2.0B Controller) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x307120 — 0x30712F	S/U	MBUFF2_A	TouCAN_A Message Buffer 2. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x307130 — 0x30713F	S/U	MBUFF3_A	TouCAN_A Message Buffer 3. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x307140 — 0x30714F	S/U	MBUFF4_A	TouCAN_A Message Buffer 4. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x307150 — 0x30715F	S/U	MBUFF5_A	TouCAN_A Message Buffer 5. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x307160 — 0x30716F	S/U	MBUFF6_A	TouCAN_A Message Buffer 6. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x307170 — 0x30717F	S/U	MBUFF7_A	TouCAN_A Message Buffer 7. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x307180 — 0x30718F	S/U	MBUFF8_A	TouCAN_A Message Buffer 8. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x307190 — 0x30719F	S/U	MBUFF9_A	TouCAN_A Message Buffer 9. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x3071A0 — 0x3071AF	S/U	MBUFF10_A	TouCAN_A Message Buffer 10. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x3071B0 — 0x3071BF	S/U	MBUFF11_A	TouCAN_A Message Buffer 11. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x3071C0 — 0x3071CF	S/U	MBUFF12_A	TouCAN_A Message Buffer 12. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x3071D0 — 0x3071DF	S/U	MBUFF13_A	TouCAN_A Message Buffer 13. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x3071E0 — 0x3071EF	S/U	MBUFF14_A	TouCAN_A Message Buffer 14. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
0x3071F0 — 0x3071FF	S/U	MBUFF15_A	TouCAN_A Message Buffer 15. See **Figure 16-3** and **Figure 16-4** for message buffer definitions.	—	U
TouCAN_B					
0x30 7480	S	TCNMCR_B	TouCAN_B Module Configuration Register	16	S
0x30 7482	T	TTR_B	TouCAN_B Test Register	16	S
0x30 7484	S	CANICR_B	TouCAN_B Interrupt Configuration Register	16	S
0x30 7486	S/U	CANCTRL0_B/ CANCTRL1_B	TouCAN_B Control Register 0/ TouCAN_B Control Register 1	16	S
0x30 7488	S/U	PRESDIV_B/ CTRL2_B	TouCAN_B Control and Prescaler Divider Register/ TouCAN_B Control Register 2	16	S
0x30 748A	S/U	TIMER_B	TouCAN_B Free-Running Timer Register		S
0x30 748C — 0x30 748E	—	—	Reserved	—	—
0x30 7490	S/U	RXGMASKHI_B	TouCAN_B Receive Global Mask High	16	S

Table A-11 TouCAN (CAN 2.0B Controller) (Continued)

Address	Access	Symbol	Register	Size	Reset
0x30 7492	S/U	RXGMASKLO_B	TouCAN_B Receive Global Mask Low	16	S
0x30 7494	S/U	RX14MASKHI_B	TouCAN_B Receive Buffer 14 Mask High	16	S
0x30 7496	S/U	RX14MASKLO_B	TouCAN_B Receive Buffer 14 Mask Low	16	S
0x30 7498	S/U	RX15MASKHI_B	TouCAN_B Receive Buffer 15 Mask High	16	S
0x30 749A	S/U	RX15MASKLO_B	TouCAN_B Receive Buffer 15 Mask Low	16	S
0x30 749C — 0x30 749E	—	—	Reserved	—	—
0x30 74A0	S/U	ESTAT_B	TouCAN_B Error and Status Register	16	S
0x30 74A2	S/U	IMASK_B	TouCAN_B Interrupt Masks	16	S
0x30 74A4	S/U	IFLAG_B	TouCAN_B Interrupt Flags	16	S
0x30 74A6	S/U	RXECTR_B/ TXECTR_B	TouCAN_B Receive Error Counter/ TouCAN_B Transmit Error Counter	16	S
0x307500 — 0x30750F	S/U	MBUFF0_B	TouCAN_B Message Buffer 0.	—	U
0x307510 — 0x30751F	S/U	MBUFF1_B	TouCAN_B Message Buffer 1.	—	U
0x307520 — 0x30752F	S/U	MBUFF2_B	TouCAN_A Message Buffer 2.	—	U
0x307530 — 0x30753F	S/U	MBUFF3_B	TouCAN_B Message Buffer 3.	—	U
0x307540 — 0x30754F	S/U	MBUFF4_B	TouCAN_B Message Buffer 4.	—	U
0x307550 — 0x30755F	S/U	MBUFF5_B	TouCAN_B Message Buffer 5.	—	U
0x307560 — 0x30756F	S/U	MBUFF6_B	TouCAN_B Message Buffer 6.	—	U
0x307570 — 0x30757F	S/U	MBUFF7_B	TouCAN_B Message Buffer 7.	—	U
0x307580 — 0x30758F	S/U	MBUFF8_B	TouCAN_B Message Buffer 8.	—	U
0x307590 — 0x30759F	S/U	MBUFF9_B	TouCAN_B Message Buffer 9.	—	U
0x3075A0 — 0x3075AF	S/U	MBUFF10_B	TouCAN_B Message Buffer 10.	—	U
0x3075B0 — 0x3075BF	S/U	MBUFF11_B	TouCAN_B Message Buffer 11.	—	U
0x3075C0 — 0x3075CF	S/U	MBUFF12_B	TouCAN_B Message Buffer 12.	—	U
0x3075D0 — 0x3075DF	S/U	MBUFF13_B	TouCAN_B Message Buffer 13.	—	U
0x3075E0 — 0x3075EF	S/U	MBUFF14_B	TouCAN_B Message Buffer 14.	—	U
0x3075F0 — 0x3075FF	S/U	MBUFF15_B	TouCAN_B Message Buffer 15.	—	U

Table A-12 UIMB (U-Bus to IMB3 Bus Interface)

Address	Access	Symbol	Register	Size	Reset
0x30 7F80	S[1]	UMCR	UIMB Module Configuration Register. See **Table 12-6** for bit descriptions.	32	H
0x30 7F90	S/T	UTSTCREG	Test Register — Reserved	32	—
0x30 7FA0	S, read only	UIPEND	Pending Interrupt Request Register. See **Table 12-7** for bit descriptions.	32	H

NOTES:
1. Bit 3 (HSPEED) is write-once.

Table A-13 SRAM (Static RAM Access Memory)

Address	Access	Symbol	Register	Size	Reset
SRAM_A					
0x38 0000	S[1]	SRAMMCR_A	SRAM_A Module Configuration Register. See **Table 20-1** for bit descriptions.	16	S,H, POR
0x38 0004	T	SRAMTST_A	SRAM_A Test Register.	16	S,H, POR
SRAM_B					
0x38 0008	S[1]	SRAMMCR_B	SRAM_B Module Configuration Register. See **Table 20-1** for bit descriptions.	16	S,H, POR
0x38 000C	T	SRAMTST_B	SRAM_B Test Register.	16	S,H, POR

NOTES:
1. Bit 0 (LCK) locks the register (write-protected except in test mode) and is write once.

Table A-14 SRAM (Static RAM Access Memory) Array

Address	Access	Symbol	Register	Size	Reset
0x3F 8000 — 0x3F 97FF	—		Reserved	—	—
0x3F 9800 — 0x3F BFFF	U, S		SRAM_A RAM Array (10 K Bytes)	8, 16, 32	—
0x3F C000 — 0x3F FFFF	U, S		SRAM_B RAM Array (16 K Bytes)	8, 16, 32	—