



APPENDIX B REGISTER GENERAL INDEX

-A-

Associated registers 10-4

-B-

BAR (breakpoint address register) 21-46

BBC

global region attribute register description (MI_GRA) 4-11

module configuration register (BBCMCR) 4-12

region attribute registers MI_RAx description (MI_RAx) 4-10

region base address registers (MI_RBx) 4-10

BBCMCR (BBC module configuration register) 4-12

BR0 (BR3 - memory controller base registers 0 - 3) 10-28

Breakpoint address register (BAR) 21-46

Breakpoint counter A value and control register (COUNTA) 21-52

Breakpoint counter B value and control register (COUNTB) 21-53

-C-

CANCTRL0 (control register 0) 16-25

CANCTRL1 (control register 1) 16-26

CANCTRL2 (control register 2) 16-28

CANICR (TouCAN interrupt configuration register) 16-24

CANMCR (TouCAN module configuration register) 16-22

CCW (conversion command word table) 13-45

CFSR0 (TPU3 channel function select register 0) 17-16

CFSR1 (TPU3 channel function select register 1) 17-16

CFSR2 (TPU3 channel function select register 2) 17-16

CFSR3 (TPU3 channel function select register 3) 17-16

CIER (TPU3 channel interrupt enable register) 17-15

CISR (TPU3 channel interrupt status register) 17-19

CMF

EEPROM configuration register (CMFMCR) 19-5

EEPROM control registers 19-4

EEPROM high voltage control register (CMFCTL) 19-8

CMFCFIG (hard reset configuration word) 19-16

CMFCTL (CMF EEPROM high voltage control register) 19-7, 19-8

CMFMCR (CMF EEPROM configuration register) 19-5

CMPA-CMPD (comparator A-D value register) 21-45

CMPE-CMPF (comparator E-F value registers) 21-46

CMPG-CMPH (comparator G-H value registers) 21-47

COLIR

change of lock interrupt register 8-34

COLIR (change of lock register) 8-34

Comparator A-D value registers (CMPA-CMPD) 21-45

Comparator E-F value registers (CMPE-CMPF) 21-46

Comparator G-H value registers (CMPG-CMPH) 21-47

COUNTA (breakpoint counter A value and control register) 21-52

COUNTB (breakpoint counter B value and control register) 21-53

CPR0 (TPU3 channel priority register 0) 17-18

CPR1 (TPU3 channel priority register 1) 17-18

CR (condition register) 3-17
CTR (count register) 3-20



-D-

DAR (data address register) 3-23
DDRQA (port QA data direction register) 13-34
DDRQS (PORTQS data direction register) 14-12
Debug enable register (DER) 21-55
DEC (decrementer register) 3-25, 6-29
Decrementer register (DEC) 6-29
DER (debug enable register) 21-55
Development port data register (DPDR) 21-57
DMBR (dual mapping base register) 10-32
DMOR (dual mapping option register) 10-33
DPTMCR (DPTRAM module configuration register) 18-3
DPTRAM
 module configuration register (DPTMCR) 18-3
 ram base address register (RAMBAR) 18-4
 test register 18-4
DSCR (TPU3 development support control register) 17-12
DSISR (dae/source instruction service register) 3-23
DSSR (TPU3 development support status register) 17-14
Dual mapping base register (DMBR) 10-32
Dual mapping option register 10-33

-E-

ECR (exception cause register) 21-54
EMCR (external master control register) 6-23
ESTAT (error and status register) 16-30
Exception cause register (ECR) 21-53
External master control register (EMCR) 6-23

-F-

FPRs - (floating-point registers) 3-13
FPSCR (floating-point status and control register) 3-14

-G-

General-Purpose I/O registers 6-35
GPRs (general-purpose registers) 3-13

-H-

HSQR0 (TPU3 host sequence register 0) 17-17
HSQR1 (TPU3 host sequence register 1) 17-17
HSSR0 (TPU3 host service request register 0) 17-17
HSSR1 (TPU3 host service request register 1) 17-18

-I-

I-Bus support control register (ICTRL) 21-47
ICTRL (i-bus support control register) 21-47
IFLAG (interrupt flag register) 16-32
IMASK (interrupt mask register) 16-32
IMMR (internal memory mapping register) 6-22
Internal memory map register 6-22

-K-

Keep alive power registers lock mechanism 8-23



L2U

- global region attribute register (L2U_GRA) 11-15
- module configuration register (L2U_MCR) 11-13
- region attribute registers (L2U_RAx) 11-15
- region base address registers (L2U_RBAX) 11-14
- L2U_GRA (L2U global region attribute register) 11-16
- L2U_MCR (L2U module configuration register) 11-13
- L2U_RAx (L2U region X attribute register) 11-15
- L2U_RBAX (L2U region x base address register) 11-14
- L-Bus support control register 1 (LCTRL1) 21-49
- L-Bus support control register 2 (LCTRL2) 21-50
- LCTRL1 (l-bus support control register 1) 21-49
- LCTRL2 (l-bus support control register 2) 21-50
- LJSRR (left justified, signed result register) 13-48
- LJURR (left justified, unsigned result register) 13-49
- LR (link register) 3-20

MBISM

- interrupt registers 15-10

MCPSM

- status/control register (MCPSMCSR) 15-13

MCPSMCSR (MCPSM status/control register) 15-13

MDASM

- data A register (MDASMAR) 15-22

- data B register (MDASMBR) 15-22

- status/control register - duplicated (MDASMSCRD) 15-23

- status/control register (MDASMSCR) 15-24

MDASMAR (MDASM data A register) 15-22

MDASMBR (MDASM data B register) 15-23

MDASMSCR (MDASM status/control register) 15-24

MDASMSCRD (MDASM status/control register - duplicated) 15-23

Memory controller base registers (BR0 - BR3) 10-28

Memory controller option registers (OR0 - OR3) 10-30

Memory controller status registers (MSTAT) 10-28

MI_GRA (global region attribute register) 4-11

MIOS

- 16-bit parallel port I/O submodule (MPIOISM) Registers 15-32

- bus interface (MBISM) Registers 15-8

- counter prescaler submodule (MCPSM) Registers 15-12

- double action submodule (MDASM) Registers 15-20

- interrupt request submodule 0 (MIRSM0) Registers 15-35

- interrupt request submodule 1 (MIRSM1) Registers 15-38

- modulus counter submodule (MMCSM) Registers 15-15

- pulse width modulation submodule (MPWMSM) Registers 15-28

MIOS1

- interrupt level register 0 (MIOSLVL0) (MIOS1LVL0) 15-10

- interrupt level register 1 (MIOSLVL1) (MIOS1LVL1) 15-11

- module and version number register (MIOS1VNR) 15-9

- module configuration register (MIOS1MCR) 15-9

- test and pin control register 15-8

- vector register 15-9

MIOS1ER0 (MIRSM0 interrupt enable register) 15-37

MIOS1ER1 (interrupt enable register) 15-39

MIOS1LVL0 (MIOS1 interrupt level register 0) 15-11

MIOS1LVL1 (MIOS1 interrupt level 1 register) 15-11

MIOS1MCR (MIOS1 module configuration register) 15-9

MIOS1RPR0 (MIRSM0 request pending register) 15-37



MIOS1RPR1 (MIRSM1 request pending register) 15-40
MIOS1SR0 (MIRSM0 interrupt status register) 15-36
MIOS1SR1 (MIRSM1 interrupt status register) 15-38
MIOS1TPCR ((test and pin control register) 15-8
MIOS1VNR (MIOS1 module/version number register) 15-9
MIRSM0
 interrupt enable register (MIOS1ER0) 15-37
 interrupt status register (MIOS1SR0) 15-36
 request pending register (MIOS1RPR0) 15-37
MIRSM1
 interrupt enable register (MIOS1ER1) 15-39
 interrupt status register (MIOS1SR1) 15-38
 request pending register (MIOS1RPR1) 15-40
MISCNT (MISC counter) 18-6
MISRH (multiple input signature register high) 18-5
MISRL (multiple input signature register low) 18-5
MMCSM
 modulus latch register (MMCSMML) 15-16
 status/control register - duplicated (MMCSMSCRD) 15-16
 status/control register (MMCSMSCR) 15-17
 up-counter register (MMCSMCNT) 15-16
MMCSMCNT (MMCSM up-counter register) 15-16
MMCSMML (MMCSM modulus latch register) 15-16
MMCSMSCR (MMCSM status/control register) 15-17
MMCSMSCRD (MMCSM status/control register - duplicated) 15-17
MPIO SM
 data direction register (MPIO SMDDR) 15-33
 data register (MPIO SMDR) 15-32
MPIO SMDDR (MPIO SM data direction register) 15-33
MPIO SMDR (MPIO SM data register) 15-33
MPWMSM
 counter register (MPWMSMCNTR) 15-30
 period register (MPWMSMPERR) 15-29
 pulse width register (MPWMSMPULR) 15-29
 status/control register (MPWMSMCR) 15-30
MPWMSMCNTR (MPWMSM counter register) 15-30
MPWMSMPERR (MPWMSM period register) 15-29
MPWMSMPULR (MPWMSM pulse width register) 15-29
MPWMSMCR (MPWMSM status/control register) 15-30
MSR (machine state register) 3-21
MSTAT (memory controller status register) 10-28

—O—

OR0 (OR3 - memory controller option registers 0 - 3) 10-30

—P—

PDMCR (Pad module configuration register) 2-30
Periodic interrupt status and control register (PISCR) 6-33
Periodic interrupt timer count register (PITC) 6-33
Periodic interrupt timer register (PITR) 6-34
PISCR (periodic interrupt status and control register) 6-33
PITC (periodic interrupt timer count) 6-33
PITR (periodic interrupt timer register) 6-34
PLL,
 low power, and reset control register (PLPRCR) 8-32
PLPRCR (PLL, low power, and reset control register) 8-32
PORTQA (port QA data register) 13-33
PORTQB (port QB data register) 13-33
PORTQS (port QS data register) 14-10

PQSPAR (PORTQS pin assignment register) 14-11
PRESDIV (prescaler divide register) 16-27
PVR (processor version register) 3-26



–Q–

QACR0 (QADC64 control register 0) 13-34
QACR1 (QADC64 control register 1) 13-35
QACR2 (QADC64 control register 2) 13-38
QADC64
 control register 0 (QACR0) 13-34
 control register 1 (QADC64CR1) 13-35
 control register 2 (QADC64CR2) 13-38
 interrupt register (QADC64INT) 13-32
 module configuration register (QADC64MCR) 13-32
 port A/B data register (PORTQA/B) 13-33
 port data direction register (DDRQA) 13-34
 status register 0 (QADC64SR0) 13-39
 status register 1 (QADC64SR1) 13-41
 successive approximation register (SAR) 13-14
 test register (QADC64TEST) 13-32
QADC64INT (QADC64 interrupt register) 13-32
QADC64MCR (QADC64 module configuration register) 13-32
QASR0 (QADC64 status register 0) 13-40, 13-41
QDSCI_IL (QSM2 dual SCI interrupt level register) 14-8
QSCI1CR (QSCI1 control register) 14-60
QSCI1SR (QSCI1 status register) 14-62
QSMCM
 configuration register (QMCR) 14-7
 interrupt level registers (QDSCI_IL, QSPI_IL) 14-8
 port QS data register (PORTQS) 14-10
 PORTQS data direction register (DDRQS) 14-12
 PORTQS pin assignment register (PQSPAR) 14-11
 QSCI1 control register (QSCI1CR) 14-60
 QSCI1 status register (QSCI1SR) 14-62
 QSPI command RAM (CRx) 14-22
 QSPI control register 0 (SPCR0) 14-16
 QSPI control register 1 (SPCR1) 14-17
 QSPI control register 2 (SPCR2) 14-18
 QSPI control register 3 (SPCR3) 14-19
 QSPI registers 14-15
 QSPI status register (SPSR) 14-20
 queued SCI1 status and control registers 14-60
 SCI control register 0 (SCCxR0) 14-45
 SCI control register 1 (SCCxR1) 14-45
 SCI data register (SCxDR) 14-49
 SCI registers 14-44
 SCI status register (SCxSR) 14-47
 test register (QTEST) 14-8
QSMCMCR (QSMCM module configuration register) 14-7
QSPI_IL (QSPI interrupt level register) 14-9

–R–

RAMBAR (ram array base address register) 18-5
RCPU
 additional implementation-specific registers 3-28
 condition register (CR) 3-16
 condition register CR0 field definition 3-17
 condition register CR1 field definition 3-17
 condition register crn field - compare instruction 3-18



count register (CTR) 3-20
dae/source instruction service register (DSISR) 3-23
data address register (DAR) 3-23
decrementer register (DEC) 3-24
EIE, EID, and NRI special-purpose registers 3-27
floating-point exception cause register (FPECR) 3-27
floating-point registers (FPRs) 3-13
floating-point status and control register (FPSCR) 3-13
general special-purpose registers (SPRG0-SPRG3) 3-26
general-purpose registers (GPRs) 3-13
implementation-specific special-purpose registers 3-27
integer exception register (XER) 3-18
link register (LR) 3-19
machine state register (MSR) 3-21
machine status save/restore register 0 (SRR0) 3-25
machine status save/restore register 1 (SRR1) 3-25
powerpc OEA register set 3-21
powerpc UISA register set 3-12
powerpc VEA register set - time base 3-20
processor version register (PVR) 3-26
Real-Time clock alarm register (RTCAL) 6-32
Real-Time clock register (RTC) 6-32
Real-Time clock status and control register (RTCSC) 6-31
Reset status register (RSR) 7-5
RJURR (right justified, unsigned result register) 13-48
RSR (reset status register) 7-5
RTC (real time clock alarm register) 6-32
RTC (real time clock register) 6-32
RTCSC (real time clock status and control register) 6-31
RXECTR (receive error counter) 16-33
RXGMSKHI (receive global mask register high) 16-29

-S-

SCCR (system clock control register) 8-29
SCCxR0 (QSMCM SCI control register 0) 14-45
SCCxR1 (QSMCM SCI control register 1) 14-46
SCDR (QSMCM SCI data register) 14-49
SCxSR (QSMCM SCIx status register) 14-47
SGPIO
 control register (SGPIOCR) 6-36
 data register 1 (SGPIODT1) 6-35
 data register 2 (SGPIODT2) 6-35
SGPIOCR (SGPIO control register) 6-36
SGPIODT1 (SGPIO data register 1) 6-35
SGPIODT2 (SGPIO data register 2) 6-35
SIEL (SIU interrupt edge level register) 6-26
SIMASK (SIU interrupt mask register) 6-25
SIPEND
 register (SIPEND) 6-24
SIPEND (SIU interrupt pending register) 6-25
SIU
 interrupt edge level register (SIEL) 6-26
 interrupt mask register (SIMASK) 6-25
 interrupt registers 6-24
 interrupt vector register (SIVEC) 6-26
 module configuration register (SIUMCR) 6-19
SIUMCR (SIU module configuration register) 6-19
SIVEC (SIU interrupt vector) 6-26
Software service register (SWSR) 6-27
SPCR0 (QSPI control register 0) 14-16



SPCR1 (QSPI control register 1) 14-18
SPCR2 (QSPI control register 2) 14-19
SPCR3 (QSPI control register) 14-19
SPRG0-SPRG3 (general special-purpose registers 0-3) 3-26
SPSR (QSPI status register) 14-20
SRAM
 module configuration register (SRAMMCR) 21-2
 test register (SRAMTST) 21-3
SRAMMCR (SRAM module configuration register) 21-3
SRR0 (machine status save/restore register 0) 3-25
SRR1 (machine status save/restore register 1) 3-25
SWSR (software service register) 6-28
SYPCR (system protection control register) 6-27
System clock control register (SCCR) 8-29
System configuration and protection registers 6-19
System configuration registers 6-19
System protection control register (SYPCR) 6-27
System protection registers 6-27
System timer registers 6-29

-T-

TB (time base) 3-20, 3-24, 6-30
TBREF0 (time base reference register 0) 6-30
TBREF1 (time base reference register 1) 6-30
TBSCR (time base control and status register) 6-31
TESR (transfer error status register) 6-28
TICR (TPU3 interrupt configuration register) 17-14
Time base control and status register (TBSCR) 6-30
Time base reference registers (TBREF0) 6-30
TIMER (free running timer register) 16-28
TouCAN
 control register 0 (CANCTRL0) 16-25
 control register 1 (CANCTRL1) 16-26
 control register 2 (CANCTRL2) 16-28
 error and status register (ESTAT) 16-30
 interrupt configuration register (CANICR) 16-24
 interrupt flag register (IFLAG) 16-32
 interrupt mask register (IMASK) 16-32
 module configuration register (CANMCR) 16-22
 prescaler divide register (PRES DIV) 16-27
 receive buffer 14 mask registers 16-29
 receive buffer 15 mask registers 16-29
 receive global mask registers (RXGMSKHI) 16-29
 receive mask registers 16-7
 test configuration register 16-24
TPU3
 channel function select registers (CFSRx) 17-15
 channel interrupt enable register (CIER) 17-15
 channel interrupt status register (CISR) 17-19
 channel priority registers (CPRx) 17-18
 decoded channel number register (DCNR) 17-19
 development support control register (DSCR) 17-12
 development support status register (DSSR) 17-14
 host sequence registers (HSQRx) 17-16
 host service request registers (HSSRx) 17-17
 interrupt configuration register (TICR) 17-14
 link register (LR) 17-19
 module configuration register (TPUMCR) 17-10
 module configuration register 2 (TPUMCR2) 17-20
 module configuration register 3 (TPUMCR3) 17-21



service grant latch register (SGLR) 17-19
test configuration register (TCR) 17-12
test registers (ISDR, ISCR) 17-22
TPUMCR (TPU3 module configuration register) 17-10
TPUMCR2 (TPU3 module configuration register 2) 17-20
TPUMCR3 (TPU3 module configuration register 3) 17-21
Transfer error status register (TESR) 6-28

-U-

UIMB

module configuration register (UMCR) 12-7
pending interrupt request register (UIPEND) 12-8
test control register (UTSTCREG) 12-8
UIPEND (UIMB pending interrupt request register) 12-8
UMCR (UIMB module configuration register) 12-7

-V-

VDDSRM

sensor register (VSRMSR) 8-35
VSRMSR (VDDSRM control register) 8-35

-X-

XER (integer exception register) 3-19