APPENDIX F
MEMORY ACCESS TIMING

F.1 Introduction

Table F-1 lists all possible memory access timing to internal and external memory combinations. The clock values show the number of clocks from the moment an address is valid on a specific bus, until data is back on that same bus. The following assumptions were used when compiling the information:

- The arbitration time was ignored. The values assume that the bus (or buses) involved in a transaction was in the IDLE state when the transaction needs that bus.
- The UIMB works in a mode of 1:1. This is relevant for IMB accesses values. In the case of 2:1 mode, the clock latency for a cycle on the IMB should be doubled. (each IMB access takes two clocks.)
- The basic delay of external bus to U-bus is four clocks (external master case).
- All IMB accesses are assumed to be 16-bit accesses only. If 32-bit accesses are used, then each such IMB access is split into two separate 16-bit cycles with normal IMB performance for each.

Table F-1 Memory Access Times Using Different Buses

	INTERNAL				EXTERNAL RAM/ FLASH		SHOW CYCLE	
	FLASH	RAM	IMB	SIU	Internal Memory Mapped External	Non-mapped Internal Memory	Write	Read
RCPU Load/Store	3/4[1]	1	6	5	4+N[2]	4+N	2	2
RCPU Instruction Fectches	2-1-1-1-1...	3[3]	-	-	2+N	2+N	-	1[4]
Peripheral Mode (ony ext. master is active)	4/5	6	7	6				
Slave Mode (both ext. & int. CPUs are active)	5/6	7	8	7				

NOTES:
1. "/" comes for on/off page flash access.
2. N is the number of clocks from external address valid till external data valid in the case of read cycle. In the case of zero wait states, N = 2.
3. Assuming BBC is parked on U-BUS.
4. Until address is valid on external pins

Table F-2 Timing Examples

Access	# Clock													Total
	1	2	3	4	5	6	7	8	9	10	11	12	13	
Load/Store -> Ebus	L	U	E											6[1]
				E	U	L								
Load/Store -> IMB 16 bits	L	U	IMB											6
				IMB	U	L								
Instruction Fetch-> cmf new page 3 concecutive accesses	C,U													2
		U[2]												
		C,U												1
		U												
			C,U											1
			U											
Instruction Fetch-> cmf new page Load/Store -> IMB	C,U													2
		U												
	L	U	IMB											6
				IMB	U	L								
Instruction Fetch-> cmf new page Load/Store -> IMB		C	U											6
						U								
	L	U	IMB											6
				IMB	U	L								
External Bus-> cmf new page	E		U											5
				U	E									
External Bus-> IMB	E		U	IMB										7
					IMB	U	E							
Instruction Fetch-> cmf 2 concecutive accesses & External Bus-> cmf		C,U												2
			U											
			C	-[3]	-	-	-	-	-	-	-	U		11
													U	
	E		retry	E[4]		U								8
							U	E						

NOTES:

1. N is the number of clocks from external address valid until external data valid in the case of read cycle. In the case of zero wait states, N = 2.
2. Core instruction fetch data bus is usualy the UBUS
3. 8 clocks are dedicated for external access, and internal accesses are denied.
4. Assuming the external master immediately retries

LEGEND

Shaded areas = address phase ; Non-shaded areas = data phase