



## APPENDIX G ELECTRICAL CHARACTERISTICS

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing characteristics of the MPC555.

The MPC555 is designed to operate at 40 MHz. The electrical characteristics are preliminary and are from previous designs, design simulations, or initial evaluation. These characteristics may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these characteristics will be met. Finalized characteristics will be published after complete characterization and device qualifications have been completed.

### G.1 Absolute Maximum Ratings ( $V_{SS} = 0$ V)

**Table G-1 Absolute Maximum Ratings**

Rating	Symbol	Min. Value	Max. Value	Unit
3-V Supply Voltage <sup>1</sup>	$V_{DDL}$	-6.0	4.0	V
Flash Supply Voltages <sup>2</sup>	$V_{PP}$	-6.0	6.0	V
Flash Core Voltage <sup>1</sup>	$V_{DDF}$	-6.0	4.0	V
Oscillator, Keep Alive Reg. Supply Voltage <sup>1</sup>	KAPWR	-6.0	4.0	V
SRAM Supply Voltage <sup>1</sup>	$V_{DDSRAM}$	-6.0	4.0	V
Clock Synthesizer Supply Voltage <sup>1</sup>	$V_{DDSYN}$	-6.0	4.0	V
QADC Supply Voltage <sup>3</sup>	$V_{DDA}$	-6.0	6.0	V
5-V Supply Voltage	$V_{DDH}$	-0.3	6.0	V
DC Input Voltages <sup>4</sup>	$V_{IN}$	$V_{SS} - 0.3$	$V_{DDH} + 0.3$	V
Reference Supply $V_{RH}$ , with Reference to $V_{RL}$	$V_{RH}$	-0.3	6.0	V
$V_{SS}$ Differential Voltage	$V_{SS} - V_{SSA}$	-0.1	0.1	V
$V_{DD}$ Differential Voltage <sup>5</sup>	$V_{DDL} - V_{DDA}$	-0.3	4.0	V
$V_{REF}$ Differential Voltage	$V_{RH} - V_{RL}$	-6.0	6.0	V
$V_{RL}$ to $V_{SSA}$ Differential Voltage	$V_{RL} - V_{SSA}$	-6.0	0.3	V
Maximum Input Current per pin <sup>6, 7, 8</sup>	$I_{MA}$	-25	25	mA
QADC Maximum Input Current per Pin	$I_{max}$	-25	25	mA
Operating Temperature Range (Packaged)	$T_A$	-40 ( $T_L$ )	+125 ( $T_H$ )	°C
Operating Temperature Range (Die Form) (Maximum junction temperature for packaged devices)	$T_J$	-40	+150	°C
Storage Temperature Range	$T_{STG}$	-55	+155	°C

**Table G-1 Absolute Maximum Ratings (Continued)**

Rating	Symbol	Min. Value	Max. Value	Unit
Maximum Solder Temperature <sup>9</sup>	T <sub>sdr</sub>		220	°C
Moisture Sensitivity Level <sup>10</sup>	MSL		3	

**NOTES:**

1. For internal digital supply of  $V_{DDL} = 3.3$  V typical.
2. During program/erase operation the value of  $V_{PP}$  must be  $5.0$  V  $\pm$  5%.
3.  $V_{DDA} = 5.0$  V  $\pm$  10%.
4. All 3-V input pins are 5-V tolerant
5. Refers to allowed random sequencing of power supplies.
6. Maximum continuous current on I/O pins provided the overall power dissipation is below the power dissipation of the package. Proper operation is not guaranteed at this condition.
7. Condition applies to one pin at a time.
8. Transitions within the limit do not affect device reliability or cause permanent damage. Exceeding limit may cause permanent conversion error on stressed channels and on unstressed channels.
9. Solder profile per CDF-AEC-Q100, current revision.
10. Moisture sensitivity per JEDEC test method A112.

Functional operating conditions are given in **G.7 DC Electrical Characteristics**. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ).

**G.2 Target Failure Rate**

Target failure rate of **TBD** ppm pending characterization and evaluation of qualifiable silicon.

**G.3 Package**

The MPC555 is available in two forms, packaged and die. The package is a 272-ball PBGA, Motorola case outline 1135A-01 (See **Figure 2-1** for a case drawing or contact Motorola.) For die characteristics, contact the Motorola factory.

**G.4 EMI Characteristics****G.4.1 Reference Documents**

The documents referenced for the EMC testing of MPC555 are listed below.

1. SAE J1752/3 Issued 1995-03
2. VDE UK 767.14/ZVEI-Ad-Hoc-HL-AK Version1.0 May 1994



## G.4.2 Definitions and Acronyms

EMC — Electromagnetic compatibility

EMI — Electromagnetic interference

TEM cell — Transverse electromagnetic mode cell

## G.4.3 Testing Characteristics

1. Scan range: 150 kHz — 1000 MHz
2. Operating frequency: 20 MHz, 40 MHz
3. Operating voltages: 3.3 V, 5.0 V
4. Max spikes: 50 dBuV
5. I/O port waveforms: 50% duty cycle @ 100  $\mu$ s period
6. Temperature: 25°C (-40°C, 125°C if available)

## G.5 Thermal Characteristics

**Table G-2 Thermal Characteristics**

Characteristic	Symbol	Value	Unit
BGA Package Thermal Resistance, Junction to Ambient — Natural Convection	$R_{\theta JA}$	42.8 <sup>1,2</sup>	°C/W
BGA Package Thermal Resistance, Junction to Ambient — Four layer (2s2p) board, nat- ural convection	$R_{\theta MA}$	30.4 <sup>3,4</sup>	°C/W
BGA Package Thermal Resistance, Junction to Board	$R_{\theta JB}$	19.9 <sup>5</sup>	°C/W
BGA Package Thermal Resistance, Junction to Case (top)	$R_{\theta JC}$	6.3 <sup>6</sup>	°C/W
BGA Package Thermal Resistance, Junction to Package Top, Natural Convection	$\Psi_{JC}$	2.7 <sup>7</sup>	°C/W

NOTES:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and the board thermal resistance.
2. Per SEMI G38-87 and JESD51-2 with the board horizontal.
3. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and the board thermal resistance.
4. Per JESD51-6 with the board horizontal.
5. Thermal resistance between the die and the printed circuit board (Four layer [2s2p] board, natural convection).
6. Indicates the thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per EIA/JESD51-2.

An estimation of the chip junction temperature,  $T_J$ , in °C can be obtained from the equation:



$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_A$  = ambient temperature (°C)

$R_{\theta JA}$  = package junction to ambient resistance (°C/W)

$P_D$  = power dissipation in package

The junction to ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. Unfortunately, the answer is only an estimate; test cases have demonstrated that errors of a factor of two are possible. As a result, more detailed thermal characterization is supplied.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$  = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$  = junction to case thermal resistance (°C/W)

$R_{\theta CA}$  = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$  is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance,  $R_{\theta CA}$ . For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for ceramic packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

The simplest thermal model of a package which has demonstrated reasonable accuracy (about 20%) is a two resistor model consisting of a junction to board and a junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature.

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$



where:

$T_B$  = board temperature ( $^{\circ}\text{C}$ )

$R_{\theta JB}$  = package junction to board resistance ( $^{\circ}\text{C}/\text{W}$ )

$P_D$  = power dissipation in package (W)

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction to board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

When the board temperature is not known, a thermal simulation of the application is needed. The simple two resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation. Consultation on the creation of the complex model is available.

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ( $\Psi_{JT}$ ) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JA} \times P_D)$$

where:

$T_T$  = thermocouple temperature on top of package ( $^{\circ}\text{C}$ )

$R_{\theta JA}$  = thermal characterization parameter

$P_D$  = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 characteristic published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

### G.5.1 Thermal References:

Semiconductor Equipment and Materials International  
805 East Middlefield Rd  
Mountain View, CA 94043  
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) characteristics are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.



JEDEC characteristics are available on the WEB at: <http://www.jedec.org>

1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
2. B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

## G.6 ESD Protection

**Table G-3 ESD Protection**

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model (HBM)		2000	V
HBM Circuit Description	R1	1500	W
	C	100	pF
ESD Target for Machine Model (MM)		200	V
MM Circuit Description	R1	0	W
	C	200	pF
Number of Pulses Per Pin			
Positive Pulses (MM)		3	
Negative Pulses (MM)	—	3	—
Positive Pulses (HBM)		1	
Negative Pulses (HBM)		1	
Interval of Pulses	—	1	Second

Notes:

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device characteristic requirements. Complete DC parametric and functional testing shall be performed per applicable device characteristic at room temperature followed by hot temperature, unless specified otherwise in the device characteristic.

## G.7 DC Electrical Characteristics



**Table G-4 DC Electrical Characteristics**

( $V_{DDL} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{DDH} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $T_A = T_L$  to  $T_H$ )

Characteristic	Symbol	Min	Max	Unit
3-V only Input High Voltage <sup>1</sup> Except EXTAL and EXTCLK	$V_{IH3}$	2.0	$V_{DDH} + 0.3$	V
3-V Input High Voltage EXTCLK	$V_{IHC}$	2.4	$V_{DDH} + 0.3$	V
5-V Input Only High Voltage <sup>2</sup>	$V_{IH5}$	$0.7 \cdot V_{DDH}$	$V_{DDH} + 0.3$	V
5-V Input High Voltage (QADC PQA, PQB)	$V_{IHA5}$	$0.7 \cdot V_{DDA}$	$V_{DDA} + 0.3$	V
Muxed 3-V/ 5-V Pins (GPIO Muxed with Addr. and Data) 3-V Input High Voltage Addr., Data 5-V Input High Voltage (GPIO)	$V_{IH3M}$ $V_{IH5M}$	2.0 $0.7 \cdot V_{DDH}$	$V_{DDH} + 0.3$ $V_{DDH} + 0.3$	V
3-V Input Low Voltage Except EXTCLK	$V_{IL3}$	$V_{SS} - 0.3$	0.8	V
3-V Input Low Voltage EXTCLK	$V_{IL3C}$	$V_{SS} - 0.3$	0.4	V
5-V Input Low Voltage	$V_{IL5}$	$V_{SS} - 0.3$	$0.4 \cdot V_{DDH}$	V
5-V Input Low Voltage (QADC PQA, PQB)	$V_{ILA5}$	$V_{SSA} - 0.3$	$0.4 \cdot V_{DDA}$	V
Muxed 3-V/ 5-V Pins (GPIO Muxed with Addr., Data) 3-V Input Low Voltage (Addr., Data) 5-V Input Low Voltage (GPIO)	$V_{IL3M}$ $V_{IL5M}$	$V_{SS} - 0.3$ $V_{SS} - 0.3$	0.8 $0.4 \cdot V_{DDH}$	V V
QADC Analog Input Voltage <sup>3</sup>	$V_{INDC}$	$V_{SSA} - 0.3$	$V_{DDA} + 0.3$	V
3-V Mode Select Current <sup>4</sup> Pull-up @ 0 V, Pull-down @ $V_{DDL}$	$I_{act3 \text{ V}}$	20	130	$\mu\text{A}$
5-V Mode Select Current <sup>4</sup> Pull-up @ $V_{IL5}$ , Pull-down @ $V_{IH5}$	$I_{act5 \text{ V}}$	20	130	$\mu\text{A}$
3-V Input Leakage Current <sup>4</sup> Pull-up/down Inactive	$I_{inact3 \text{ V}}$	—	1.0	$\mu\text{A}$
5-V Input Leakage Current <sup>4</sup> Pull-up/down Inactive	$I_{inact5 \text{ V}}$	—	1.0	$\mu\text{A}$
QADC64 Input Current, Channel Off <sup>5</sup> PQA PQB	$I_{OFF}$	-200 -150	200 150	nA

**Table G-4 DC Electrical Characteristics (Continued)**

( $V_{DDL} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{DDH} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $T_A = T_L \text{ to } T_H$ )



Characteristic	Symbol	Min	Max	Unit
3-V Output High Voltage $V_{DD} = V_{DDL}$ ( $I_{OH} = -2 \text{ mA}$ )	$V_{OH3}$	2.4	—	V
5-V Output High Voltage $V_{DD} = V_{DDH}$ ( $I_{OH} = -2 \text{ mA}$ ) All 5-V Only Outputs Except TPU.	$V_{OH5}$	$V_{DDH} - 0.7$	—	V
5-V Output High Voltage $V_{DD} = V_{DDH}$ ( $I_{OH} = -5 \text{ mA}$ ) For TPU Pins Only	$V_{OHTP5}$	$V_{DDH} - 0.65$	—	V
Muxed 3-V/ 5-V Pins (GPIO Muxed with Addr, Data) 3-V Output High Voltage ( $I_{OH} = -2 \text{ mA}$ ) 5-V Output High Voltage ( $I_{OH} = -2 \text{ mA}$ )	$V_{OH3M}$ $V_{OH5M}$	2.4 $V_{DDH} - 0.7$	—	V
3-V Output Low voltage $V_{DD} = V_{DDL}$ ( $I_{OL} = 3.2 \text{ mA}$ )	$V_{OL3}$	—	0.5	V
5-V Output Low Voltage $V_{DD} = V_{DDH}$ ( $I_{OL} = 2 \text{ mA}$ ) All 5-V Only Outputs Except TPU.	$V_{OL5}$	—	0.45	V
5-V Output Low Voltage $V_{DD} = V_{DDH}$ ( $I_{OL} = 10 \text{ mA}$ ) For TPU Pins Only	$V_{OL5}$	—	1.0	V
Muxed 3-V/ 5-V Pins (GPIO Muxed with Addr, Data) 3-V Output Low Voltage ( $I_{OL} = 3.2 \text{ mA}$ ) 5-V Output Low Voltage ( $I_{OL} = 2 \text{ mA}$ )	$V_{OL3M}$ $V_{OL5M}$	—	0.5 0.45	V
Output Low Current CLKOUT @ $V_{OL} = 0.5 \text{ V}$	$I_{OL}$	2.0	—	mA
Output High Current CLKOUT @ $V_{OH} = 2.4 \text{ V}$	$I_{OH}$	2.0	—	mA
CLKOUT Capacitance – COM[1:0] of SCCR = 0b01 COM[1:0] of SCCR = 0b00	$C_{clk}$	—	45 90	pF
ENGCLK Capacitance@20Mhz EECLK[1:0] of SCCR = 0b01 EECLK[1:0] of SCCR = 0b00	$C_{eng}$	—	45 90	pF
Capacitance for Input, Output, and Bidirectional $V_{in} = 0 \text{ V}$ , $f = 1 \text{ MHz}$ (except QADC)	$C_{in}$	—	7	pF
Load Capacitance for Bus Pins Only <sup>6</sup> COM[1:0] of SCCR = 0bX1 COM[1:0] of SCCR = 0bX0	$C_L$	—	25 50	pF
Total Input Capacitance PQA Not Sampling PQB Not Sampling Incremental Capacitance Added During Sampling	$C_{IN}$	— — —	15 10 5	pF
Hysteresis (Only IRQ, TPU, MIOS, GPIO, QADC (Digital Inputs) and RESET) <sup>7</sup>	$V_H$	0.5	—	V



**Table G-4 DC Electrical Characteristics (Continued)**

( $V_{DDL} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{DDH} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $T_A = T_L \text{ to } T_H$ )



Characteristic	Symbol	Min	Max	Unit
Operating Current (3-V Supplies) @ 33 MHz <sup>8</sup> Expanded $V_{DDL} / V_{DDI}$ KAPWR $V_{DDSRAM}$ $V_{DDSYN}$ (Crystal Frequency: 20 Mhz) $V_{DDF}$  Single Chip $V_{DDL} / V_{DDI}$ KAPWR $V_{DDSRAM}$ $V_{DDSYN}$ (Crystal Frequency: 20 Mhz) $V_{DDF}$	$I_{DDL}$ $I_{DDKAP}$ $I_{DDSRM}$ $I_{DDSYN}$ $I_{DDF}$  $I_{DDL}$ $I_{DDKAP}$ $I_{DDSRM}$ $I_{DDSYN}$ $I_{DDF}$		190 4.1 4.1 8.2 18  190 4.1 4.1 8.2 18	mA
Operating Current (5-V Supplies) @ 33 MHz <sup>9</sup> $V_{DDH}$ $V_{DDA}$ $V_{PP}$	$I_{DDH5}$ $I_{DDA}$ $I_{DDPP}$		21 5 30	mA
Operating Current (3-V Supplies) @ 40 MHz <sup>10</sup> Expanded $V_{DDL} / V_{DDI}$ KAPWR $V_{DDSRAM}$ $V_{DDSYN}$ (Crystal Frequency: 20 Mhz) $V_{DDF}$ <sup>11</sup>  Single Chip $V_{DDL} / V_{DDI}$ KAPWR $V_{DDSRAM}$ $V_{DDSYN}$ (Crystal Frequency: 20 Mhz) $V_{DDF}$	$I_{DDL}$ $I_{DDKAP}$ $I_{DDSRM}$ $I_{DDSYN}$ $I_{DDF}$  $I_{DDL}$ $I_{DDKAP}$ $I_{DDSRM}$ $I_{DDSYN}$ $I_{DDF}$		230 5.0 5.0 10 22  230 5.0 5.0 10 22	mA
Operating Current (5-V Supplies) @ 40 MHz <sup>12</sup> $V_{DDH}$ $V_{DDA}$ <sup>13</sup> $V_{PP}$	$I_{DDH5}$ $I_{DDA}$ $I_{DDVPP}$		25 5.0 30	mA
QADC64 Low Power Stop Mode ( $V_{DDA}$ )	$I_{DDA}$		10	$\mu\text{A}$
Low Power Current @ 40 MHz DOZE, Active PLL and Active Clocks SLEEP, Active PLL with Clocks off DEEP SLEEP, PLL and Clocks off	$I_{DDDZ}$ $I_{DDSLP}$ $I_{DDPSLP}$		<b>TBD</b> <sup>14</sup> <b>TBD</b> <sup>15</sup> <b>TBD</b> <sup>16</sup>	mA mA $\mu\text{A}$
$V_{DDL}$ , $V_{DDI}$ Operating Voltage	$V_{DDL}$ , $V_{DDI}$	3.0	3.6	V
$V_{PP}$ Flash Operating Voltage	$V_{PP}$	$V_{DDL} - 0.35 \text{ V}$	5.50	V
$V_{PP}$ Flash Programming Voltage	$V_{PP}$	4.75	5.25	V

**Table G-4 DC Electrical Characteristics (Continued)**

( $V_{DDL} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{DDH} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $T_A = T_L$  to  $T_H$ )



Characteristic	Symbol	Min	Max	Unit
Oscillator, Keep Alive Registers Operating Voltage during normal operation ( $V_{DDL}$ powered-up) <sup>17,18</sup>	KAPWR	$V_{DDL} - 0.2$	$V_{DDL} + 0.2$	V
Oscillator, Keep Alive Registers Operating Voltage during power-down operation	KAPWR	3.0	3.6	V
SRAM Operating Voltage during normal operation ( $V_{DDL}$ powered-up) <sup>19</sup>	$V_{DDSRAM}$	$V_{DDL} - 0.2$	$V_{DDL} + 0.2$	V
$V_{DDH}$ Operating Voltage	$V_{DDH}$	4.5	5.5	V
QADC Operating Voltage	$V_{DDA}$	4.5	5.5	V
Clock Synthesizer Operating Voltage <sup>20</sup>	$V_{DDSYN}$	$V_{DDL} - 0.2$	$V_{DDL} + 0.2$	V
$V_{SS}$ Differential Voltage	$V_{SS} - V_{SSA}$	-100	100	mV
QADC64 Reference Voltage Low <sup>21</sup>	$V_{RL}$	$V_{SSA}$	$V_{SSA} + 0.1$	V
QADC64 Reference Voltage High <sup>22</sup>	$V_{RH}$	$V_{DDA} - 0.3$	$V_{DDA}$	V
QADC64 $V_{REF}$ Differential Voltage	$V_{RH} - V_{RL}$	4.5	5.5	V
QADC64 Reference Supply Current, DC	$I_{REF}$	—	500	$\mu\text{A}$
QADC64 Reference Supply Current, Transient	$I_{REF}$	—	4.0	mA
Standby Supply Current <sup>4</sup> KAPWR Only			4	mA
$V_{DDSRAM}$ Only (RAM Standby Current) @ $T_J = 90^\circ\text{C}$			100	$\mu\text{A}$
$V_{DDSRAM}$ Only (RAM Standby Current) @ $T_J = 90^\circ\text{C}$ with Low Voltage Protection Circuitry			150	$\mu\text{A}$
$V_{DDSRAM}$ Only (RAM Standby Current) @ $T_J = 150^\circ\text{C}$			250	$\mu\text{A}$
RAM Standby Voltage for Data Retention (Power Down Mode) <sup>4</sup> Specified $V_{DD}$ Applied ( $V_{DD} = V_{SS}$ )	$V_{DDSRAM}$	1.4 <sup>23</sup>	3.6	V
DC Injection Current per Pin GPIO, TPU, MIOS, QSM, EPEE and 5 V <sup>4, 24</sup>	$I_{IC5}$	-1.0	1.0	mA
DC Injection Current Per Pin 3 V <sup>4, 23, 25</sup>	$I_{IC3}$	-1.0	1.0	mA
QADC64 Disruptive Input Current <sup>23, 26</sup>	$I_{NA}$	-3	3	mA
Power Dissipation -40 MHz 33 MHz	PD		1 0.8	W

NOTES:

1. This spec is for 3-V output and 5-V input friendly pins.
2. This spec is for 5-V output and 5-V input pins.
3. Within this range, no significant injection will be seen. See QADC64 disruptive input current ( $I_{NA}$ ).
4. After characterization this value may be improved.
5. Maximum leakage occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 – 12°C, in the ambient temperature range of 50 – 125°C.
6. All bus pins support two drive strengths capabilities, 25 pF and 50 pF. Current drive is less at the 25-pF capacitive load. Both modes achieve 40-MHz timing.
7. Only IRQ, TPU, MIOS, GPIO, QADC (when digital inputs) and RESET pins have hysteresis, thus there is no hysteresis characteristic required for all other pins



8. Values to be characterized. Current consumption values will be updated as information becomes available.
9. Values to be characterized. Current consumption values will be updated as information becomes available.
10. All power consumption characteristics assume 50-pF loads and running a typical application. Of the power consumption of some modules could go up is they are exercised heavier, but the power consumption of other modules would decrease.
11. The worst case  $V_{DDF}$  occurs during  $\overline{HRESET}$  active (booting), other modules will not be running.
12. Values to be characterized. Current consumption values will be updated as information becomes available.
13. Current measured at maximum system clock frequency with QADC active.
14. Pending characterization.
15. Pending characterization.
16. Pending characterization.
17. KAPWR and  $V_{DDSRAM}$  are powered up prior to any other supply.
18. This parameter is periodically sampled rather than 100% tested
19. KAPWR and  $V_{DDSRAM}$  are powered up prior to any other supply.
20. This parameter is periodically sampled rather than 100% tested.
21. To obtain full-range results,  $V_{SSA} \leq V_{RL} \leq V_{INDC} \leq V_{RH} \leq V_{DDA}$
22. To obtain full-range results,  $V_{SSA} \leq V_{RL} \leq V_{INDC} \leq V_{RH} \leq V_{DDA}$
23. The voltage at which the LVSRS bits in the VSRMCR register will be set ranges from 1.5 – 2.4 V.
24. All injection current is transferred to the  $V_{DDH}$ . An external load is required to dissipate this current to maintain the power supply within the specified voltage range.
25. Total injection current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.
26. Below disruptive current conditions, the channel being stressed has conversion values of \$3FF for analog inputs greater than  $V_{RH}$  and \$000 for values less than  $V_{RL}$ . This assumes that  $V_{RH} \leq V_{DDA}$  and  $V_{RL} \geq V_{SSA}$  due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

## G.8 Oscillator and PLL Electrical Characteristics

**Table G-5 Oscillator and PLL**

Characteristic	Symbol	Min	Typical	Max	Unit
Oscillator Startup Time (For Typical Crystal Capacitive Load) 4-MHz Crystal 20-MHz Crystal	OSCstart4 OSCstart20			10 10	mS
PLL Lock Time	$T_{LOCK}$			500	Input Clocks
PLL Operating Range	$F_{VCOOUT}$	30		80	MHz
Crystal Operating Range, MODCK=0b010,0b110 MODCK[1:3] = 0b001, 0b011, 0b100, 0b101, 0b111)	$F_{CRYSTAL}$	2 15		5 25	MHz
PLL Jitter		-1%		+1%	—
Limp Mode Clock Out Frequency		<b>3<sup>1</sup></b>	7	<b>12<sup>1</sup></b>	MHz
Oscillator Bias Current (XTAL) 4 MHz 20 MHz	$I_{BIAS}$	<b>TBD<sup>2</sup></b> <b>TBD<sup>2</sup></b>		— — —	mA
Oscillator Drive (XTAL)	$I_{OSC}$	<b>TBD<sup>2</sup></b>		—	mA
Oscillator Bias Resistor	$R_{OSC}$	<b>TBD<sup>2</sup></b>	1	<b>TBD<sup>2</sup></b>	MΩ

**NOTES:**

1. Estimated value, real values to be characterized and updated.
2. Values to be characterized.

## G.9 Power Up/Down Sequencing

See [SECTION 8 CLOCKS AND POWER CONTROL](#).



## G.10 FLASH Electrical Characteristics

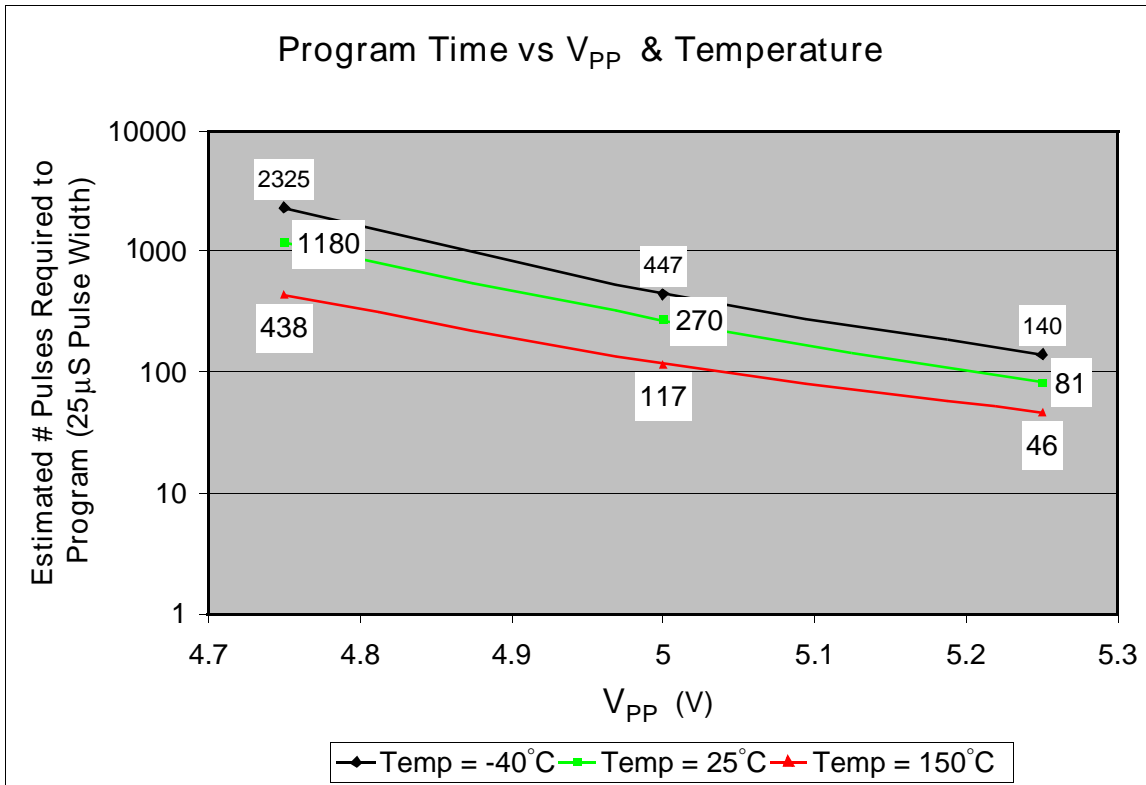
**Table G-6 Program and Erase Characteristics**

( $V_{DDF} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{PP} = 4.75 \text{ V to } 5.25 \text{ V}$ ,  $T_A = T_L \text{ to } T_H$ )

Symbol	Meaning	Value			Units
		Minimum	Typical	Maximum	
$E_{PULSE}$	Number of Erase Pulses	1	1	1	
$T_{ERASE}$	Erase Pulse Time	0.9	1	1.1	S
$P_{PULSE(4.75 \text{ V}_{pp})}$	Number of Program Pulses @ $V_{PP} = 4.75$	—	1200 <sup>1</sup>	3500 <sup>2,3,5</sup>	Pulses
$P_{PULSE(5.0 \text{ V}_{pp})}$	Number of Program Pulses @ $V_{PP} = 5.00$	—	300 <sup>4</sup>	1000 <sup>5</sup>	Pulses
$P_{PULSE(5.25 \text{ V}_{pp})}$	Number of Program Pulses <sup>6</sup> @ $V_{PP} = 5.25$	—	125 <sup>7</sup>	500 <sup>5</sup>	Pulses
$T_{PROG}$	Program Pulse Time	21.2	25.6	32.0	$\mu\text{S}$
$C_{PULSE(4.75 \text{ V}_{pp})}$	Number of CENSOR Clear Pulses @ $V_{PP} = 4.75$	1	1	3 <sup>8</sup>	Pulses
$C_{PULSE(5.0 \text{ V}_{pp})}$	Number of CENSOR Clear Pulses @ $V_{PP} = 5.00$	1	1	3 <sup>8</sup>	Pulses
$C_{PULSE(5.25 \text{ V}_{pp})}$	Number of CENSOR Clear Pulses @ $V_{PP} = 5.25$	1	1	3 <sup>8</sup>	Pulses
$T_{CLEAR}$	CENSOR Clear Pulse Time	0.9 <sup>8</sup>	1 <sup>8</sup>	1.1 <sup>8</sup>	S
$S_{PULSE(4.75 \text{ V}_{pp})}$	Number of CENSOR Set Pulses @ $V_{PP} = 4.75$	1	1	3 <sup>8</sup>	Pulses
$S_{PULSE(5.0 \text{ V}_{pp})}$	Number of CENSOR Set Pulses @ $V_{PP} = 5.00$	1	1	3 <sup>8</sup>	Pulses
$S_{PULSE(5.25 \text{ V}_{pp})}$	Number of CENSOR Set Pulses @ $V_{PP} = 5.25$	1	1	3 <sup>8</sup>	Pulses
$T_{SET}$	CENSOR Set Pulse Time	0.9 <sup>8</sup>	1 <sup>8</sup>	1.1 <sup>8</sup>	S

**NOTES:**

1. The typical number of pulses at  $V_{PP} = 4.75 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .
2. The worst case programming time occurs at  $V_{PP} = 4.75 \text{ V}$  and  $T_A = -40^\circ\text{C}$ .
3. This value is based on initial device characterization and is not tested in production.
4. The typical number of pulses is at  $V_{PP} = 5.00 \text{ v}$  and  $T_A = 25^\circ\text{C}$ .
5. Assumes pulse width = 25.6  $\mu\text{s}$ .
6. The best case (fastest) programming time of < 50 pulses is at  $V_{PP} = 5.25 \text{ V}$  and  $T_A = 125^\circ\text{C}$ .
7. The typical number of pulses is at  $V_{PP} = 5.25 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .
8. After characterization this value may be improved.



**Figure G-1 Typical Program Time vs.  $V_{PP}$  and Temperature  
(for CDR1 “Target” Process)**

**Table G-7 CMF AC and DC Power Supply Characteristics**

Symbol	Meaning	Min. Value	Max Value	Unit
$V_{DDF}$	Operating Voltage Read, Program or Erase	3.0	3.6 V	V
$I_{DDF}$	Operating Current at 40.0MHz, $V_{DDF} = 3.3$ V for a 256K-byte Module Read, Program or Erase Operation Disabled	— —	22 5	mA
$V_{PP}$	External Program or Erase voltage Read Program or Erase	$V_{DDF} - 0.35$ 4.75	5.5 5.25	V
$I_{PP}$	External Program and Erase Current <sup>1</sup> Read, $V_{PP} = 5$ V Program, $V_{PP} = 5.25$ V Erase, $V_{PP} = 5.25$ V		<100 <sup>1</sup> 30 <sup>1</sup> 30 <sup>1</sup>	$\mu A^1$ mA <sup>1</sup> mA <sup>1</sup>

**NOTES:**

1. Average current is less than 30 mA when programming both modules simultaneously.

## G.10.1 Flash Module Life



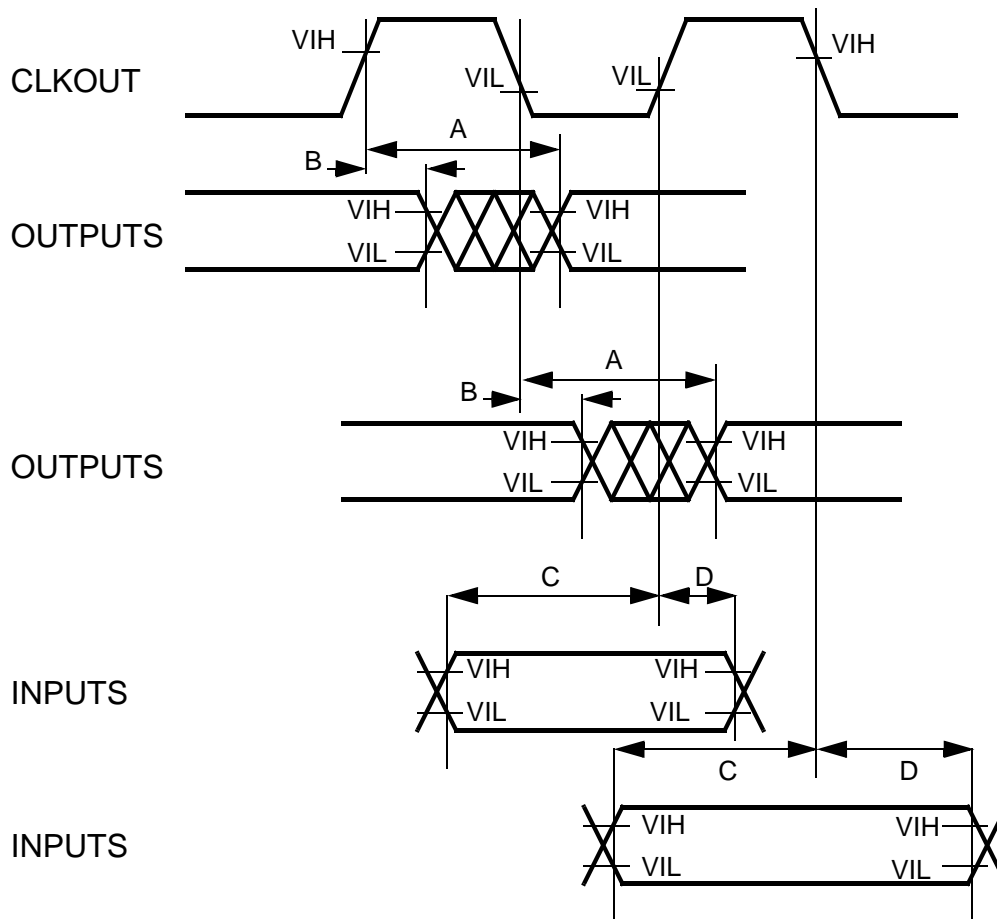
**Table G-8 Flash Module Life**

Symbol	Meaning	Value
P/E Cycles <sup>1</sup>	Maximum Number of Program/ Erase cycles <sup>2</sup> to Guarantee Data Retention	100 <sup>3,4</sup>
Retention	Data Retention at Average Operating Temperature of 85 °C	Minimum 10 years

NOTES:

1. Target failure rate at specified number of program/erase cycles of 2ppm pending characterization of production silicon.
2. A program/erase cycle is defined as switching the bits from 1 → 0 → 1.
3. Reprogramming of a CMF array block prior to erase is not required.
4. Number of program/erase cycles to be adjusted pending characterization of production silicon.

## G.11 Timing



- A. Maximum Output Delay Characteristic
- B. Minimum Output Hold Time
- C. Minimum input Setup Time Characteristic
- D. Minimum input Hold Time Characteristic

**Figure G-2 CLKOUT Timing**

### Table G-9 Bus Operation Timing

( $T_A = T_L$  to  $T_H$ )



	Characteristic	Expression	33MHz		40MHz		Unit
			Min	Max	Min	Max	
1	CLKOUT Period	TC		30.30		25	ns
2	Clock Pulse Width Low		15 – 2%		12.5 – 2%		ns
3	Clock Pulse Width High		15 – 2%		12.5 – 2%		ns
4	CLKOUT Rise Time			5		5	ns
5	CLKOUT Fall Time			5		5	ns
6	Circuit Parameter	TCC	8		7		ns
7	CLKOUT to Signal Invalid (Hold Time) A(0:31) RD/WR BURST D(0:31)	0.25TC – 1.25	6		5		ns
7a	CLKOUT to Signal Invalid: (Hold Time) TSIZ(0:1) REG RSV AT(0:3) BDIP PTR RETRY	0.25TC – 1.25	6		5		ns
7b	CLKOUT to Signal Invalid (Hold Time) (See Note 1.) BR BG FRZ VFLS(0:1) VF(0:2) IWP(0:2) LWP(0:1) STS <sup>1</sup>	0.25TC – 1.25	6		5		ns
7c	Slave mode CLKOUT to Signal Invalid D(0:31)	<b>0.25TC + TCC</b>	8		7		ns
8	CLKOUT to Signal Valid A(0:31) RD/WR BURST D(0:31)	0.25TC + TCC	7.5	15	6.25	13	ns



### Table G-9 Bus Operation Timing (Continued)

( $T_A = T_L$  to  $T_H$ )



	Characteristic	Expression	33MHz		40MHz		Unit
			Min	Max	Min	Max	
8a	CLKOUT to Signal Valid TSIZ(0:1) REG $\overline{RSV}$ AT(0:3) $\overline{BDIP}$ $\overline{PTR}$ $\overline{RETRY}$	$0.25TC + TCC$	7.5	15	6.25	13	ns
8b	CLKOUT to Signal Valid (See Note 1.) $\overline{BR}$ $\overline{BG}$ VFLS(0:1) VF(0:2) IWP(0:2) FRZ LWP(0:1) $\overline{STS}$ valid.	$0.25TC + TCC$	7.5	15	6.25	13	ns
8c	Slave Mode CLKOUT to Signal Valid D(0:31)	$0.25TC + TCC + 4$		18		17	ns
9	CLKOUT to High Z A(0:31) $\overline{RD}/\overline{WR}$ $\overline{BURST}$ D(0:31) TSIZ(0:1) REG $\overline{RSV}$ AT(0:3) $\overline{PTR}$ $\overline{RETRY}$	$0.25TC + TCC$	7.5	15	6.25	13	ns
10	CLKOUT to $\overline{TS}$ , $\overline{BB}$ Assertion	$0.25TC + TCC$	7.5	15	6.25	13	ns
10a	CLKOUT to $\overline{TA}$ , $\overline{BI}$ Assertion (When Driven by the Memory Controller)	—		10		10	ns
10b	CLKOUT to $\overline{RETRY}$ Assertion (When Driven by the Memory Controller)	—		10		10	ns
11	CLKOUT to $\overline{TS}$ , $\overline{BB}$ Negation	$0.25TC + TCC$	7.5	15	6.25	13	ns
11a	CLKOUT to $\overline{TA}$ , $\overline{BI}$ Negation (When Driven by the Memory Controller)	—		11		11	ns
11b	CLKOUT to $\overline{RETRY}$ Negation (When Driven by the Memory Controller)	—		11		11	ns
12	CLKOUT to $\overline{TS}$ , $\overline{BB}$ High Z	$0.25TC + 14$	7.5	21	6.25	20	ns

**Table G-9 Bus Operation Timing (Continued)**

( $T_A = T_L$  to  $T_H$ )



	Characteristic	Expression	33MHz		40MHz		Unit
			Min	Max	Min	Max	
12a	CLKOUT to $\overline{TA}$ , $\overline{BI}$ High Z (When Driven by the Memory Controller)			15		15	ns
13	CLKOUT to $\overline{TEA}$ Assertion			11		11	ns
14	CLKOUT to $\overline{TEA}$ High Z			15		15	ns
15	Input Valid to CLKOUT (Setup Time) $\overline{TA}$ $\overline{TEA}$ $\overline{BI}$ (See Note 2.)		12		9.75		ns
15a	Input Valid to CLKOUT (Setup Time) $\overline{KR}$ $\overline{CR}$ $\overline{RETRY}$		11		10		ns
15b	Input Valid to CLKOUT (Setup Time) $\overline{BB}$ $\overline{BG}$ $\overline{BR}$ (See Note 3.)		9		7		ns
16	CLKOUT to Signal Invalid (Hold Time) $\overline{TA}$ $\overline{TEA}$ $\overline{BI}$ $\overline{BB}$ $\overline{BG}$ $\overline{BR}$ (See Note 2.)		2		2		ns
16a	CLKOUT to Signal Invalid (Hold Time) $\overline{RETRY}$ $\overline{KR}$ $\overline{CR}$		2		2		ns
17	Signal Valid to CLKOUT Rising Edge (Setup Time) D(0:31) (See Note 4.)		6		6		ns
18	CLKOUT Rising Edge to Signal Invalid (Hold Time) D(0:31) (See Note 4.)		2		1		ns
19	CLKOUT Rising Edge to $\overline{CS}$ asserted -GPCM- ACS = 00	$0.25TC + TCC + 1$	7.5	16	6.25	14	ns

### Table G-9 Bus Operation Timing (Continued)

( $T_A = T_L$  to  $T_H$ )



	Characteristic	Expression	33MHz		40MHz		Unit
			Min	Max	Min	Max	
19a	CLKOUT Falling Edge to $\overline{CS}$ Asserted -GPCM- ACS = 10, TRLX = 0 or 1	TCC + 1		9		8	ns
19b	CLKOUT Falling Edge to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 0 or 1	0.25TC + TCC + 1	7.5	16	6.25	14	ns
19c	CLKOUT Falling Edge to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 0, EBDF = 1	0.25TC + TCC + 4	7.5	20	6.25	17	ns
20	CLKOUT Rising Edge to $\overline{CS}$ Negated -GPCM- Read Access or Write Access When CSNT = 0 or Write Access When CSNT = 1 and ACS = 00	TCC + 1	1	9	1	8	ns
21	A(0:31) to $\overline{CS}$ Asserted -GPCM- ACS = 10, TRLX = 0		8		3		ns
21a	A(0:31) to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 0		18		8		ns
22	CLKOUT Rising Edge to $\overline{OE}$ , $\overline{WE}(0:3)$ Asserted			11		8	ns
23	CLKOUT Rising Edge to $\overline{OE}$ Negated	Must Be Higher Than Data Hold	2	11	1	8	ns
24	A(0:31) to $\overline{CS}$ Asserted -GPCM- ACS = 10, TRLX = 1		48		23		ns
24a	A(0:31) to $\overline{CS}$ Asserted -GPCM- ACS = 11, TRLX = 1		58		28		ns
25	CLKOUT Rising Edge to $\overline{WE}(0:3)$ Negated -GPCM-Write Access CSNT = '0'			11		6	ns
25a	CLKOUT Falling Edge to $\overline{WE}(0:3)$ Negated -GPCM-Write Access TRLX = '0' or '1', CSNT = '1', EBDF = 0'.	0.25TC + TCC + 1	7.5	16	6.25	14	ns
25b	CLKOUT Falling Edge to $\overline{CS}$ Negated -GPCM-Write Access TRLX = '0' or '1', CSNT = '1', ACS = '10' or ACS='11', EBDF = 0	0.25TC + TCC + 1	7.5	16	6.25	14	ns
25c	CLKOUT Falling Edge to $\overline{WE}(0:3)$ Negated -GPCM-Write Access TRLX = '0', CSNT = '1, EBDF = 1'.	0.25TC + TCC + 4	7.5	20	6.25	17	ns
25d	CLKOUT Falling Edge to $\overline{CS}$ Negated -GPCM-Write Access TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 1	0.25TC + TCC + 4	7.5	20	6.25	17	ns
26	$\overline{WE}(0:3)$ Negated to D(0:31) High Z -GPCM- Write Access, CSNT = '0'		8		3		ns

**Table G-9 Bus Operation Timing (Continued)**

( $T_A = T_L$  to  $T_H$ )



	Characteristic	Expression	33MHz		40MHz		Unit
			Min	Max	Min	Max	
26a	$\overline{WE}(0:3)$ Negated to D(0:31) High Z -GPCM- Write Access, TRLX = '0', CSNT = '1', EBDF = 0		18		8		ns
26b	$\overline{CS}$ Negated to D(0:31), High Z -GPCM- Write Access, ACS = '00', TRLX = '0' & CSNT = '0'		8		3		ns
26c	$\overline{CS}$ Negated to D(0:31), High Z -GPCM- Write Access, TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 0		18		8		ns
26d	$\overline{WE}(0:3)$ Negated to D(0:31) High Z -GPCM- Write Access, TRLX = '1', CSNT = '1', EBDF = 0		58		28		ns
26e	$\overline{CS}$ Negated to D(0:31) High Z -GPCM- Write Access, TRLX = '1', CSNT = '1', ACS = '10' or ACS='11', EBDF = 0		58		28		ns
26f	$\overline{WE}(0:3)$ Negated to D(0:31) High Z -GPCM- Write Access, TRLX = '0', CSNT = '1', EBDF = 1		12		5		ns
26g	$\overline{CS}$ Negated to D(0:31) High Z -GPCM- Write Access, TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 1		12		5		ns
26h	$\overline{WE}(0:3)$ Negated to D(0:31) High Z -GPCM- Write Access, TRLX = '1', CSNT = '1', EBDF = 1		52		24		ns
26i	$\overline{CS}$ Negated to D(0:31) High Z -GPCM- Write Access, TRLX = '1', CSNT = '1', ACS = '10' or ACS='11', EBDF = 1		52		24		ns
27	$\overline{CS}$ , $\overline{WE}(0:3)$ Negated to A(0:31) Invalid -GPCM- Write Access (See Note 5.)		8		3		ns
27a	$\overline{WE}(0:3)$ Negated to A(0:31) Invalid -GPCM- Write Access, TRLX = '0', CSNT = '1'.  $\overline{CS}$ Negated to A(0:31) Invalid -GPCM- Write Access, TRLX = '0', CSNT = '1', ACS = 10, ACS = '11', EBDF = 0		18		8		ns

### Table G-9 Bus Operation Timing (Continued)

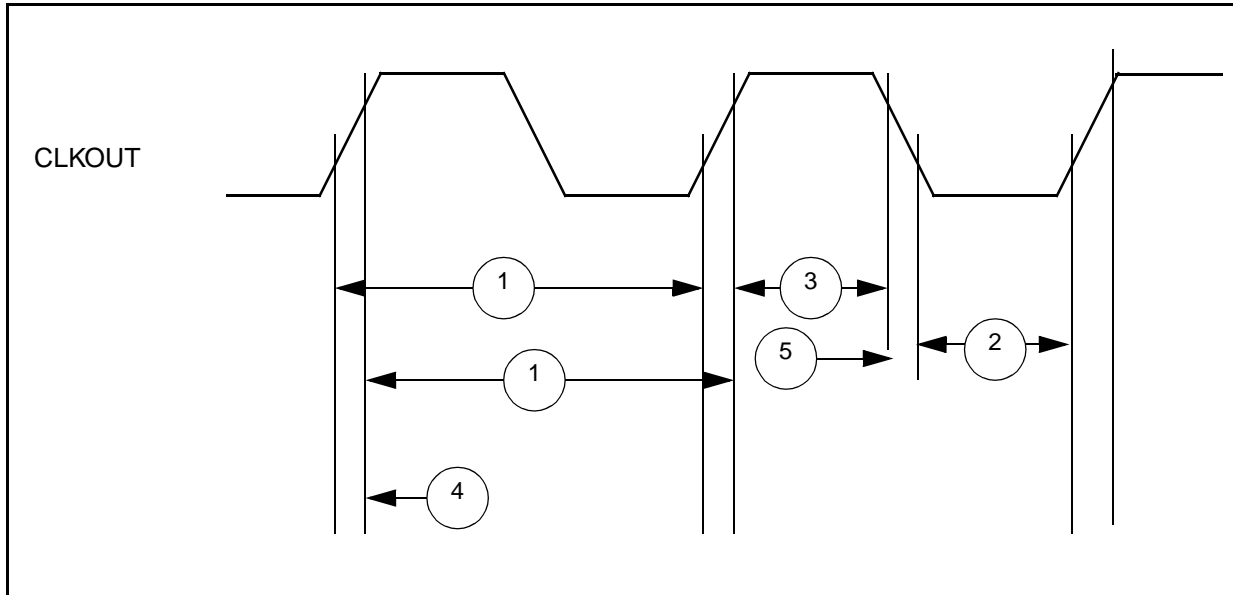
( $T_A = T_L$  to  $T_H$ )



	Characteristic	Expression	33MHz		40MHz		Unit
			Min	Max	Min	Max	
27b	$\overline{WE}(0:3)$ Negated to A(0:31) Invalid -GPCM- Write Access, $TRLX = '1'$ , $CSNT = '1'$ .  CS Negated to A(0:31) Invalid -GPCM- Write Access, $TRLX = '1'$ , $CSNT = '1'$ , $ACS = 10$ , $ACS = ='11'$ , $EBDF = 0$		58		28		ns
27c	$\overline{WE}(0:3)$ Negated to A(0:31) Invalid -GPCM- Write Access, $TRLX = '0'$ , $CSNT = '1'$ .  $\overline{CS}$ Negated to A(0:31) Invalid -GPCM- Write Access, $TRLX = '0'$ , $CSNT = '1'$ , $ACS = 10$ , $ACS = ='11'$ , $EBDF = 1$		12		4		ns
27d	$\overline{WE}(0:3)$ Negated to A(0:31) Invalid -GPCM- Write Access, $TRLX = '1'$ , $CSNT = '1'$ .  CS Negated to A(0:31) Invalid -GPCM- Write Access, $TRLX = '1'$ , $CSNT = '1'$ , $ACS = 10$ , $ACS = ='11'$ , $EBDF = 1$		52		24		ns
28	A(0:31), $TSIZ(0:1)$ , $RD/\overline{WR}$ , $BURST$ , $\overline{BDIP}$ Valid to CLKOUT Rising Edge. (Slave Mode Setup Time)		13		11		ns
28a	Slave Mode D(0:31) Valid to CLKOUT Rising Edge				7		ns
29	$\overline{TS}$ Valid to CLKOUT Rising Edge (Setup Time)		9		7		ns
30	CLKOUT Rising Edge to $\overline{TS}$ Valid (Hold Time).		2		2		ns

**NOTES:**

1. The timing for  $\overline{BR}$  output is relevant when the CMF/CMFI is selected to work with external bus arbiter. The timing for  $\overline{BG}$  output is relevant when the CMF/CMFI is selected to work with internal bus arbiter.
2. The setup times required for  $\overline{TA}$ ,  $\overline{TEA}$ , and  $\overline{BI}$  are relevant only when they are supplied by the external device (and not the memory controller).
3. The timing required for  $\overline{BR}$  input is relevant when the MPC500 family microcontroller is selected to work with internal bus arbiter. The timing for  $\overline{BG}$  input is relevant when the MPC500 is selected to work with external bus arbiter.
4. The D(0:31) input timings 17 and 18 refer to the rising edge of the CLKOUT in which the  $\overline{TA}$  input signal is asserted.
5. The timing 27 refers to CS when  $ACS = '00'$  and to  $\overline{WE}(0:3)$  when  $CSNT = '0'$ .



**Figure G-3 External Clock Timing**

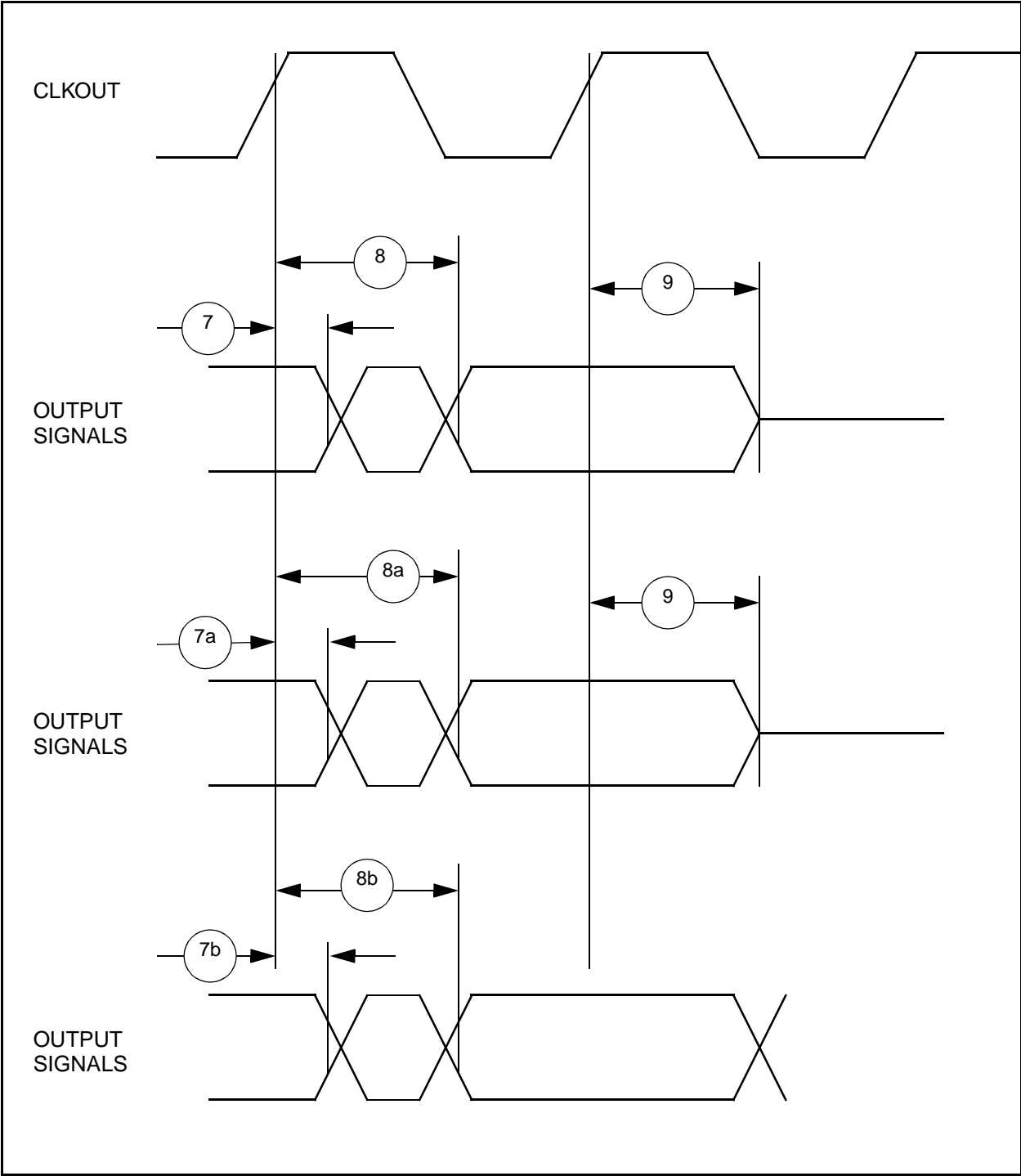
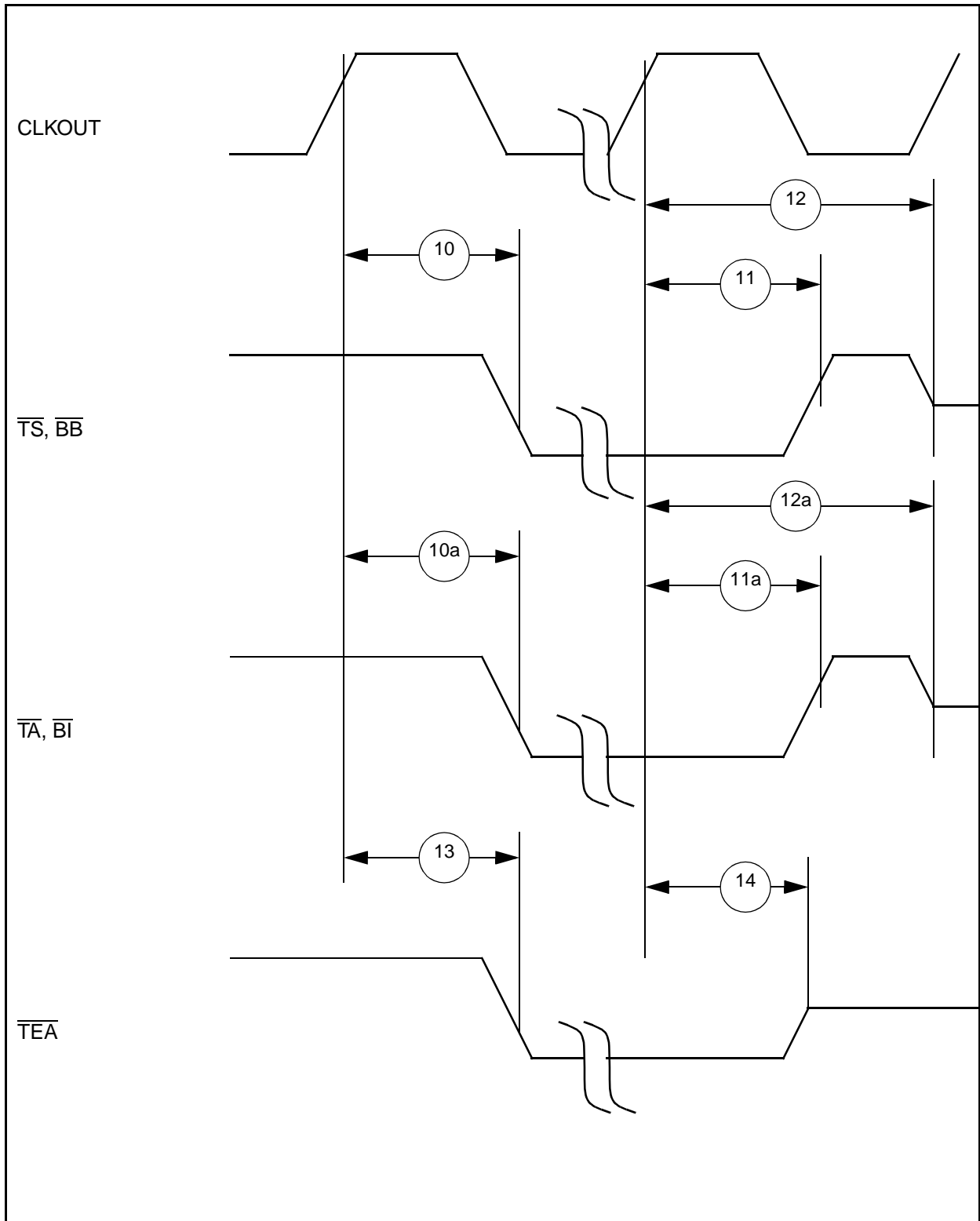


Figure G-4 Synchronous Output Signals Timing



**Figure G-5 Synchronous Active Pull-up And Open Drain Outputs Signals Timing**



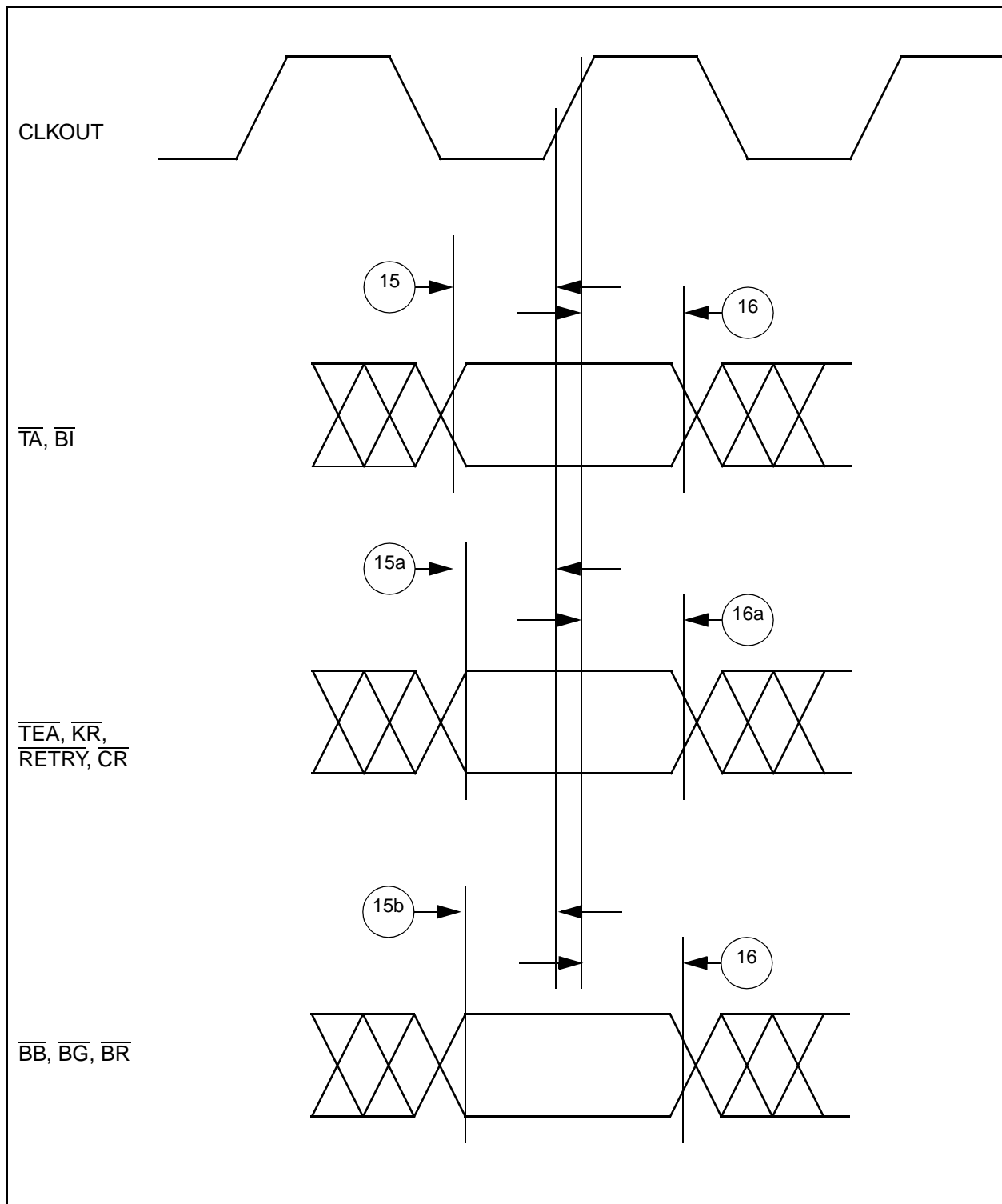
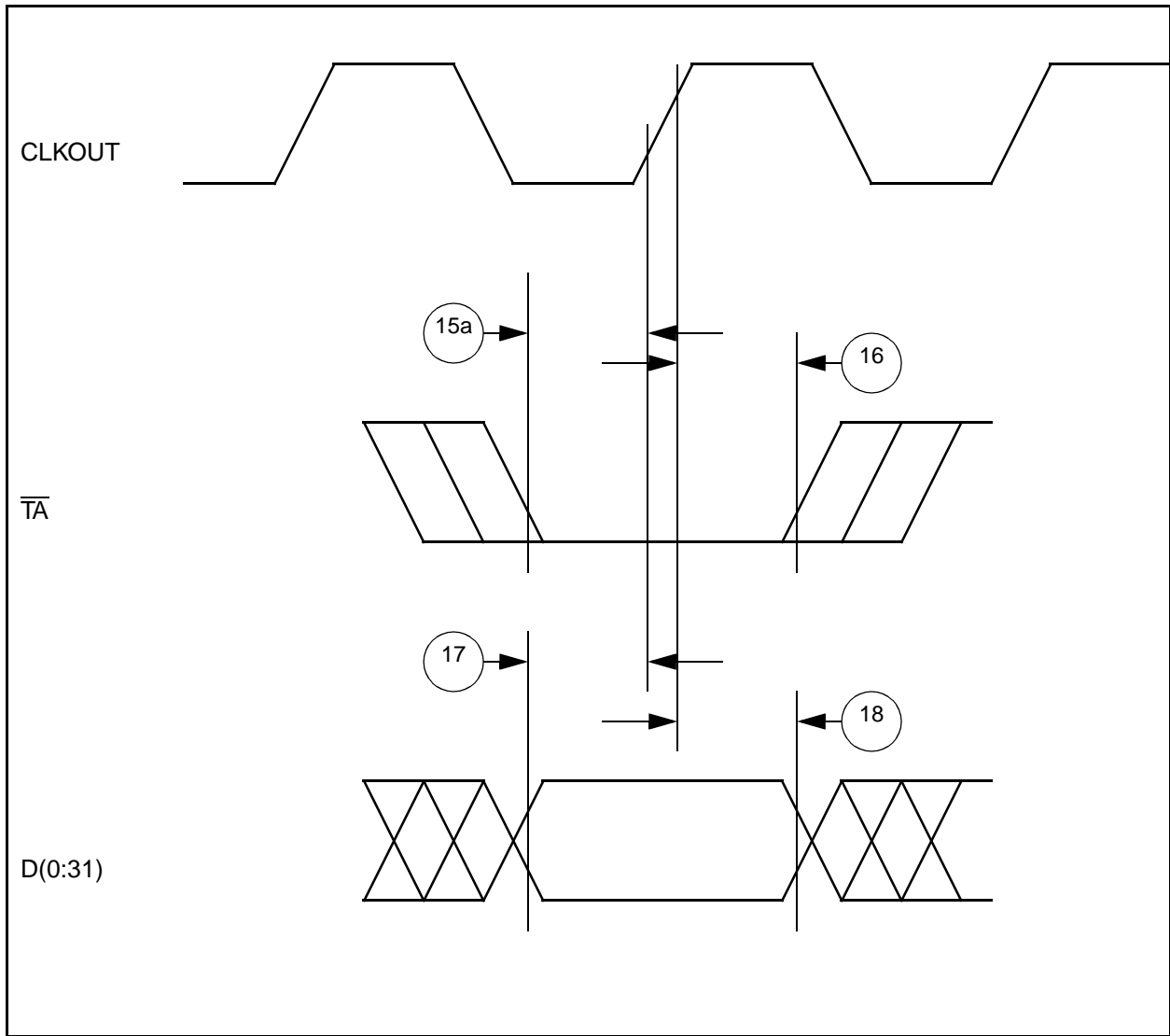


Figure G-6 Synchronous Input Signals Timing



**Figure G-7 Input Data Timing in Normal Case**

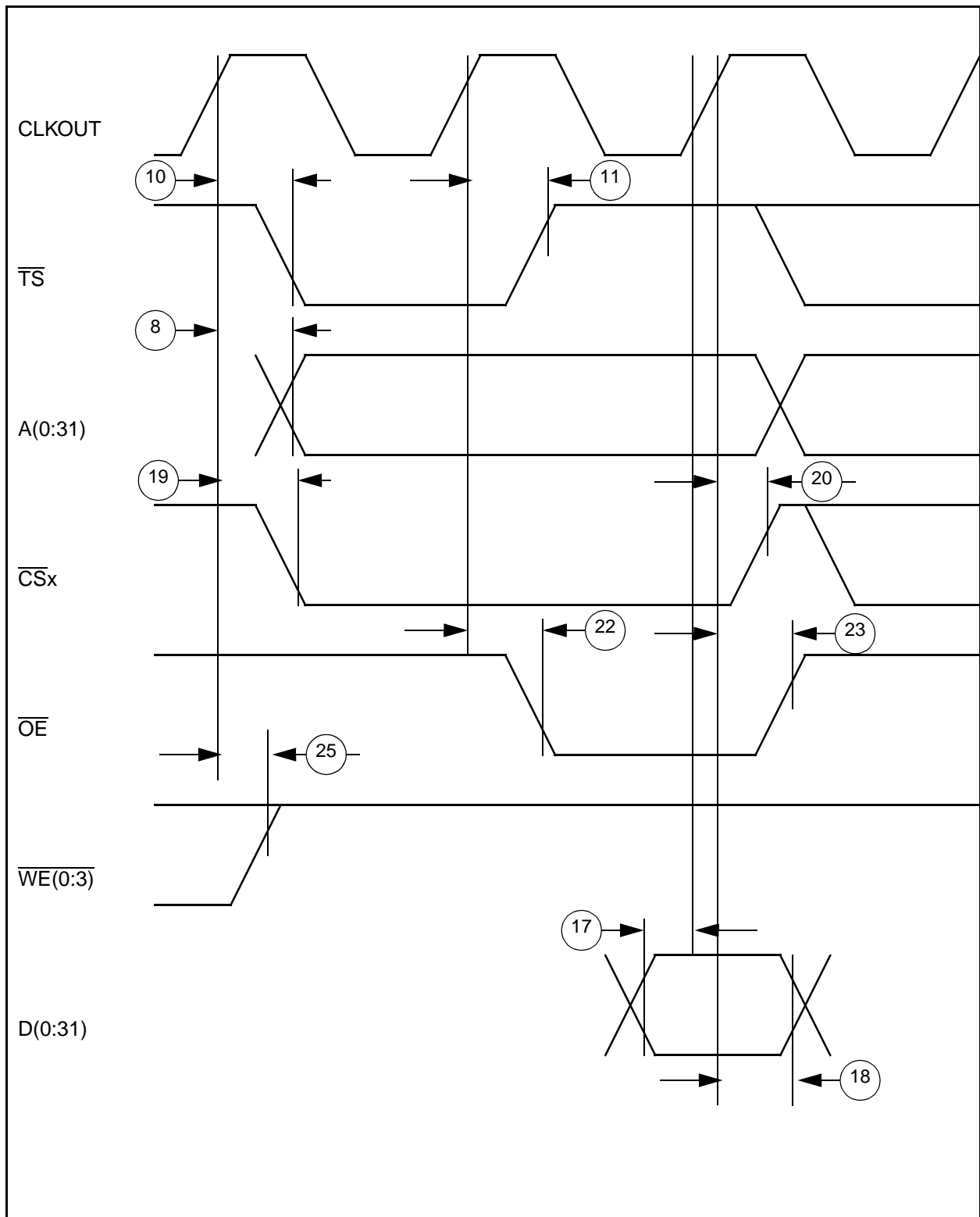


Figure G-8 External Bus Read Timing (GPCM Controlled — ACS = '00')

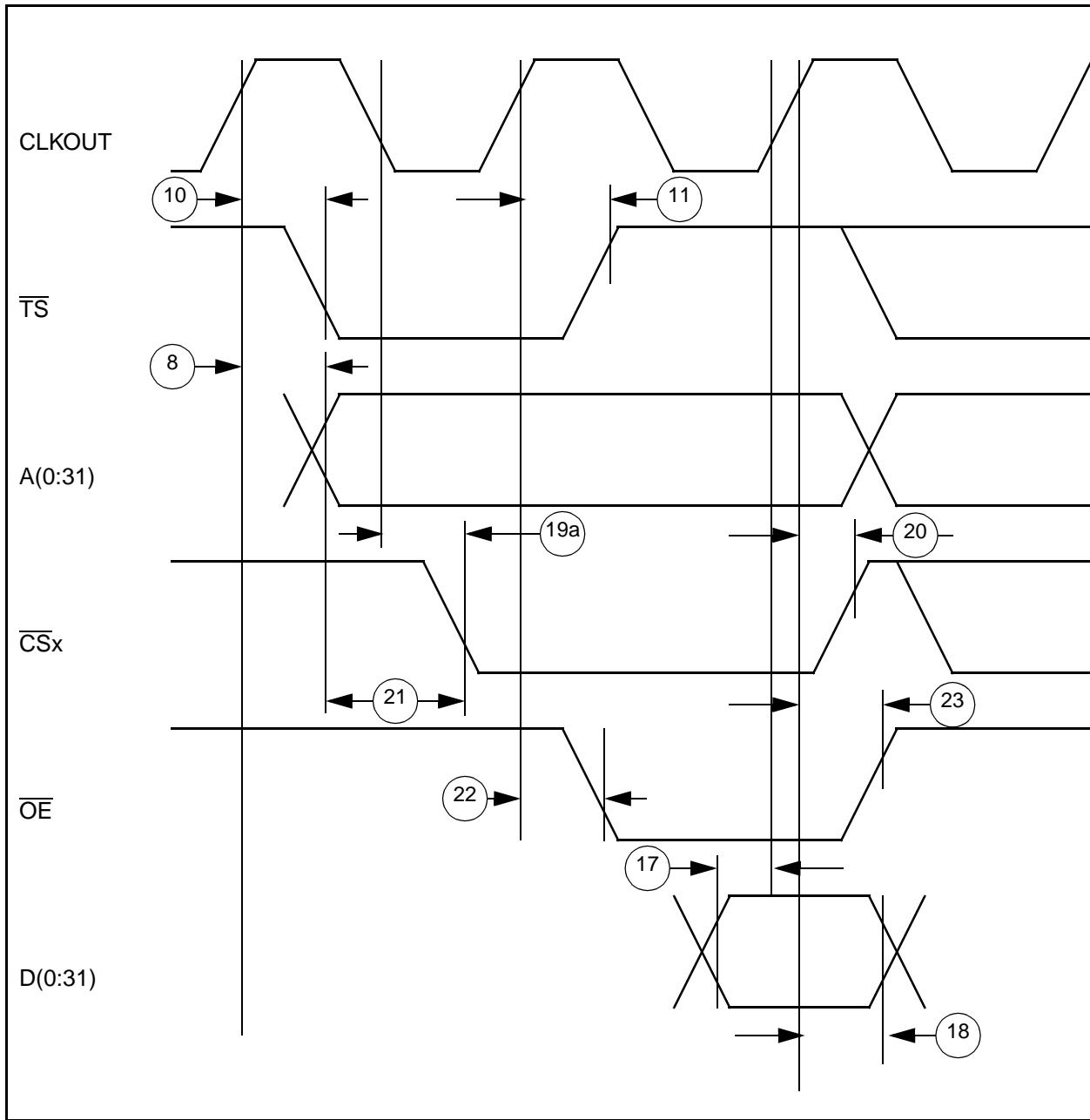


Figure G-9 External Bus Read Timing (GPCM Controlled — TRLX = '0' ACS = '10')

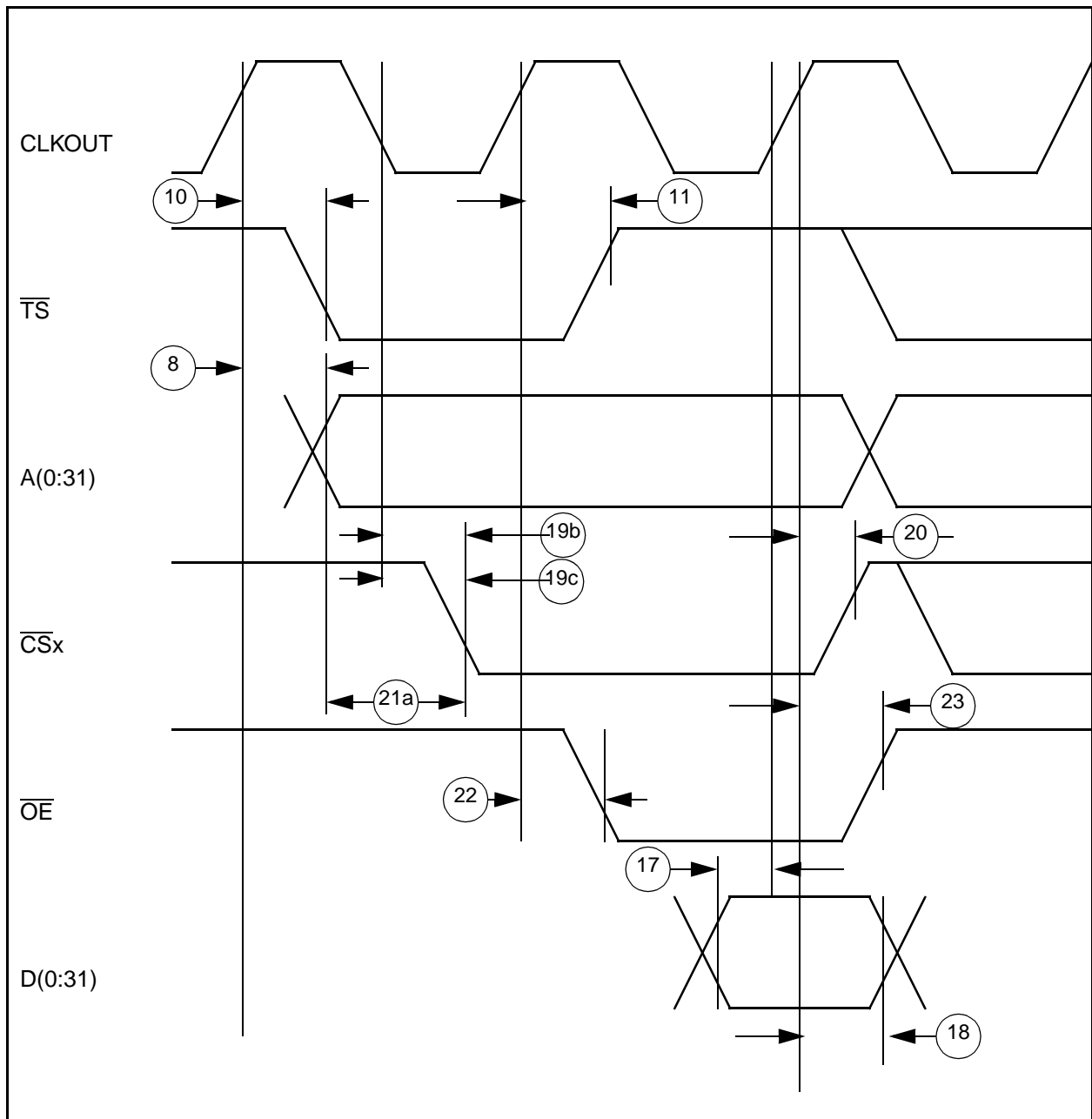
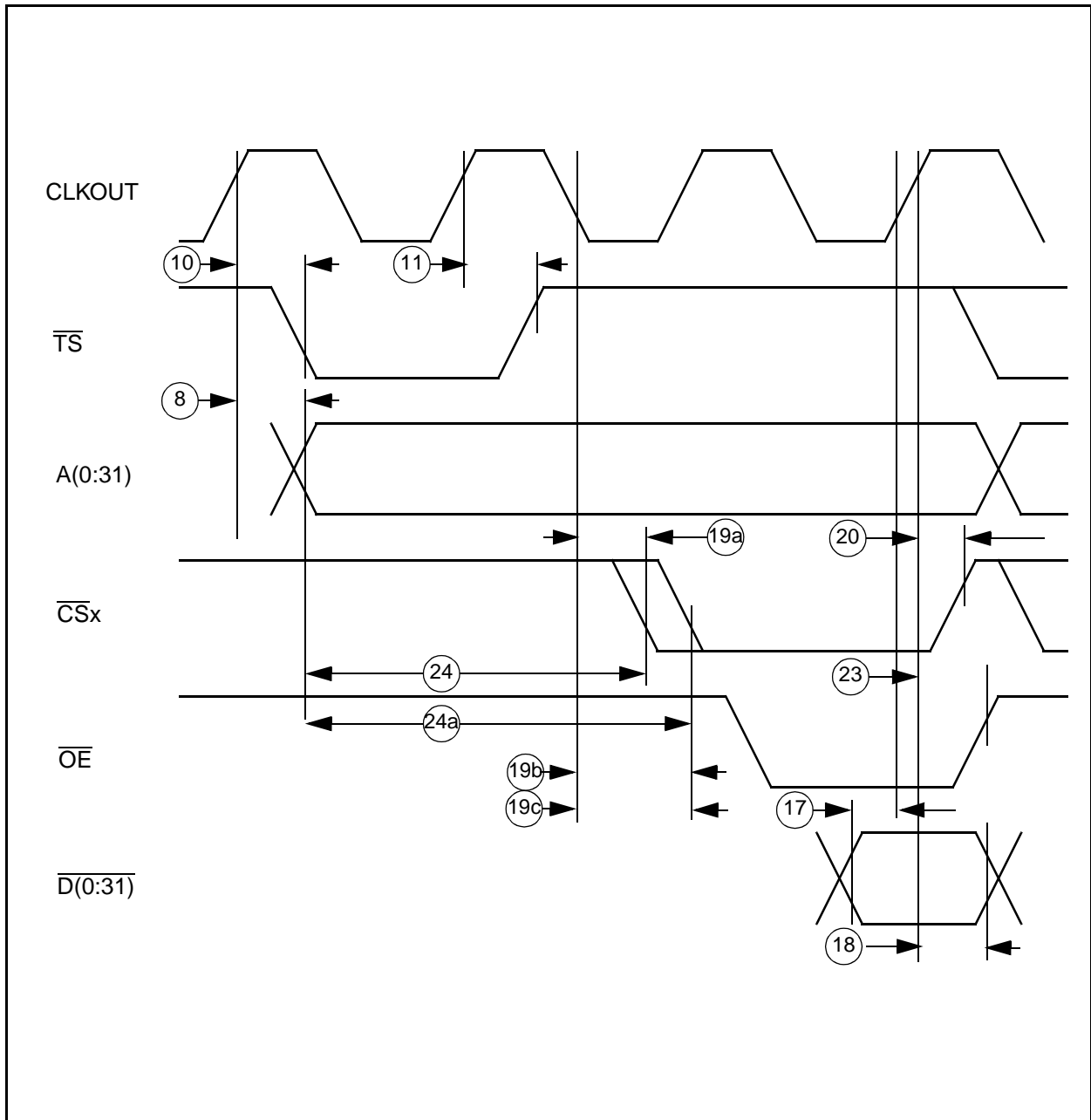
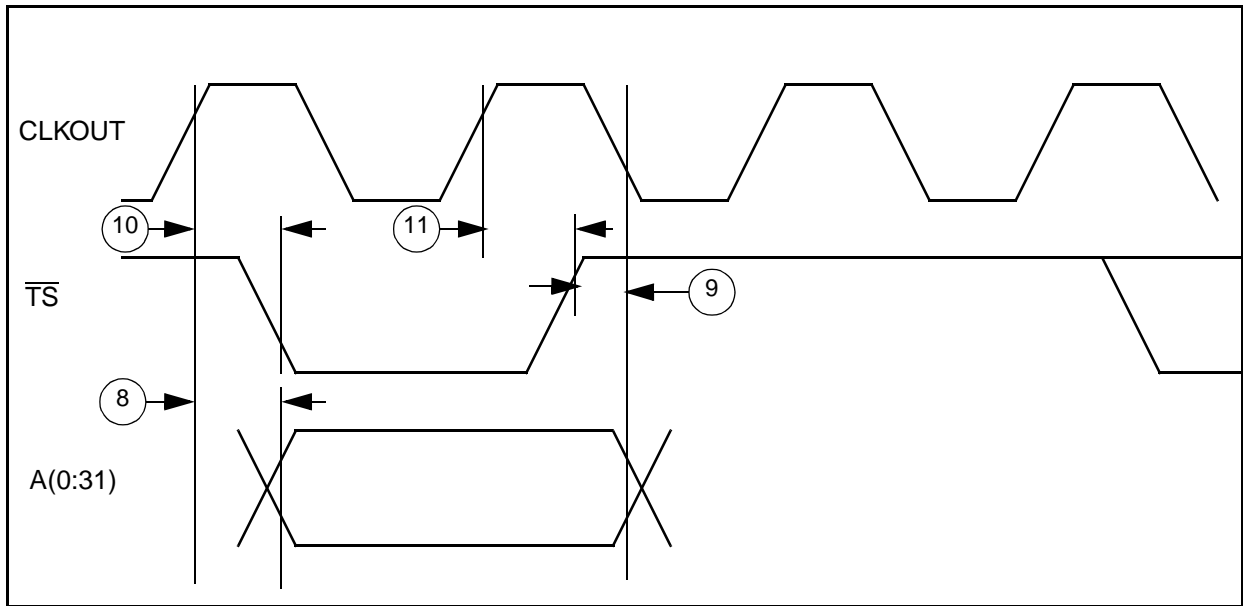


Figure G-10 External Bus Read Timing (GPCM Controlled —  $TRLX = '0'$   $ACS = '11'$ )



**Figure G-11 External Bus Read Timing**  
(GPCM Controlled — TRLX = '1', ACS = '10', ACS = '11')



**Figure G-12 Address Show Cycle Bus Timing**

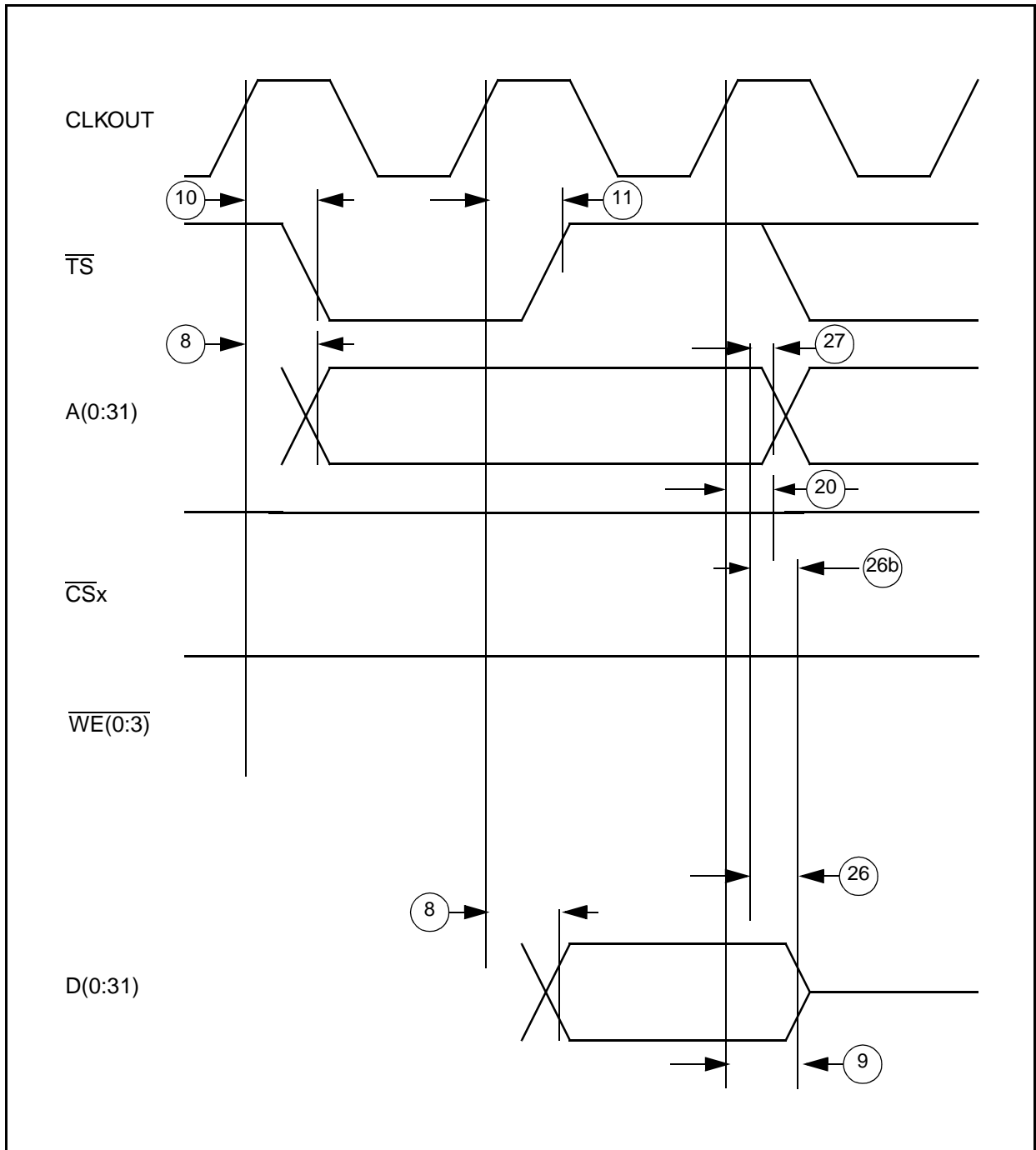


Figure G-13 Address and Data Show Cycle Bus Timing



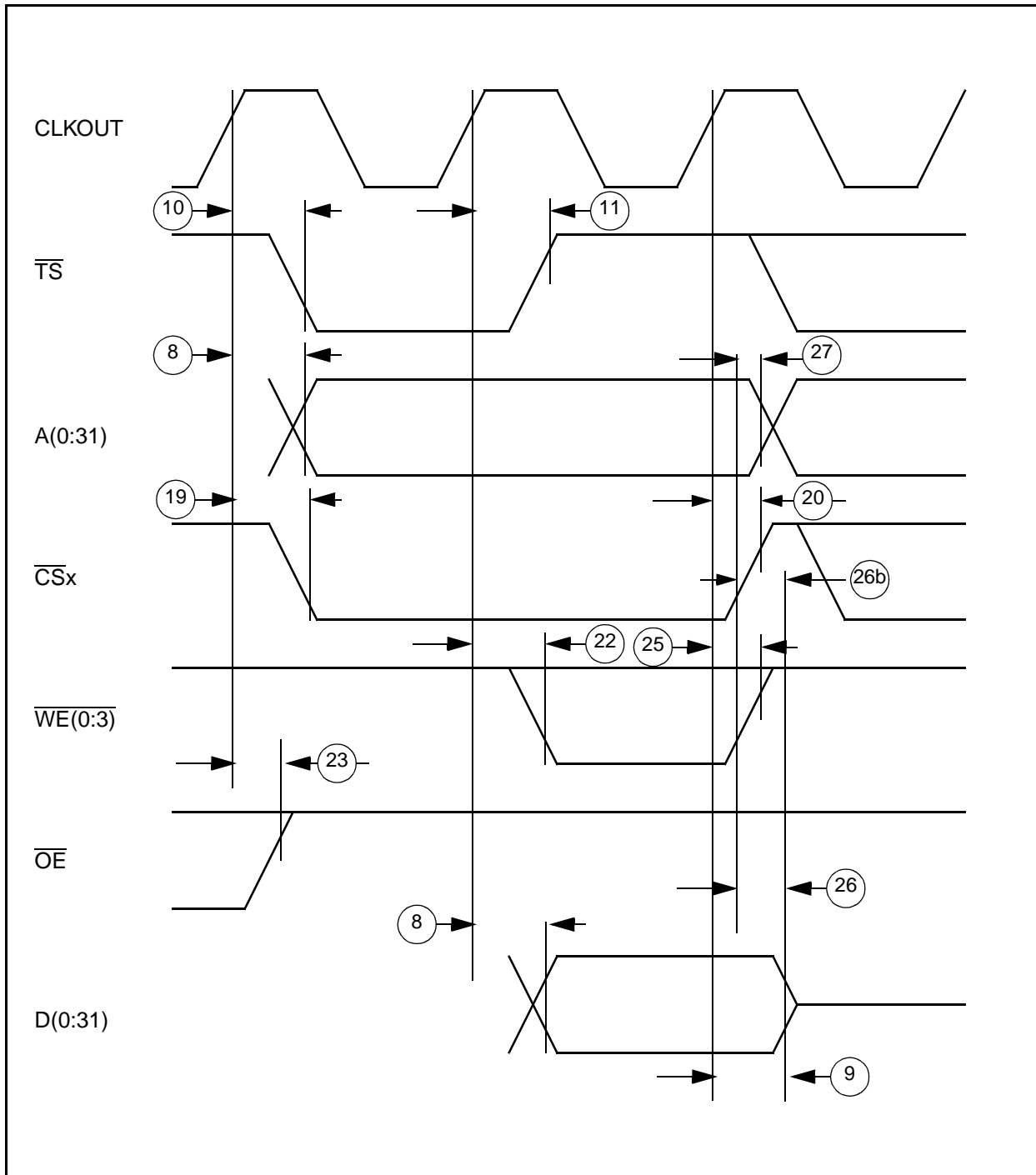


Figure G-14 External Bus Write Timing (GPCM Controlled — TRLX = '0', CSNT = '0')

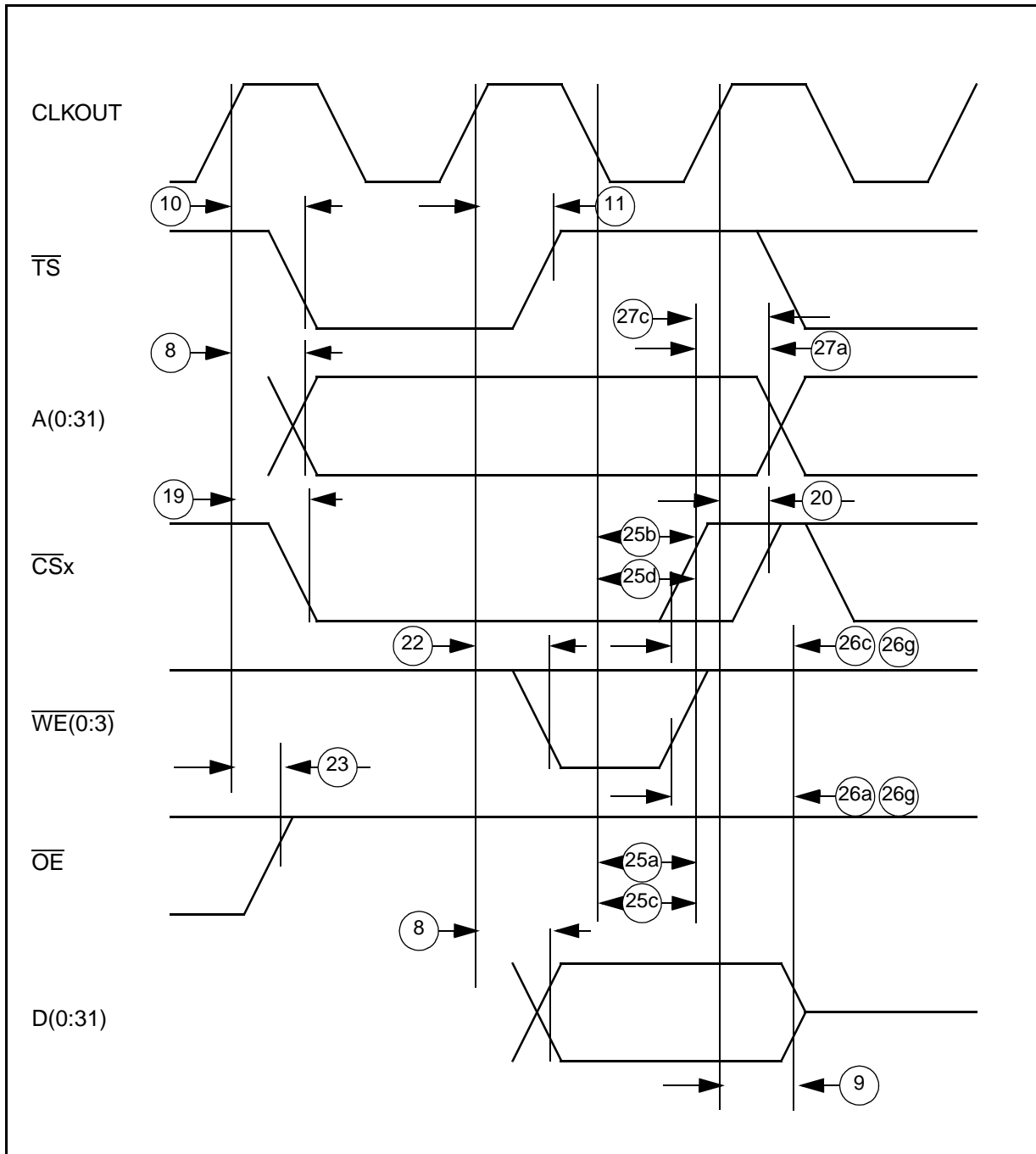


Figure G-15 External Bus Write Timing (GPCM Controlled — TRLX = '0', CSNT = '1')

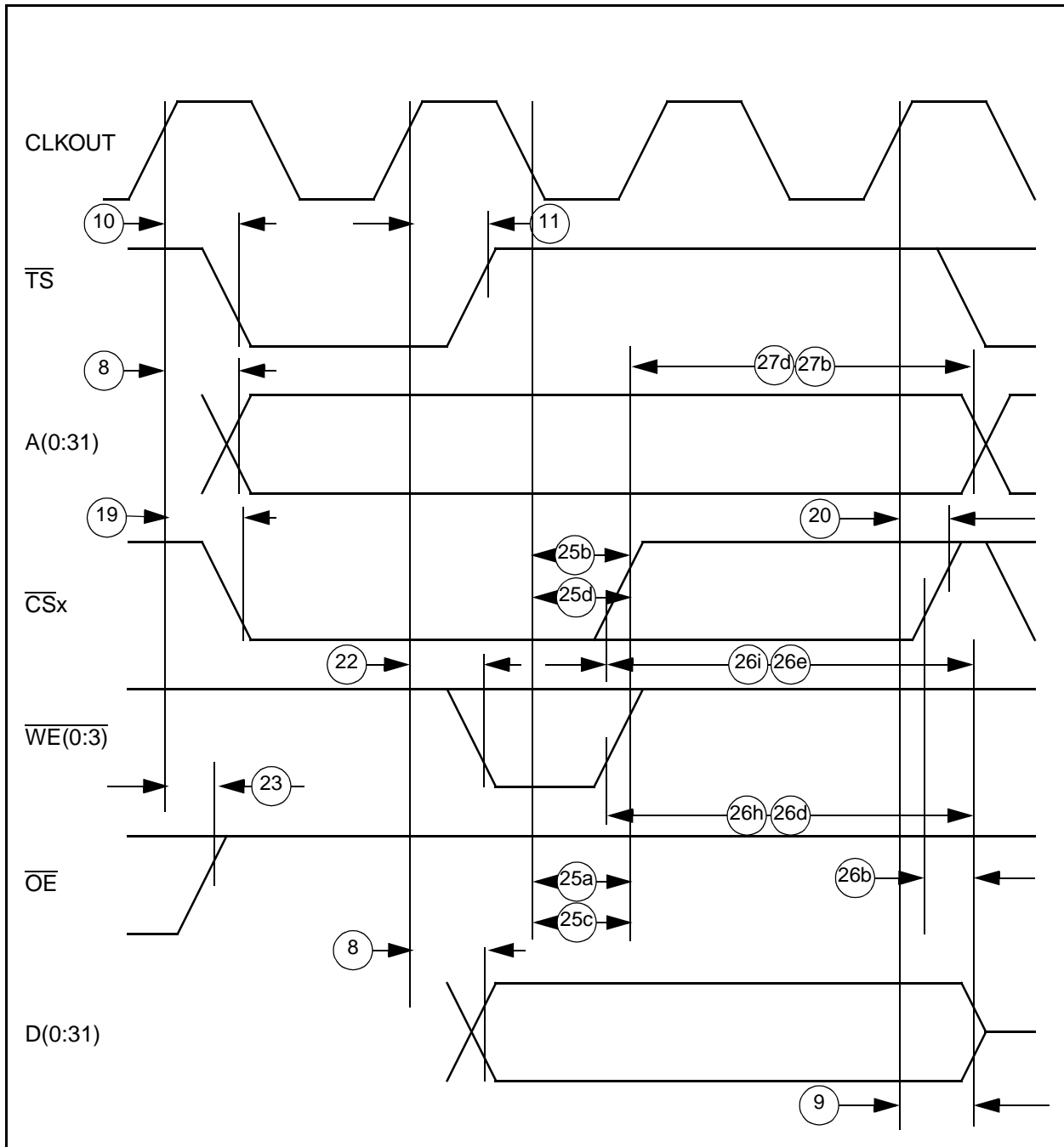


Figure G-16 External Bus Write Timing (GPCM Controlled — TRLX = '1', CSNT = '1')

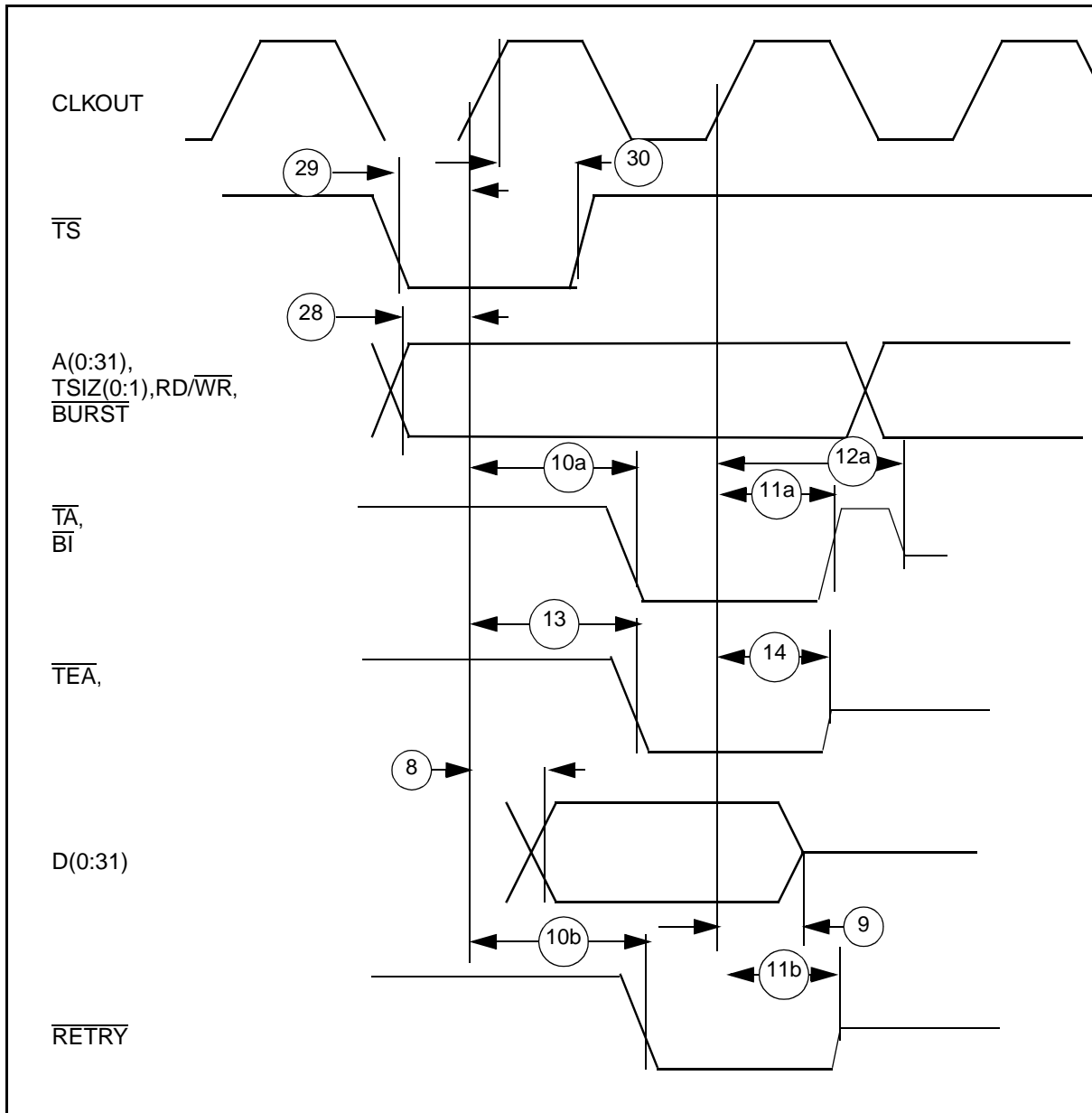
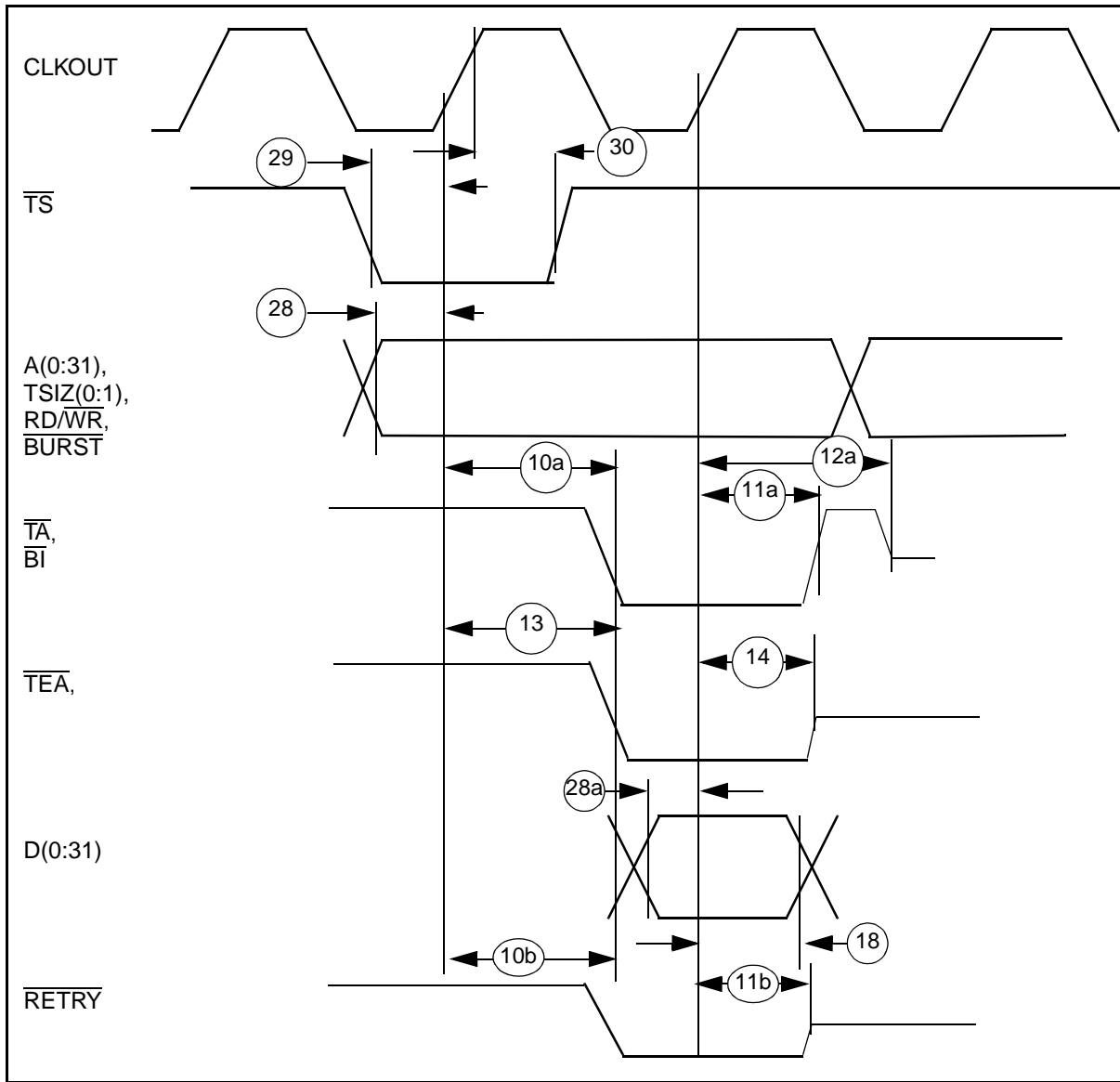


Figure G-17 External Master Read from Internal Registers Timing



**Figure G-18 External Master Write to Internal Registers Timing**

## G.12 Interrupt Timing



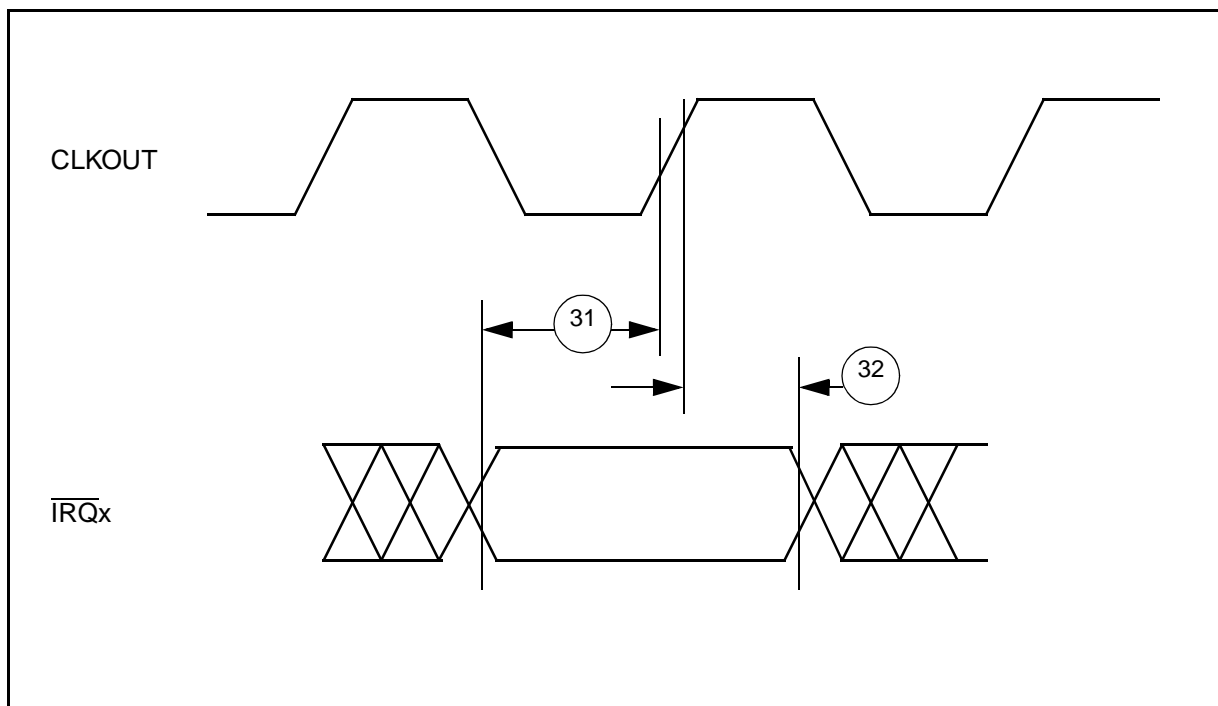
### Table G-10 Interrupt Timing

( $T_A = T_L$  to  $T_H$ )

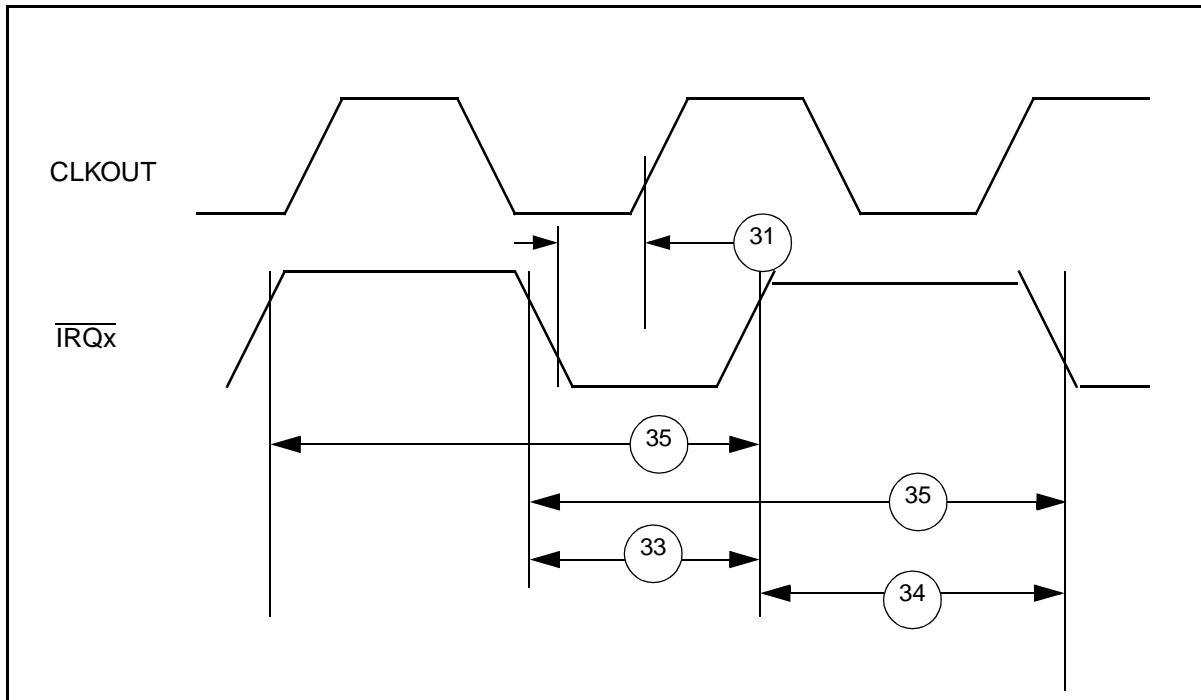
	Characteristic	Expression	33MHz		40MHz		Unit
			Min	Max	Min	Max	
31	$\overline{IRQx}$ Valid to CLKOUT Rising Edge (Setup Time) <sup>1</sup>		10		10		ns
32	$\overline{IRQx}$ Hold Time After CLKOUT <sup>1</sup>		2		2		ns
33	$\overline{IRQx}$ Pulse Width Low		3		3		ns
34	$\overline{IRQx}$ Pulse Width High		3		3		ns
35	$\overline{IRQx}$ Edge to Edge Time	$4 \cdot TC$	121		100		ns

#### NOTES:

1. The timings 31 and 32 describe the testing conditions under which the  $\overline{IRQ}$  lines are tested when being defined as level sensitive. The  $\overline{IRQ}$  lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.



**Figure G-19 Interrupt Detection Timing for External Level Sensitive Lines**



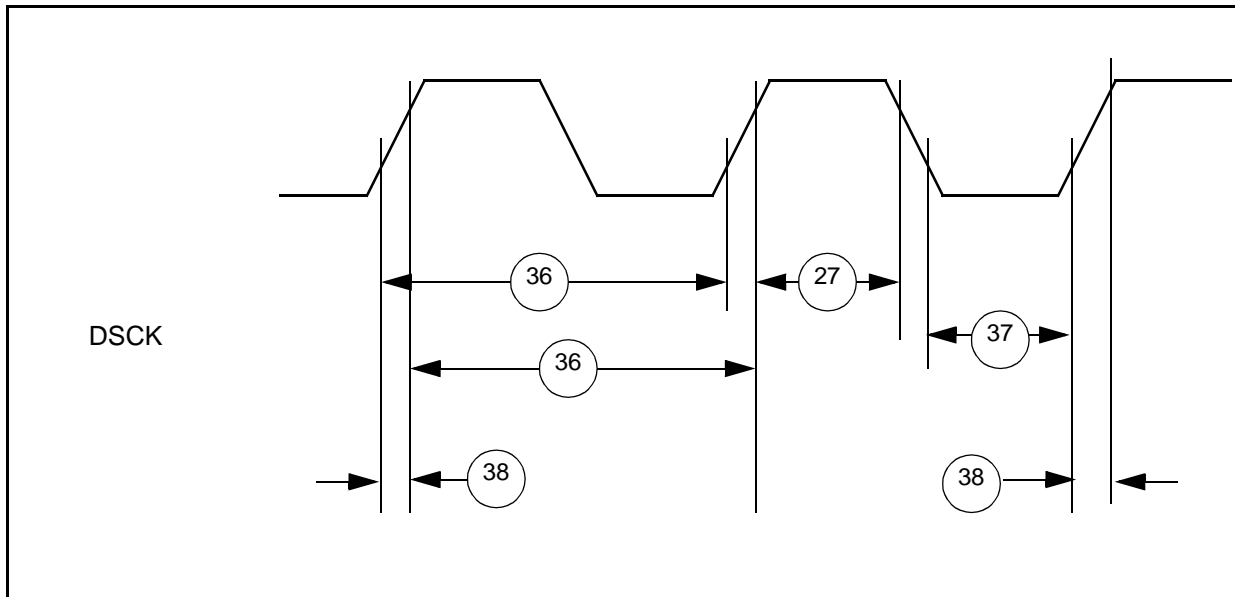
**Figure G-20 Interrupt Detection Timing for External Edge Sensitive Lines**

### G.13 Debug Port Timing

**Table G-11 Debug Port timing**

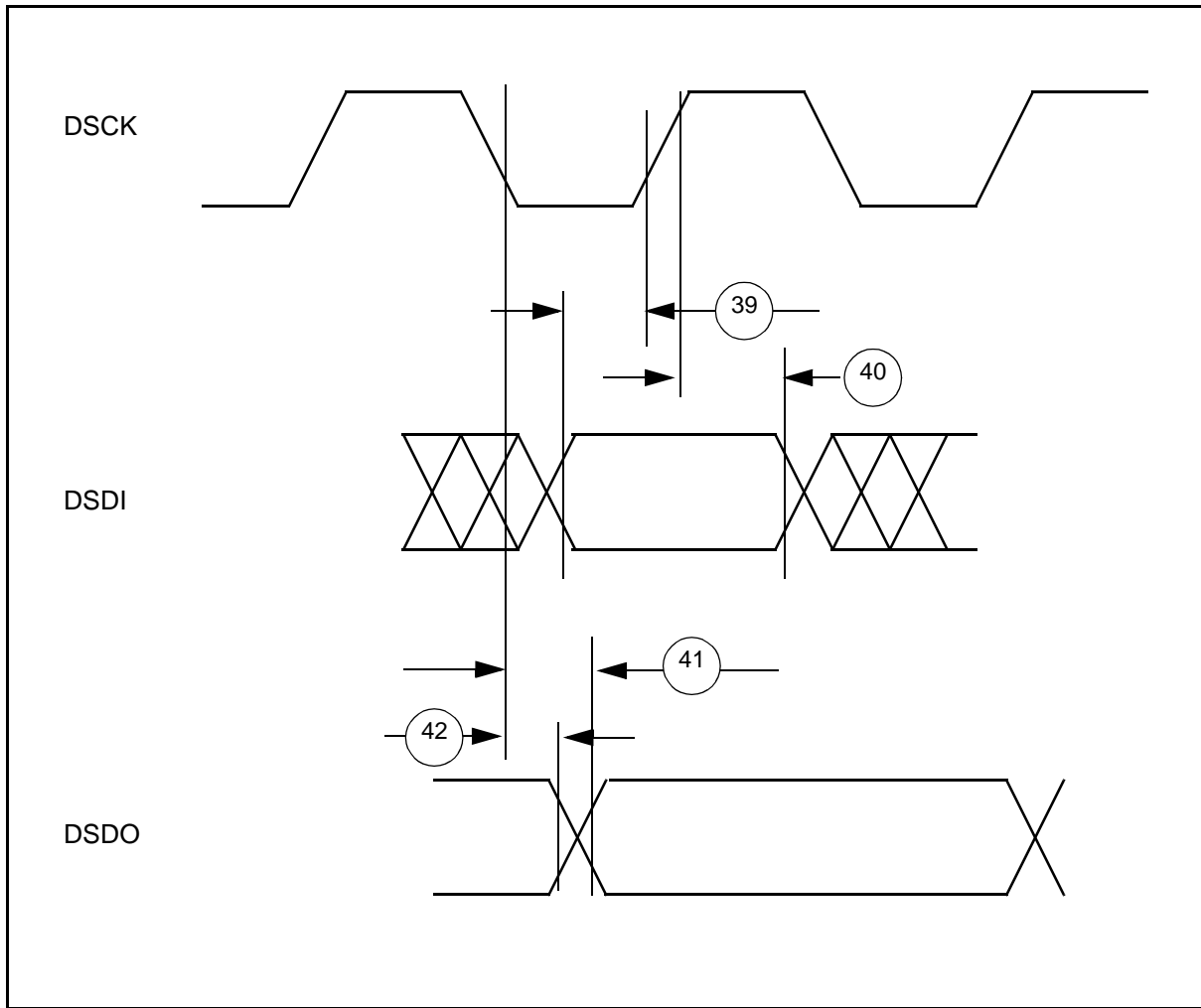
( $T_A = T_L$  to  $T_H$ )

	Characteristic	Expression	33MHz		40MHz		Unit
			Min	Max	Min	Max	
36	DSCK Cycle Time		120	—	60	—	ns
37	DSCK Clock Pulse Width		50	—	25	—	ns
38	DSCK Rise and Fall Times		0	3	0	3	ns
39	DSDI Input Data Setup Time		15	—	15	—	ns
40	DSDI Data Hold Time		5	—	5	—	ns
41	DSCK low to DSDO Data Valid		0	15	0	15	ns
42	DSCK low to DSDO Invalid		0	—	0	—	ns



**Figure G-21 Debug Port Clock Input Timing**





**Figure G-22 Debug Port Timings**

## G.14 Reset Timing



### Table G-12 RESET Timing

( $T_A = T_L$  to  $T_H$ )

	Characteristic	Expression	33MHz		40MHz		Unit
			Min	Max	Min	Max	
43	CLKOUT to $\overline{\text{HRESET}}$ High Impedance			20		20	ns
44	CLKOUT to $\overline{\text{SRESET}}$ High Impedance			20		20	ns
45	$\overline{\text{RSTCONF}}$ Pulse Width	$17 \cdot TC$	515		425		ns
46	Configuration Data to $\overline{\text{HRESET}}$ Rising Edge Setup Time	$15 \cdot TC + TCC$	463		382		ns
47	Configuration Data to $\overline{\text{RSTCONF}}$ Rising Edge Set Up Time	$15 \cdot TC + TCC$	463		382		ns
48	Configuration Data Hold Time After $\overline{\text{RSTCONF}}$ Negation		0		0		ns
49	Configuration Data Hold Time After $\overline{\text{HRESET}}$ Negation		0		0		ns
49a	$\overline{\text{RSTCONF}}$ Hold Time After $\overline{\text{HRESET}}$ Negation <sup>1</sup>		<b>TBD</b>		<b>TBD</b>		ns
50	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ Asserted to Data Out Drive		25		25		ns
51	$\overline{\text{RSTCONF}}$ Negated to Data Out High Impedance.		25		25		ns
52	CLKOUT of Last Rising Edge Before Chip Tristates $\overline{\text{HRESET}}$ to Data Out High Impedance.		25		25		ns
53	DSDI, DSCK Set Up	$3 \cdot TC$	91		75		ns
54	DSDI, DSCK hold time		0		0		ns
55	$\overline{\text{SRESET}}$ Negated to CLKOUT Rising Edge for DSDI and DSCK Sample	$8 \cdot TC$	243		200		ns
55a	$\overline{\text{HRESET}}$ , $\overline{\text{SRESET}}$ , $\overline{\text{PORESET}}$ Pulse Width <sup>2</sup>				100		ns

#### NOTES:

1. Weak pullups and pulldowns used for Reset timing will comply with the 130  $\mu\text{A}$  mode select current outlined in [Table G-4](#). The simplest way to insure meeting this requirement in systems that require the use of the TEXP function, is to connect  $\overline{\text{RSTCONF}}$ /TEXP to  $\overline{\text{SRESET}}$ .
2.  $\overline{\text{HRESET}}$ ,  $\overline{\text{SRESET}}$  and  $\overline{\text{PORESET}}$  have a glitch detector to ensure that spikes less than 20 ns are rejected. The internal  $\overline{\text{HRESET}}$ ,  $\overline{\text{SRESET}}$  and  $\overline{\text{PORESET}}$  will assert only if these signals are asserted for more than 100 ns

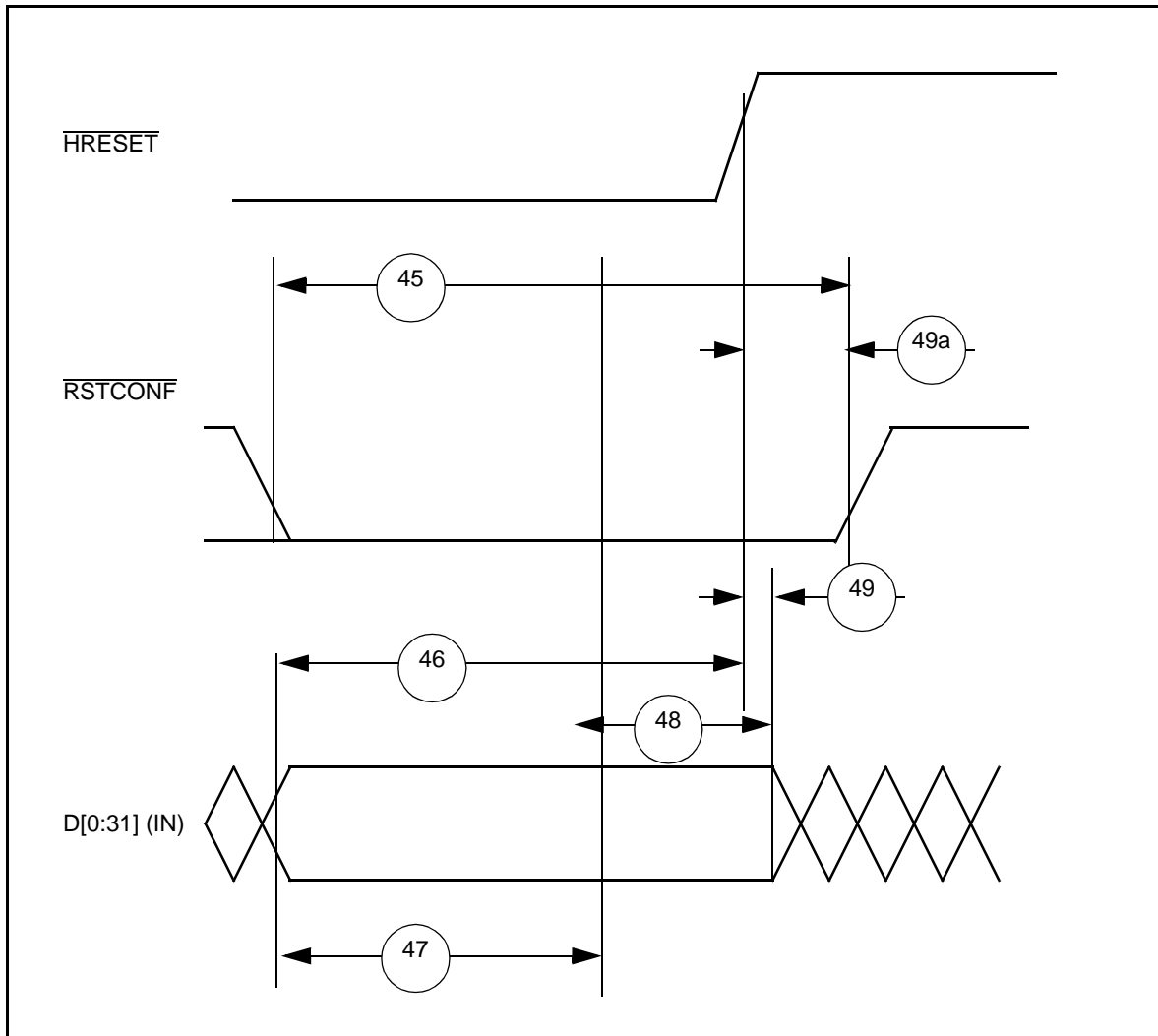
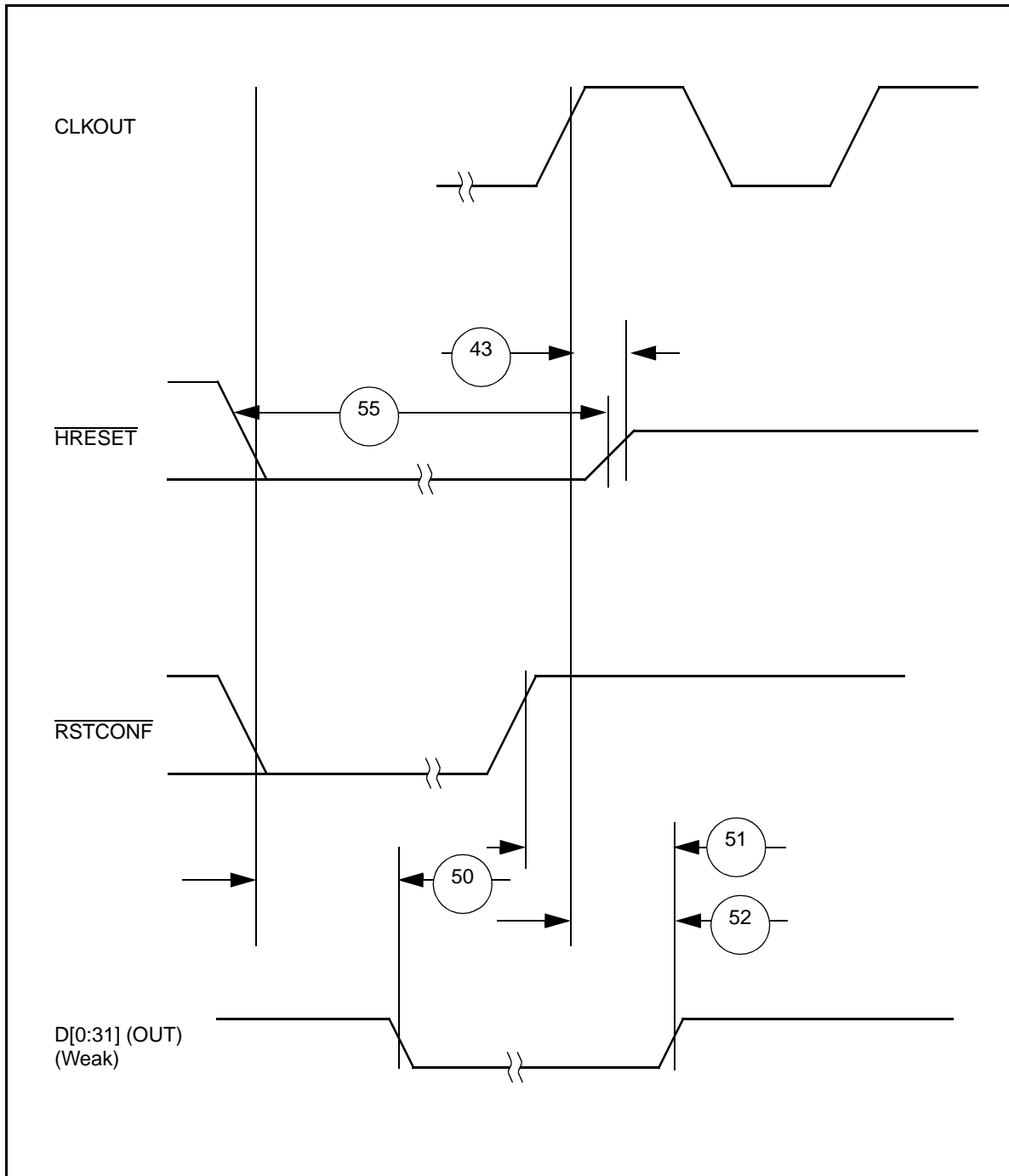
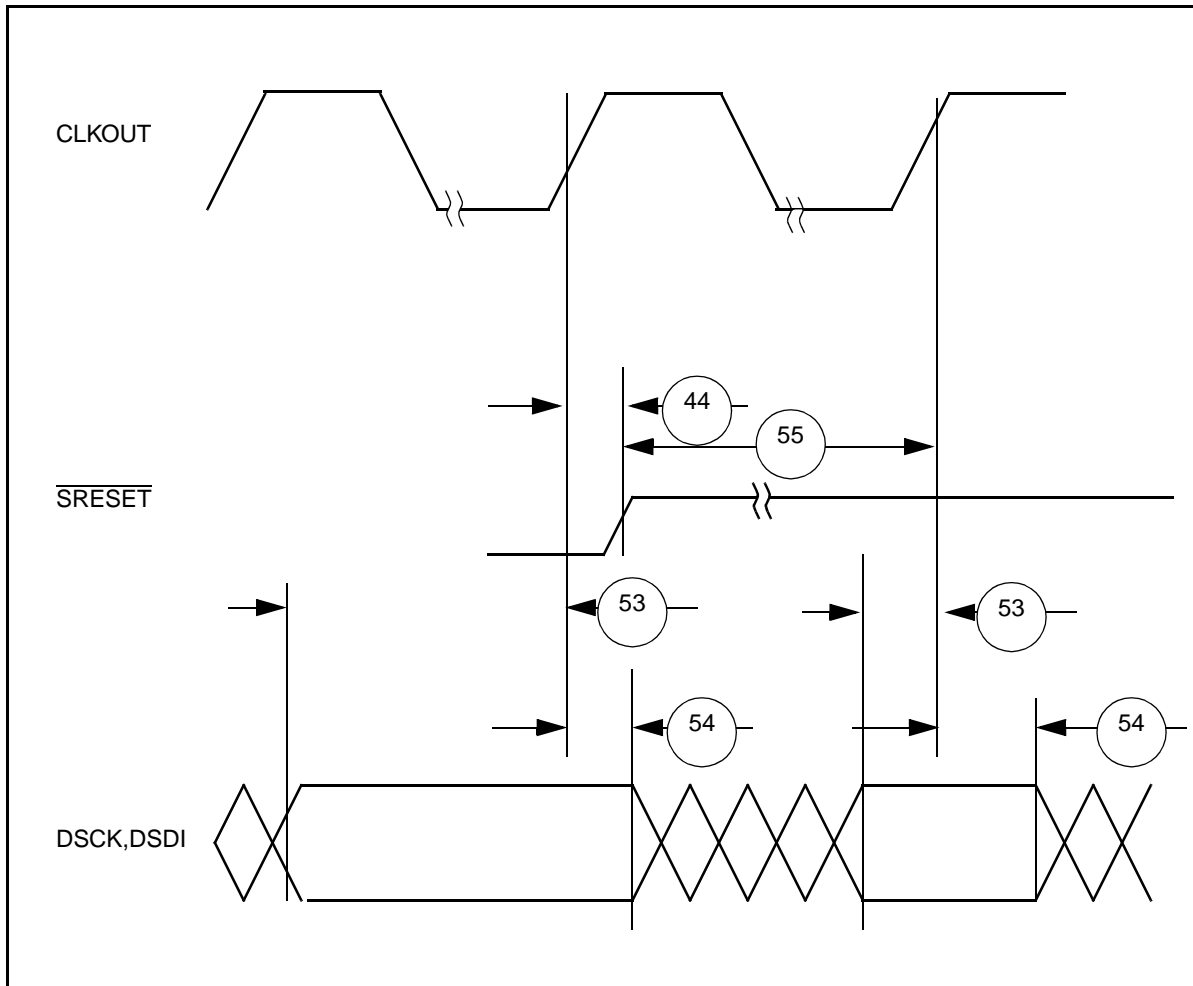


Figure G-23 Reset Timing — Configuration from Data Bus



**Figure G-24 Reset Timing — Data Bus Weak Drive during Configuration**



**Figure G-25 Reset Timing — Debug Port Configuration**

## G.15 IEEE 1149.1 Electrical Characteristics



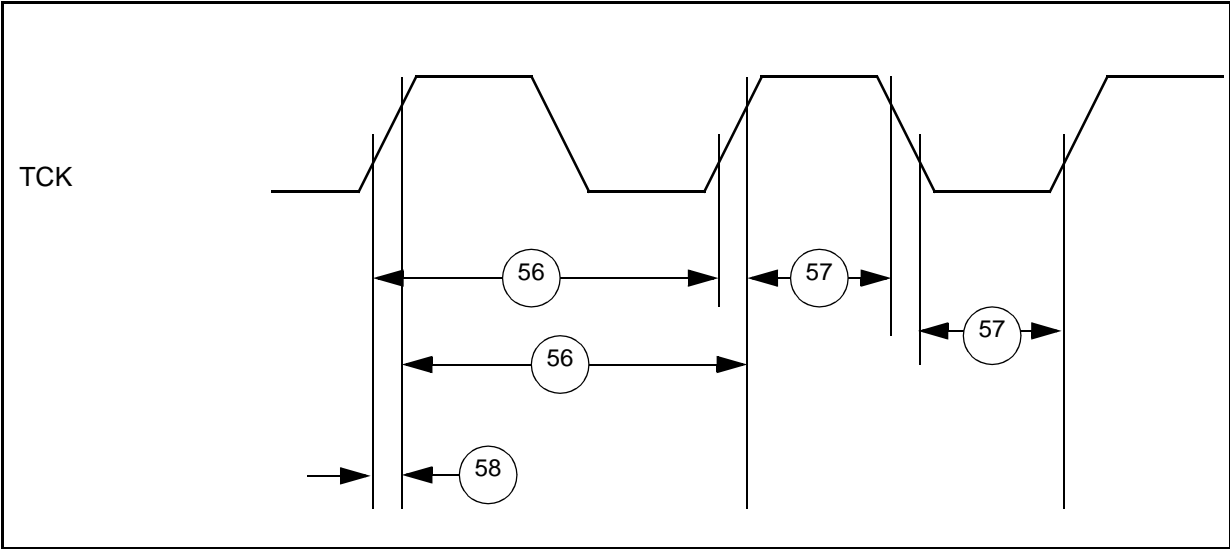
### Table G-13 JTAG timing<sup>1</sup>

( $T_A = T_L$  to  $T_H$ )

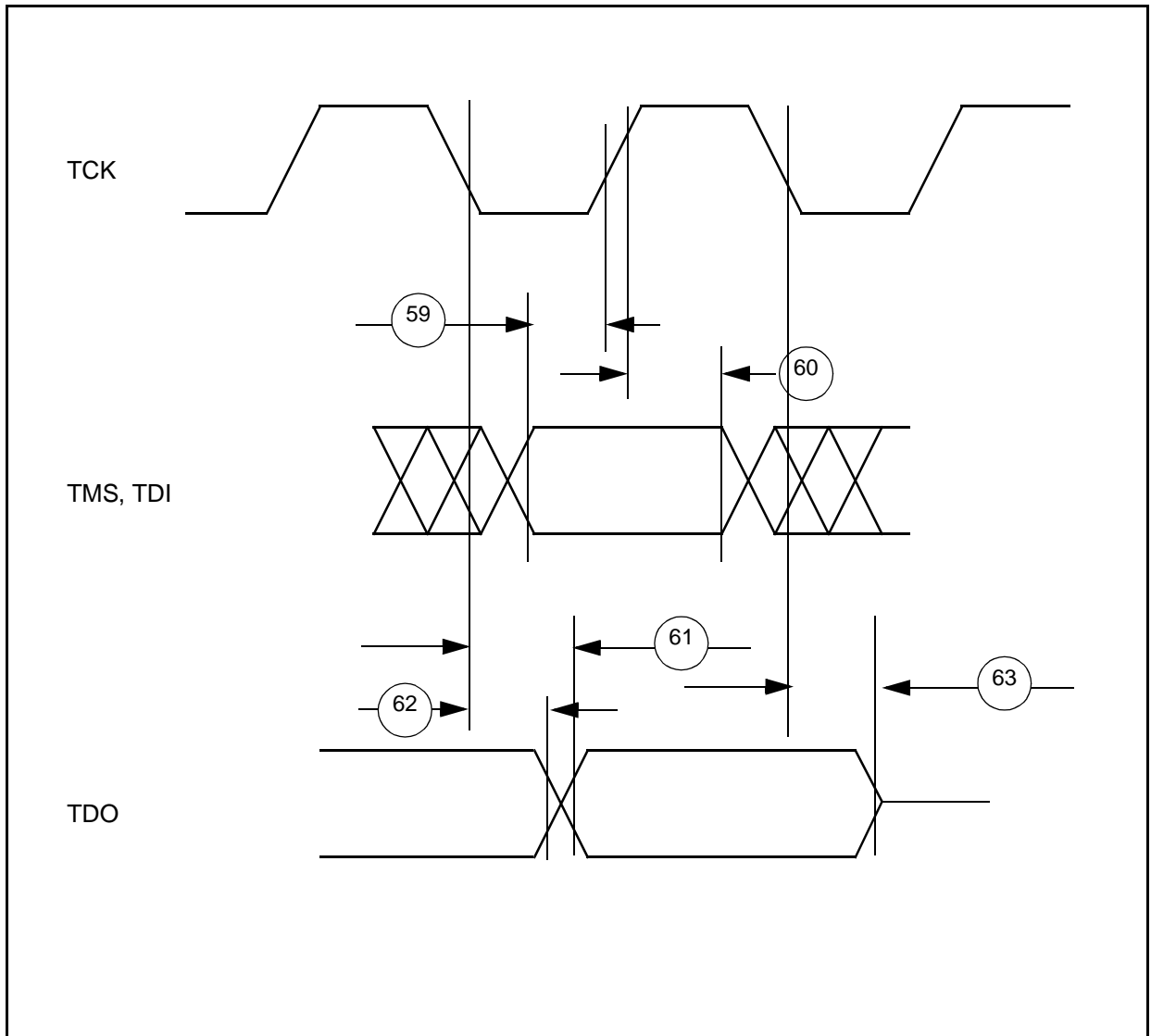
	Characteristic	Expression	33MHz		40MHz		Unit
			Min	Max	Min	Max	
56	TCK Cycle Time		—	100	—	100	ns
57	TCK Clock Pulse Width Measured at $V_{DD}/2$		—	40	—	40	ns
58	TCK Rise and Fall Times		0	10	0	10	ns
59	TMS, TDI Data Setup Time		5	—	5	—	ns
60	TMS, TDI Data Hold Time		25	—	25	—	ns
61	TCK Low to TDO Data Valid		—	20	—	20	ns
62	TCK Low to TDO Data Invalid		0	—	0	—	ns
63	TCK Low to TDO High Impedance		—	20	—	20	ns
64	$\overline{\text{TRST}}$ Assert Time		100	—	100	—	ns
65	$\overline{\text{TRST}}$ Setup Time to TCK Low		40	—	40	—	ns
66	TCK Falling Edge to Output Valid		—	50	—	50	ns
67	TCK Falling Edge to Output Valid out of High Impedance		—	50	—	50	ns
68	TCK Falling Edge to Output High Impedance		—	50	—	50	ns
69	Boundary Scan Input Valid to TCK Rising Edge		50	—	50	—	ns
70	TCK Rising Edge to Boundary Scan Input Invalid		50	—	50	—	ns

#### NOTES:

1. JTAG timing is only tested at 10 MHz

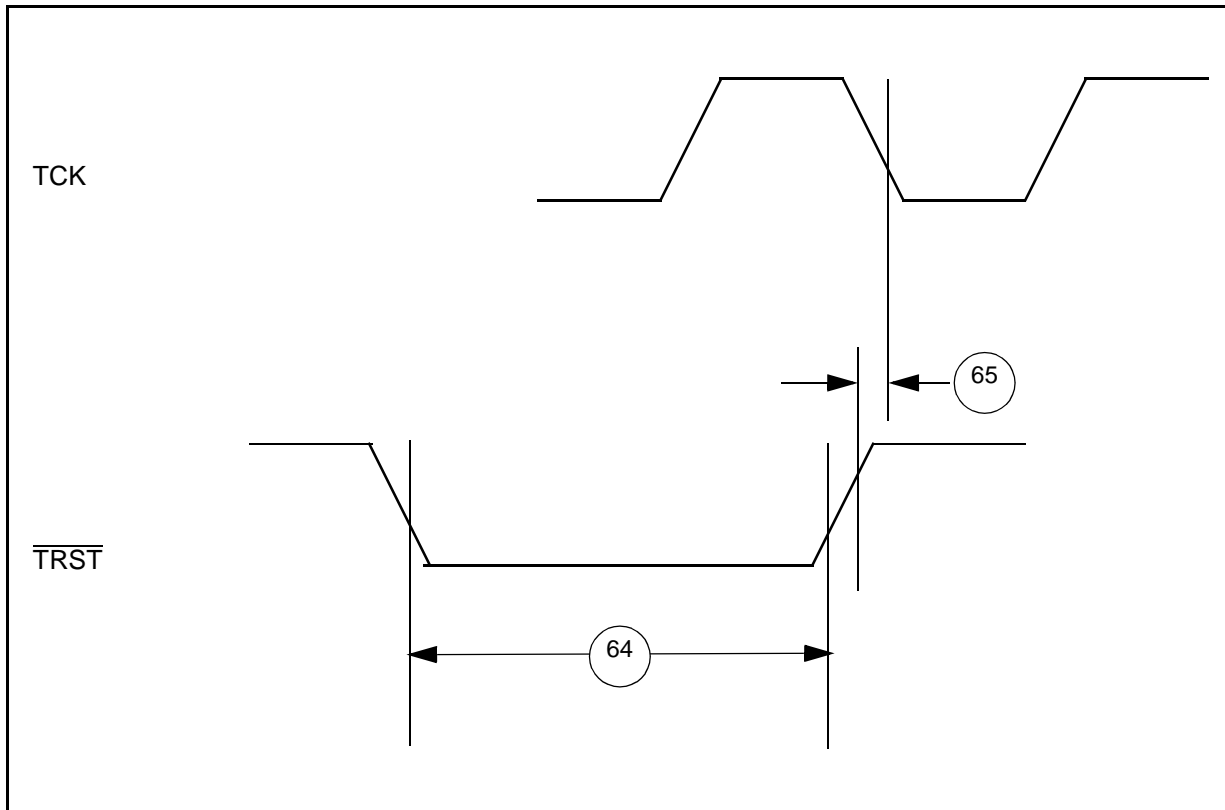


**Figure G-26 JTAG Test Clock Input Timing**

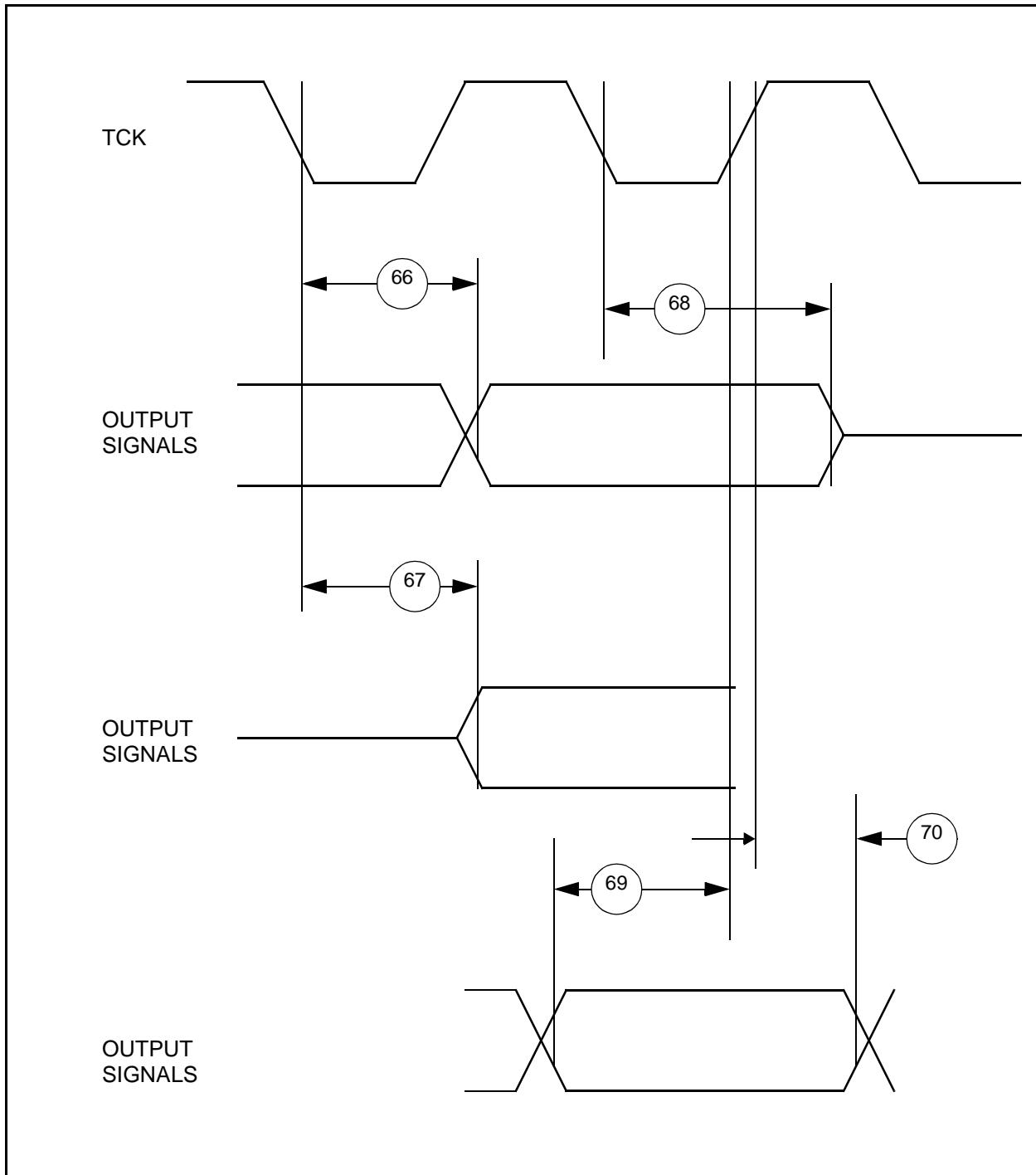


**Figure G-27 JTAG-Test Access Port Timing Diagram**





**Figure G-28 JTAG- $\overline{\text{TRST}}$  Timing Diagram**



**Figure G-29 Boundary Scan (JTAG) Timing Diagram**

## G.16 QADC64 Electrical Characteristics



**Table G-14 QADC64 Conversion Characteristics (Operating)**

( $T_A = T_L$  to  $T_H$ )

Num	Parameter	Symbol	Min	Max	Units
97	QADC Clock (QCLK) Frequency <sup>1</sup>	$F_{QCLK}$	0.5	3.0	MHz
98	Conversion Cycles <sup>2</sup>	CC	14	28	QCLK cycles
99	Conversion Time <sup>3</sup> $F_{QCLK} = 2.0$ MHz <sup>1,4</sup> Min = CCW/IST = 0b00 Max = CCW/IST = 0b11	$T_{CONV}$	7.0	14.0	$\mu$ s
100	Stop Mode Recovery Time	$T_{SR}$	—	10	$\mu$ s
101	Resolution <sup>5</sup>	—	5	—	mV
102	Absolute (Total Unadjusted) Error <sup>6, 7, 8, 9</sup> $F_{QCLK} = 2.0$ MHz <sup>3</sup> , 2 Clock Input Sample Time	AE	-2	2	Counts
103	DC Disruptive Input Injection Current <sup>10, 11, 12, 13, 14</sup>	$I_{INJ}^{15}$ $I_{INJ}^{16}$	-3 -1	3 1	mA
104	Current Coupling Ratio <sup>17</sup> PQA PQB	K	— —	$8 \times 10^{-5}$ $8 \times 10^{-5}$	
105	Incremental Error Due to Injection Current All Channels Have Same 10 k $\Omega$ < $R_s$ < 100 k $\Omega$ Channel Under Test has $R_s = 10$ k $\Omega$ , $I_{INJ} = \pm 3$ mA	$E_{INJ}$		$\pm 1.0$ $\pm 1.0$	Counts
106	Source Impedance At Input <sup>18</sup>	$R_S$	—	100	k $\Omega$
107	Incremental Capacitance During Sampling <sup>19</sup>	$C_{SAMP}$	—	5	pF

**NOTES:**

- Conversion characteristics vary with  $F_{QCLK}$  rate. Reduced conversion accuracy occurs at max  $F_{QCLK}$  rate.
- The number of conversion cycles is dependent on the IST bits in the CCW register.
- Assumes that  $f_{SYS} = 40$  MHz
- Assumes  $F_{QCLK} = 2.00$  MHz, with clock prescaler values of:  
QACR0: PSH = 0b01111, PSA = 0b0, PSL = 0b011)  
CCW: BYP = 0b0
- At  $V_{RH} - V_{RL} = 5.12$  V, one count = 5 mV.
- Accuracy tested and guaranteed at  $V_{RH} - V_{RL} = 5.0V \pm 0.5$  V
- This parameter is periodically sampled rather than 100% tested.
- Absolute error includes 1/2 count (~2.5 mV) of inherent quantization error and circuit (differential, integral, and offset) error. Characteristic assumes that adequate low-pass filtering is present on analog input pins — capacitive filter with 0.01  $\mu$ F to 0.1  $\mu$ F capacitor between analog input and analog ground, typical source isolation impedance of 10 K $\Omega$ .
- Input signals with large slew rates or high frequency noise components cannot be converted accurately. These signals may affect the conversion accuracy of other channels.
- Below disruptive current conditions, the channel being stressed has conversion values of \$3FF for analog inputs greater than  $V_{RH}$  and \$000 for values less than  $V_{RL}$ . This assumes that  $V_{RH} \leq V_{DDA}$  and  $V_{RL} \leq V_{SSA}$  due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.
- Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.



12. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using  $V_{POSCLAMP} = (\text{the lower of } V_{DDA} \text{ or } V_{DDH}) + 0.3 \text{ V}$  and  $V_{NEGCLAMP} = -0.3 \text{ V}$ , then use the larger of the calculated values. The diode drop voltage is a function of current and varies approximately 0.4 to 0.8 volts over temperature
13. This parameter is periodically sampled rather than 100% tested.
14. Derate linearly to 0.3 mA if  $V_{DDH} - V_{DDA} = 1 \text{ volt}$ . This characteristic is preliminary and may change after further characterization.
15. Condition applies to two adjacent pins.
16. Condition applies to all analog channels.
17. Current coupling ratio, K, is defined as the ratio of the output current,  $I_{out}$ , measured on the pin under test to the injection current,  $I_{inj}$ , when both adjacent pins are overstressed with the specified injection current.  $K = I_{out} / I_{inj}$   
The input voltage error on the channel under test is calculated as  $V_{err} = I_{inj} * K * R_S$
18. Maximum source impedance is application-dependent. Error resulting from pin leakage depends on junction leakage into the pin and on leakage due to charge-sharing with internal capacitance.  
Error from junction leakage is a function of external source impedance and input leakage current. In the following expression, expected error in result value due to junction leakage is expressed in voltage ( $V_{errj}$ ):  
$$V_{errj} = R_S * I_{OFF}$$
where  $I_{OFF}$  is a function of operating temperature.  
Charge-sharing leakage is a function of input source impedance, conversion rate, change in voltage between successive conversions, and the size of the filtering capacitor used. Error levels are best determined empirically. In general, continuous conversion of the same channel may not be compatible with high source impedance
19. For a maximum sampling error of the input voltage  $\leq 1\text{LSB}$ , then the external filter capacitor,  $C_f \geq 1024 * C_{SAMP}$ . The value of  $C_{SAMP}$  in the new design may be reduced.

## G.17 QSMCM Electrical Characteristics

**Table G-15 QSPI Timing**

( $T_A = T_L$  to  $T_H$ , 50 pF load on all QSPI pins)

Name	Function	Symbol	Min	Max	Unit
108	Operating Frequency <sup>1</sup> Master Slave	$f_{op}$	DC DC	$f_{sys}/4$ $f_{sys}/4$	Hz
109	Cycle Time Master Slave	$t_{qcyc}$	4*TC 4*TC	510*TC <sup>2</sup> —	ns
110	Enable Lead Time Master Slave	$t_{lead}$	2*TC 2*TC	128*TC —	ns
111	Enable Lag Time Master Slave	$t_{lag}$	— 2*TC	SCK/2 —	ns
112	Clock (SCK) High or Low Time Master Slave <sup>3</sup>	$t_{sw}$	2*TC – 60 2*TC – n	255*TC —	ns
113	Sequential Transfer Delay Master Slave (Does Not Require Deselect)	$t_{td}$	17*TC 13*TC	8192*TC —	ns
114	Data Setup Time (Inputs) Master Slave	$t_{su}$	30 20	— —	ns

**Table G-15 QSPI Timing (Continued)**

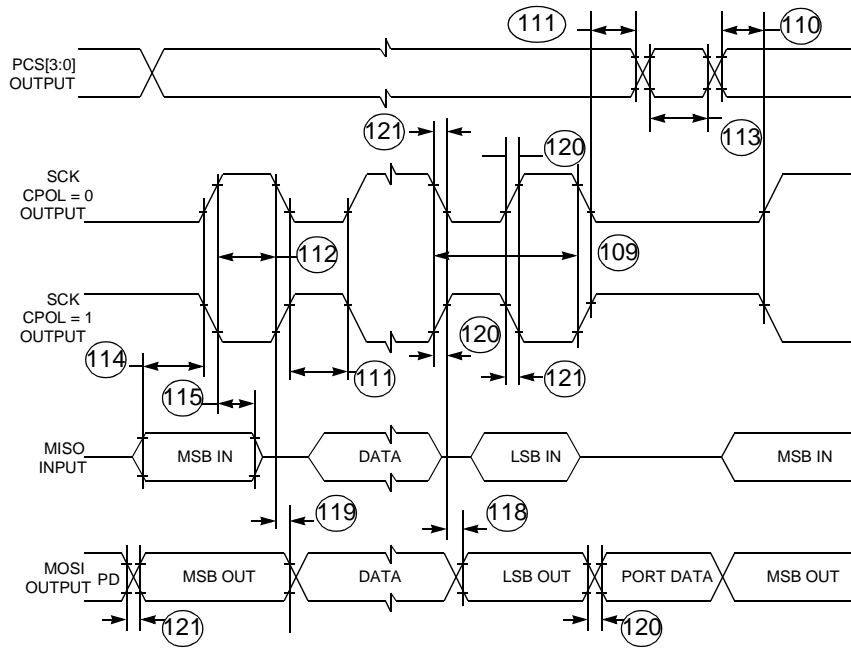
( $T_A = T_L$  to  $T_H$ , 50 pF load on all QSPI pins)



Name	Function	Symbol	Min	Max	Unit
115	Data Hold Time (Inputs) Master Slave	$t_{hi}$	0 20	— —	ns
116	Slave Access Time	$t_a$	—	TC	ns
117	Slave MISO Disable Time	$t_{dis}$	—	2*TC	ns
118	Data Valid (After SCK Edge) Master Slave	$t_v$	— —	50 50	ns
119	Data Hold Time (Outputs) Master Slave	$t_{ho}$	0 0	— —	ns
120	Rise Time Input  Output up to 50 pF Load, SLRC Bit of PDMCR = "0" up to 200 pF Load, SLRC Bit of PDMCR = "0" up to 50 pF, SLRC Bit of PDMCR = "1"	$t_{ri}$  $t_{ro}$	—  10 20 2	1  50 100 25	$\mu$ s  ns ns ns
121	Fall Time Input  Output up to 50 pF Load, SLRC Bit of PDMCR = "0" up to 200 pF Load, SLRC Bit of PDMCR = "0" up to 50 pF, SLRC Bit of PDMCR = "1"	$t_{fi}$  $t_{fo}$	—  10 20 2	1  50 100 25	$\mu$ s  ns ns ns

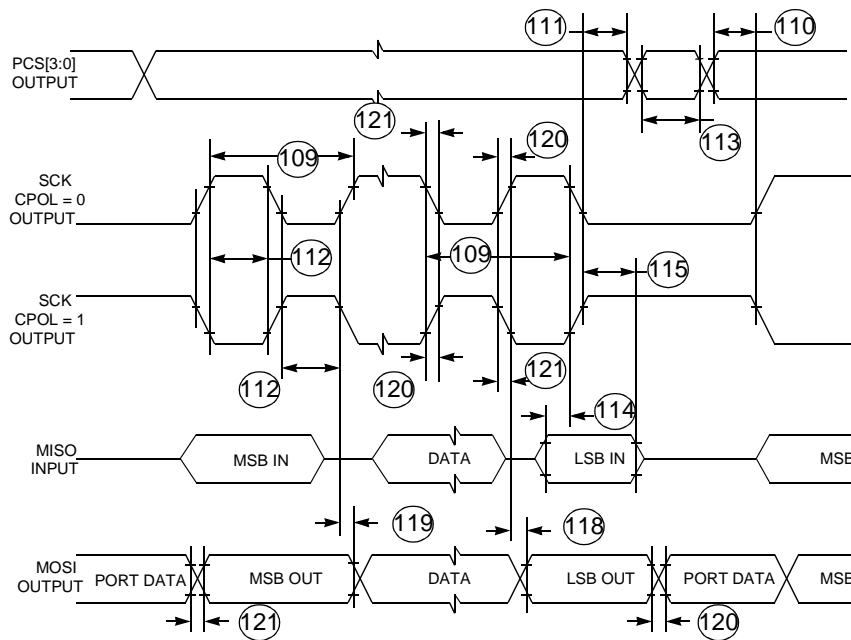
NOTES:

1. All AC timing is tested to the 3-V levels outlined in [Table G-4](#).
2. TC is defined to be the clock period.
3. For high time, n = External SCK rise time; for low time, n = External SCK fall time.



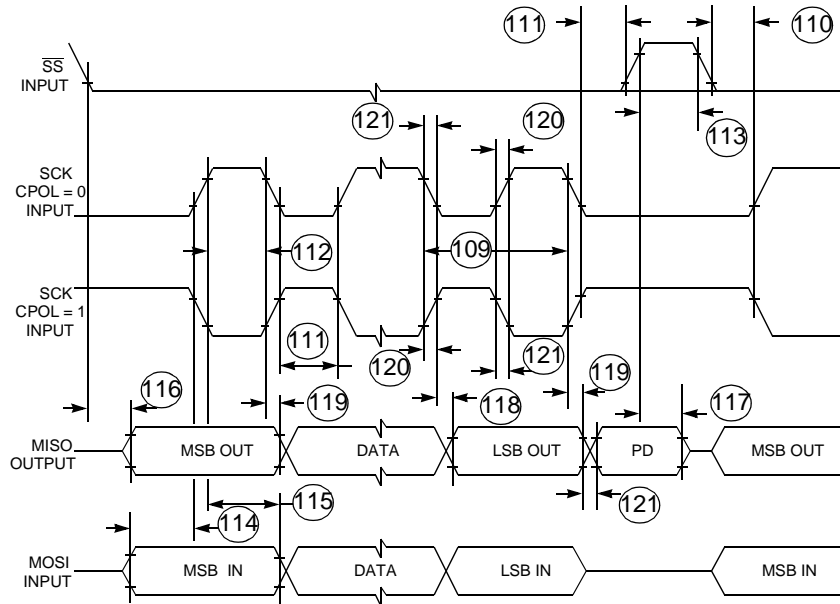
QSPI MAST CPHA0

**Figure G-30 QSPI Timing — Master, CPHA = 0**



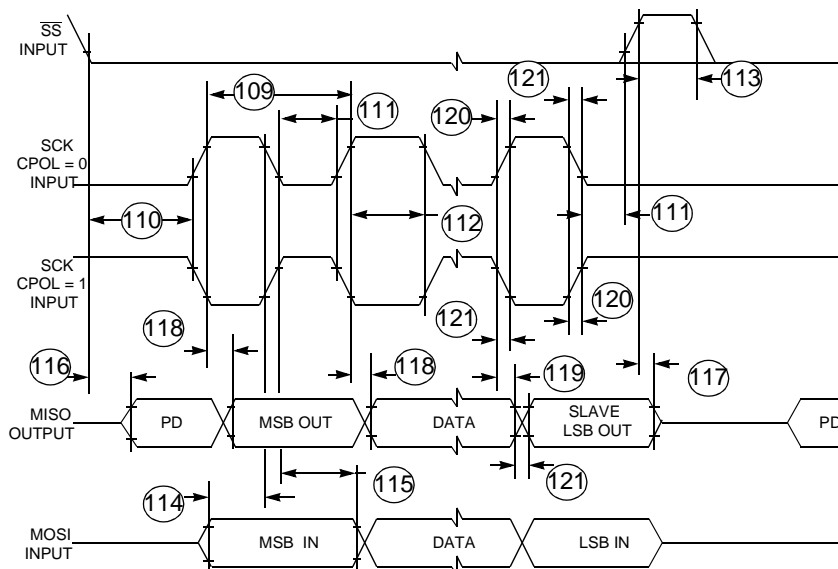
QSPI MAST CPHA1

**Figure G-31 QSPI Timing — Master, CPHA = 1**



QSPI SLV CPHA0

**Figure G-32 QSPI Timing — Slave, CPHA = 0**



QSPI SLV CPHA1

**Figure G-33 QSPI Timing — Slave, CPHA = 1**

## G.18 GPIO Electrical Characteristics



**Table G-16 GPIO Timing<sup>1</sup>**

( $T_A = T_L$  to  $T_H$ )

Num	Rating	Symbol	Min	Max	Unit
122	Rise Time Input	$t_{ri}$	—	1	$\mu$ s
	Output <sup>2</sup> (SLR0 of PDMCR = 0), up to 50 pF to up to 200 pF Load	$t_{ro}$	90	600	ns
	Output <sup>2</sup> (SLR0 of PDMCR = 0), up to 20 nF Load <sup>3</sup>		2000	7500	ns
	Output (SLR0 of PDMCR = 1), up to 50 pF Load		3	25	ns
123	Fall Time Input	$t_{fi}$	—	1	$\mu$ s
	Output <sup>2</sup> (SLR0 of PDMCR = 0), up to 50 pF to up to 200 pF Load	$t_{fo}$	90	600	ns
	Output <sup>2</sup> (SLR0 of PDMCR = 0), up to 20 nF Load <sup>3</sup>		2000	7500	ns
	Output (SLR0 of PDMCR = 1), up to 50 pF Load			25	ns

**NOTES:**

- GPIO applies to all pins used as GPIO: SGPIOA[8:31], SQPIOD[0:31], SGPIOC[0:7], QGPIO[0:6], QGPO[1:2], MPIO[0:15], A\_PQA[0:7], B\_PQA[0:7].
- This parameter is tested during initial characterization and is not tested in production.
- Care should be taken to insure that the total power dissipation of the device remain below the absolute maximum rating under this condition. See [Table G-1](#). With a capacitive load > 20 nF (up to 100 nF maximum), the user must insure that the pin is always configured as an output and set to slow slew rate mode (SLR0 of PDMCR = 0). Do not change SLR0 of PDMCR to a 1 under these conditions.

## G.19 TPU3 Electrical Characteristics

**Table G-17 TPU3 Timing**

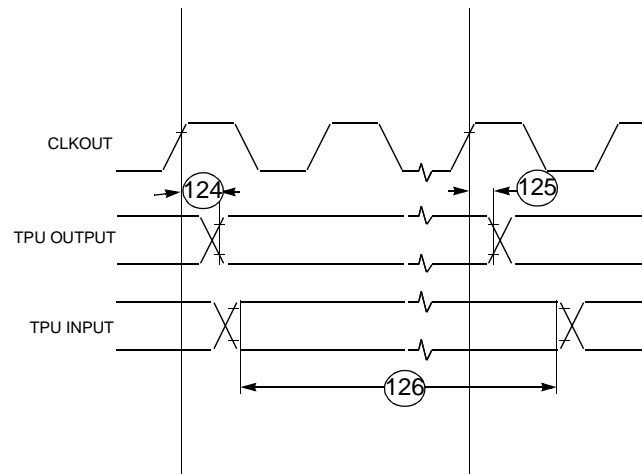
( $T_A = T_L$  to  $T_H$ )

Num	Rating	Symbol	Min	Max	Unit
124	Slew Rate of TPU Output Channel Valid <sup>1,2</sup> (SLR0 of PDMCR = 0, 50 pF to 200 pF Load) (SLR0 of PDMCR = 0, 20 nF Load) <sup>3</sup> (SLR0 of PDMCR = 1, 50 pF Load)	$t_{CHTOV}$	92 2000 3	650 7550 25	ns
125	CLKOUT High to TPU Output Channel Hold	$t_{CHTOH}$	0	15	ns
126	TPU Input Channel Pulse Width <sup>4</sup>	$t_{TIPW}$	4	—	$t_{cyc}$

**NOTES:**

- AC timing is shown with respect to 10%  $V_{DD}$  and 90%  $V_{DD}$  levels. Total slew rate from 0 to  $V_{DD}$  will be larger.
- Timing not valid for external T2CLK input.
- Care should be taken to insure that the total power dissipation of the device remain below the absolute maximum rating under this condition. See [Table G-1](#). With a capacitive load > 20 nF, the user must insure that the pin is always configured as an output.
- $t_{cyc}$  is defined as the CLKOUT Period.





**Figure G-34 TPU3 Timing**

## G.20 TOUCAN Electrical Characteristics

**Table G-18 TOUCAN Timing<sup>1</sup>**

( $T_A = T_L$  to  $T_H$ )

Num	Rating	Symbol	Min	Max	Unit
127	CNTX0 (Delay from ICLOCK)	$t_{CNTX0}$	19	—	ns
128	CNRX0 (Set-Up to ICLOCK Rise)	$t_{CNRX0}$	0	—	ns
120	Rise Time Input	$t_{ri}$	—	1	$\mu$ s
	Output	$t_{ro}$			
	50 pF Load, SLRC Bit of PDMCR = "0"		10	50	ns
	200 pF Load, SLRC Bit of PDMCR = "0"		20	100	ns
	50 pF, SLRC Bit of PDMCR = "1"		2	25	ns
121	Fall Time Input	$t_{fi}$	—	1	$\mu$ s
	Output	$t_{fo}$			
	50 pF Load, SLRC Bit of PDMCR = "0"		10	50	ns
	200 pF Load, SLRC bit of PDMCR = "0"		20	100	ns
	50 pF, SLRC Bit of PDMCR = "1"		2	25	ns
	Serial Pins (Maximum Frequency)	$t_f$	1	—	Mhz

NOTES:

1. AC timing is shown is tested to the 3-V levels outlined in [Table G-4](#).

## G.21 MIOS Timing Characteristics

All MIOS output pins are slew rate controlled. Slew rate control circuitry adds 90 ns as minimum to the output timing and 650 ns as a maximum. This slew rate is from 10%  $V_{DD}$  to 90%  $V_{DD}$ , an additional 100 ns should be added for total 0 to  $V_{DD}$  slew rate.

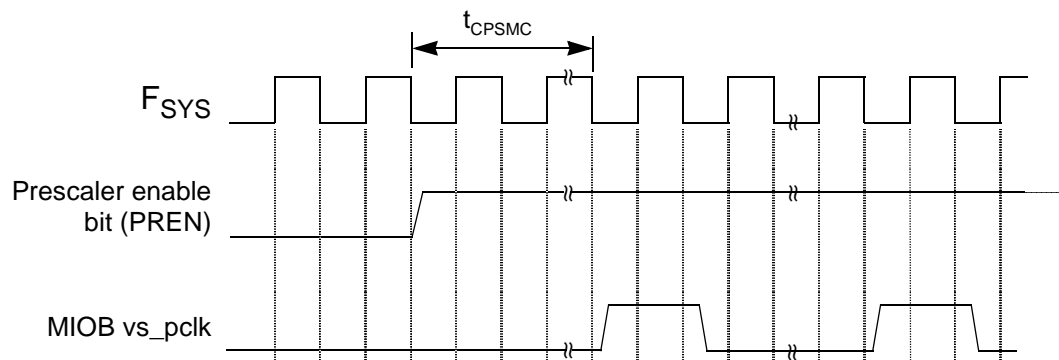


**Table G-19 MCPSM Timing Characteristics**

Characteristic	Symbol	Delay	Unit
MCPSM Enable to vs_pclk Pulse <sup>1</sup>	$t_{CPSMC}$	(MCPSMSCR_PSL[3:0]) - 1 <sup>2</sup>	System Clock Cycles

**NOTES:**

- The MCPSM clock prescaler value (MCPSMSCR\_PSL[3:0]) should be written to the MCPSMSCR (MCPSM status/control register) before rewriting the MCPSMSCR to set the enable bit (MCPSMSCR\_PREN). If this is not done the prescaler will start with the old value in the MCPSMSCR\_PSL[3:0] before reloading the new value into the counter.  
vs\_pclk is the MIOS prescaler clock which is distributed to all the counter (e.g., MPWMSM and MMCSM) submodules.
- After reset MCPSMSCR\_PSL[3:0] is set to 0b0000.



Note 1:  $F_{SYS}$  is the internal system clock for the IMB3 bus.

Note 2: The numbers associated with the  $F_{SYS}$  ticks refer to the IMB3 internal state.

Note 3: vs\_pclk is the MIOS prescaler clock which is distributed around the MIOS to counter modules such as the MMCSM and MPWMSM.

**Figure G-35 MCPSM Enable to vs\_pclk Pulse Timing Diagram**

## G.21.1 MPWMSM Timing Characteristics



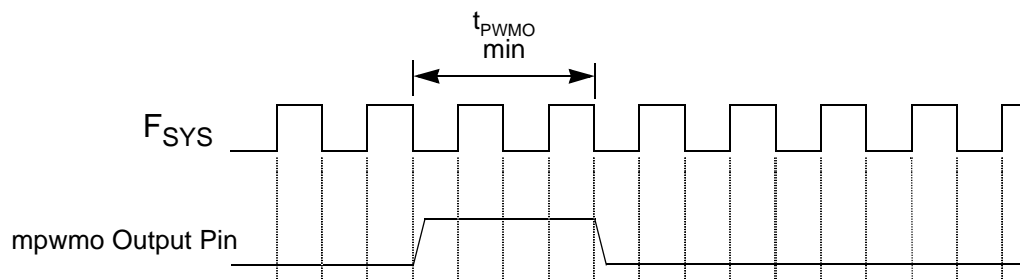
### Table G-20 MPWMSM Timing Characteristics

(All delays are in system clock periods)

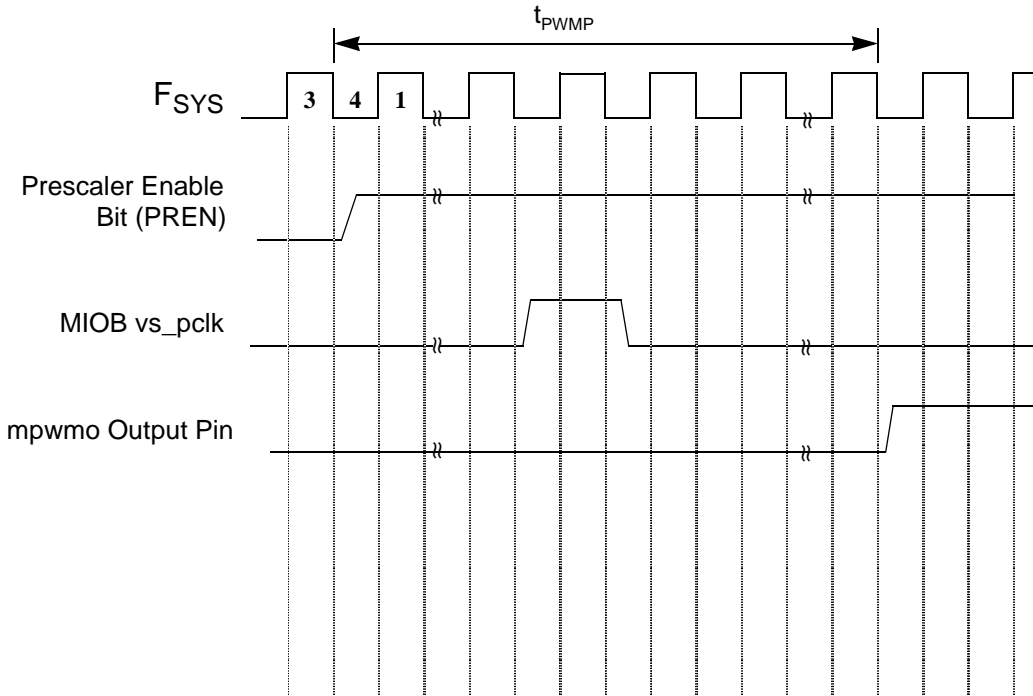
Characteristic	Symbol	Min	Max
PWMSM Output Resolution	$t_{PWMR}$	1	2.0 <sup>2</sup>
PWM Output Pulse <sup>3</sup>	$t_{PWMO}$	2.0	—
mpwmi Input Pin to MPWMSCR_PIN Status Set	$t_{PIN}$	1	2
CPSM Enable To Output Set <sup>4</sup>	$t_{PWMP}$	$(MPWMPERR - MPWMPULR + 1) * (256 - MPWMSCR\_CP) * MCPSMSCR\_PSL + 1$	
MPWMSM Enable to Output Set (MIN) <sup>5</sup>	$t_{PWME}$	$(MPWMPERR - MPWMPULR) * (256 - MPWMSCR\_CP) * MCPSMSCR\_PSL + 3 + (255 - MPWMSCR\_CP) * MCPSMSCR\_PSL$ <sup>6</sup>	
MPWMSM Enable to Output Set (MAX) <sup>5</sup>	$t_{PWME}$	$t_{PWME}(\text{MIN}) + MCPSMSCR\_PSL - 1$ <sup>6</sup>	
Interrupt Flag to Output Pin Reset (Period Start) <sup>7</sup>	$t_{FLGP}$	$(256 - MPWMSCR\_CP) * MCPSMSCR\_PSL - 1$ <sup>6</sup>	

#### NOTES:

1. Minimum output resolution depends on MPWMSM and MCPSM prescaler settings.
2. Maximum resolution is obtained by setting CPSMPSL[3:0] = 0x2 and MPWMSCR\_CP[7:0] = 0xFF.
3. Excluding the case where the output is always "0".
4. With MPWMSM enabled before enabling the MCPSM. Please also see Note \*1 on the MCPSM timing information.
5. The exact timing from mpwmsm enable to the pin being set depends on the timing of the register write and the MCPSM vs\_pclk.
6. When MCPSMSCR\_PSL = 0x0000, this gives a prescale value of 16 and it is 16 which should be used in these calculations. When MCPSMSCR\_PSL = 0x0001, the CPSM is inactive.
7. Note: the interrupt is set before the output pin is reset (Signifying the start of a new period).

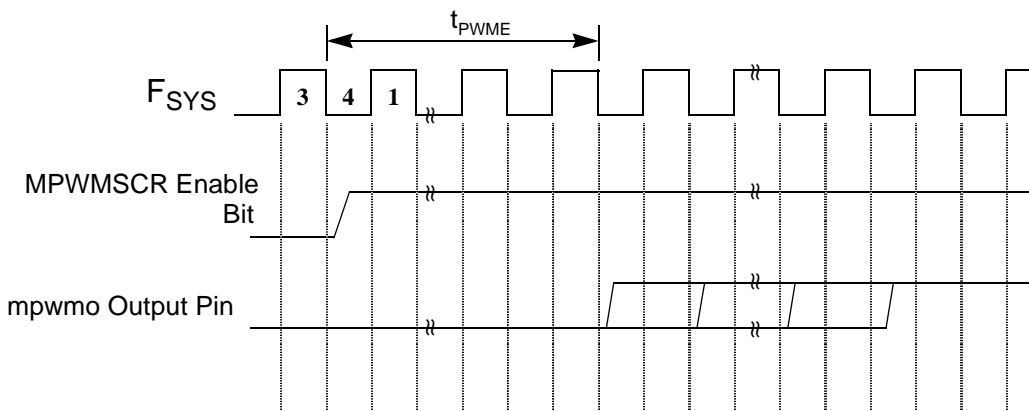


**Figure G-36 MPWMSM Minimum Output Pulse Example Timing Diagram**

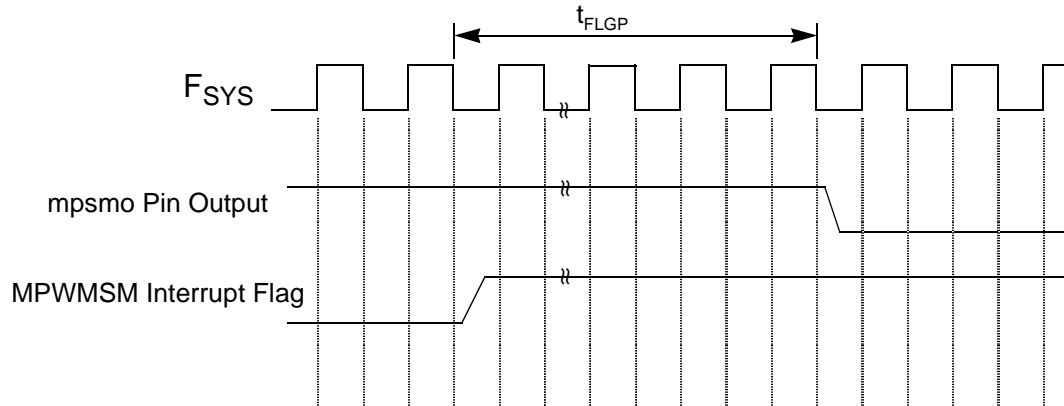


Note:  $F_{SYS}$  is the internal system clock for the IMB3 bus.

**Figure G-37 MCPSM Enable to MPWMO Output Pin Rising Edge Timing Diagram**



**Figure G-38 MPWMSM Enable to MPWMO Output Pin Rising Edge Timing Diagram**



**Figure G-39 MPWMSM Interrupt Flag to MPWMO Output Pin Falling Edge Timing Diagram**

## G.21.2 MMCSM Timing Characteristics

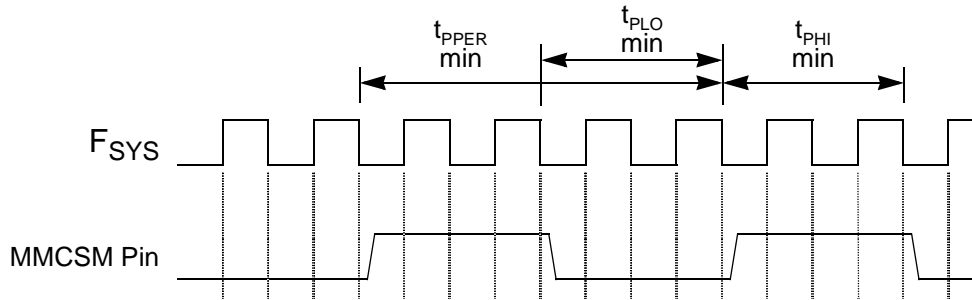
**Table G-21 MMCSM Timing Characteristics**

(All delays are in system clock periods.)

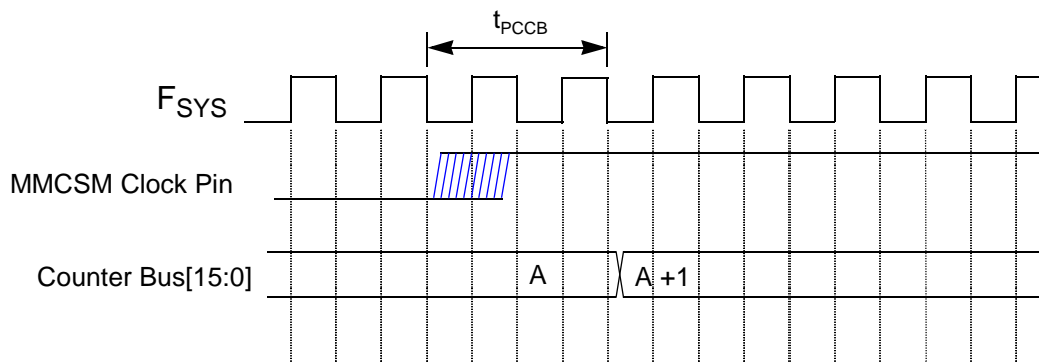
Characteristic	Symbol	Min	Max
MMCSM Input Pin Period	$t_{PPER}$	4	—
MMCSM Pin Low Time	$t_{PLO}$	2	—
MMCSM Pin High Time	$t_{PHI}$	2	—
Clock Pin to Counter Bus Increment	$t_{PCCB}$	1	2
Load Pin to New Counter Bus Value	$t_{PLCB}$	1	2
Clock Pin to PINC Delay	$t_{PINC}$	1	2
Load Pin to PINL Delay	$t_{PINL}$	1	2
Counter Bus Resolution	$t_{CBR}$	$-1$	$2^2$
Counter Bus Overflow Reload to Interrupt Flag	$t_{CBFLG}$	1	
MCPSM Enable to Counter Bus Increment	$t_{MCMP}$	$(256 - \text{MMCSMSCR\_CP}) * \text{MCPSMSCR\_PSL} + 2^3$	
MMCSM Enable to Counter Bus Increment (MIN) <sup>4</sup>	$t_{MCME}$	$4 + \text{MCPSMSCR\_PSL} * (255 - \text{MMCSMSCR\_CP})^3$	
MMCSM Enable to Counter Bus Increment (MAX) <sup>4</sup>	$t_{MCME}$	$4 + \text{MCPSMSCR\_PSL} * (255 - \text{MMCSMSCR\_CP}) + (\text{MCPSMSCR\_PSL} - 1)^3$	

**NOTES:**

1. Minimum output resolution depends on MMCSM and MCPSM prescaler settings.
2. Maximum resolution is obtained by setting  $\text{CPSMPSL}[3:0] = 0x2$  and  $\text{MMCSMSCR\_CP}[7:0] = 0xFF$ .
3. When  $\text{MCPSMSCR\_PSL} = 0x0000$ , this gives a prescale value of 16 and it is 16 which should be used in these calculations. When  $\text{MCPSMSCR\_PSL} = 0x0001$ , the CPSM is inactive.
4. The exact timing from MMCSM enable to the pin being set depends on the timing of the MMCSMSCR register write and the MCPSM vs\_pclk. The MMCSM enable is taken to mean the MMCSMSCR\_CLS[1:0] being written to 2'b11.

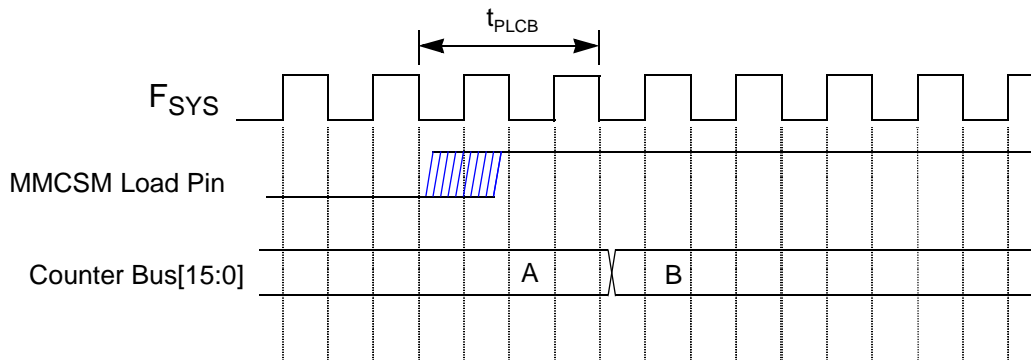


**Figure G-40 MMCSM Minimum Input Pin (Either Load or Clock) Timing Diagram**

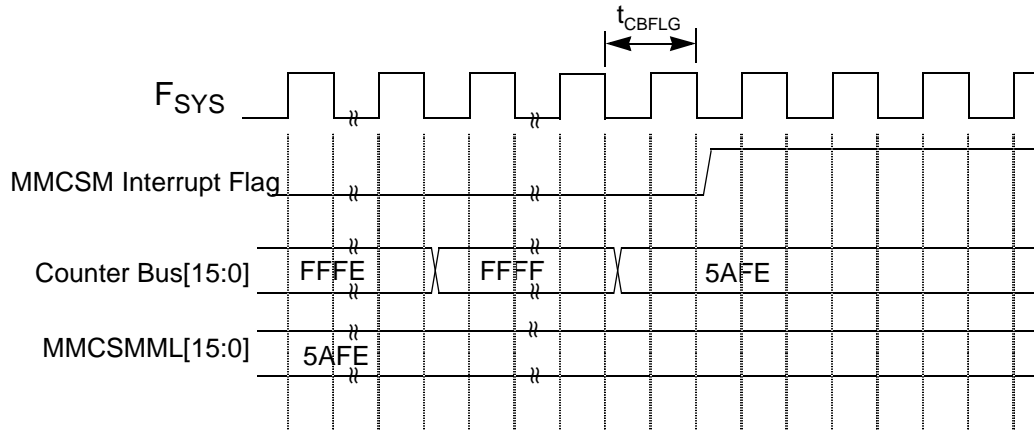


Note:  $F_{SYS}$  is the internal system clock for the IMB3 bus.

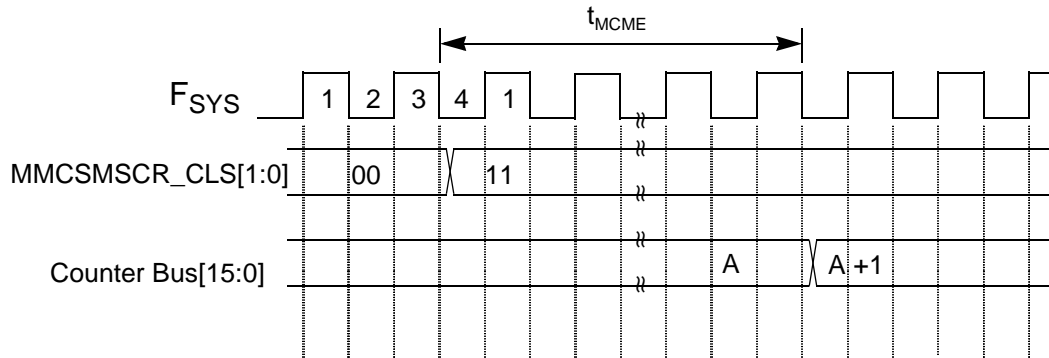
**Figure G-41 MMCSM Clock Pin to Counter Bus Increment Timing Diagram**



**Figure G-42 MMCSM Load Pin to Counter Bus Reload Timing Diagram**



**Figure G-43 MMCSM Counter Bus Reload to Interrupt Flag Setting Timing Diagram**



**Figure G-44 MMCSM Prescaler Clock Select to Counter Bus Increment Timing Diagram**

## G.21.3 MDASM Timing Characteristics



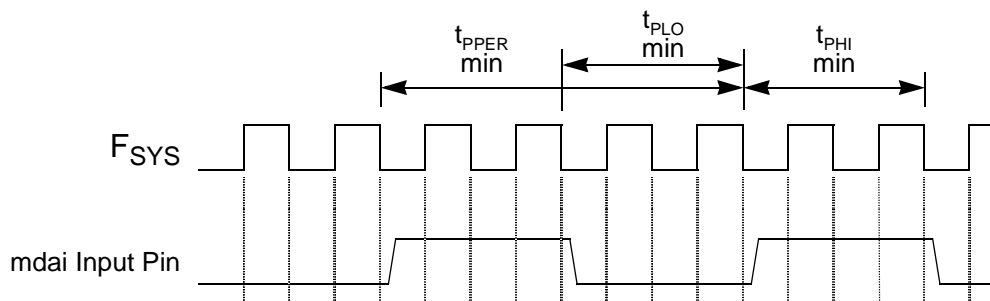
**Table G-22 MDASM Timing Characteristics**

(All delays are in system clock periods.)

Characteristic	Symbol	Min	Max
<b>Input Modes: (IPWM, IPM, IC, DIS)</b>			
MDASM Input Pin Period	$t_{PPER}$	4	—
MDASM Pin Low Time	$t_{PLO}$	2	—
MDASM Pin High Time	$t_{PHI}$	2	—
Input Capture Resolution	$t_{CAPR}$	—	2
Input Pin to Counter Bus Capture Delay	$t_{PCAP}$	1	3 <sup>1</sup>
Input Pin to Interrupt Flag Delay	$t_{PFLG}$	2	3
Input Pin to PIN Delay	$t_{PIN}$	1	2
Counter Bus Resolution	$t_{CBR}$	—	2 <sup>2</sup>
<b>Output modes: (OC, OPWM)</b>			
Output Pulse Width <sup>3</sup>	$t_{PULW}$	2	—
Compare Resolution	$t_{COMR}$	—	2 <sup>2</sup>
Counter Bus to Pin Change	$t_{CBP}$	3	
Counter Bus to Interrupt Flag Set.	$t_{CBFLG}$	3	

**NOTES:**

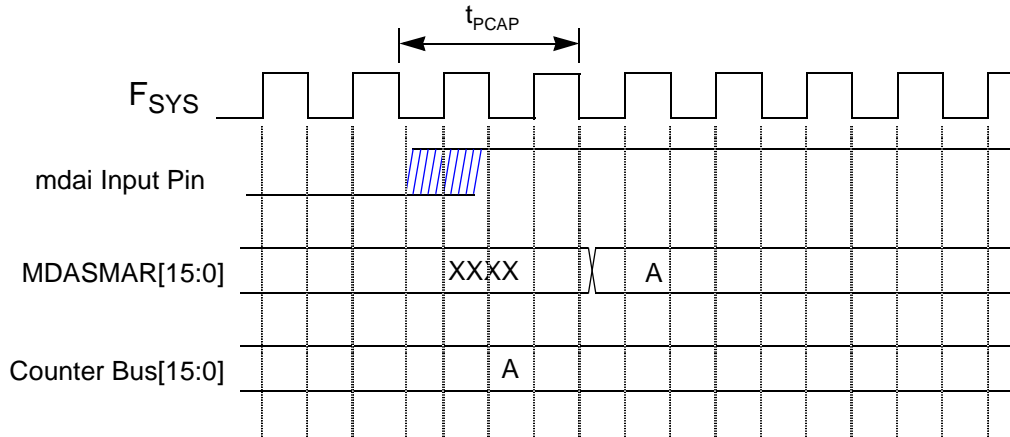
1. If the counter bus capture occurs when the counter bus is changing then the capture is delayed one cycle. In situations where the counter bus is stable when the input capture occurs the  $t_{PCAP}$  has a maximum delay of 2 cycles. (the 1 cycle uncertainty is due to the synchronizer).
2. Maximum resolution is obtained by setting CPSMPSL[3:0] = 0x2 and MDASMSR\_CP[7:0] = 0xFF.
3. Maximum output resolution and pulse width depends on counter (e.g., MMCSM) and MCPSM prescaler settings.



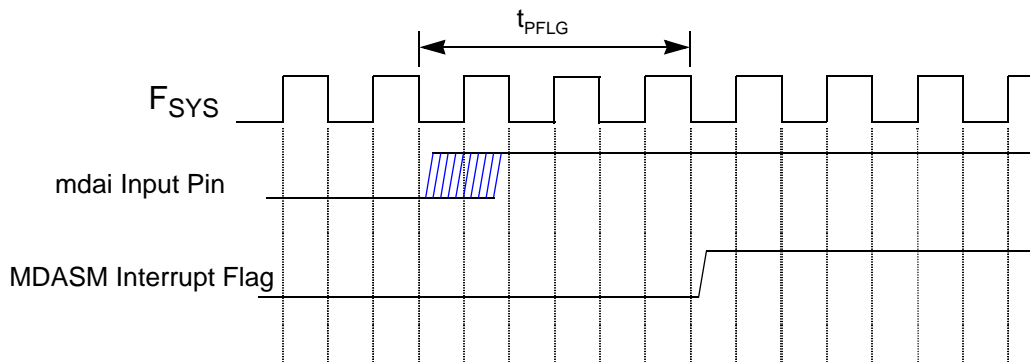
$F_{SYS}$  is the internal system clock for the IMB3 bus.

**Figure G-45 MDASM Minimum Input Pin Timing Diagram**

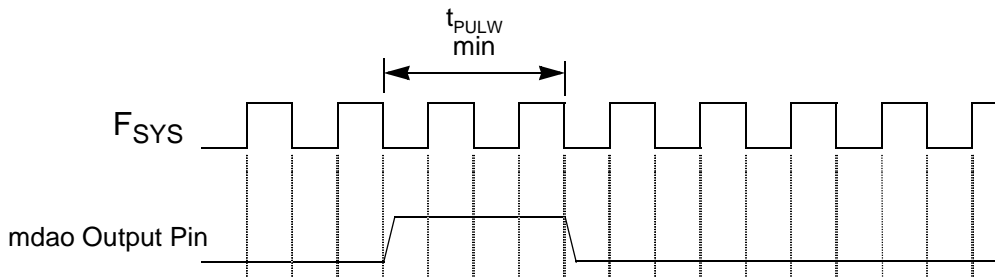




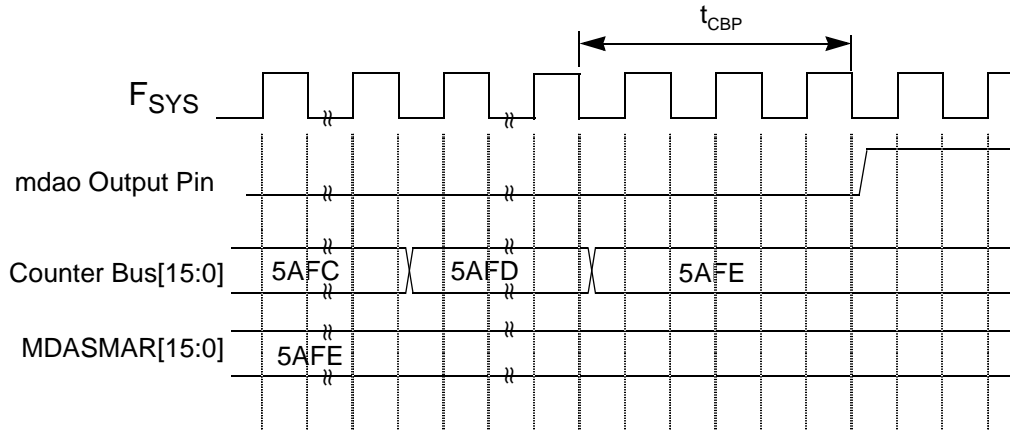
**Figure G-46 MDASM Input Pin to Counter Bus Capture Timing Diagram**



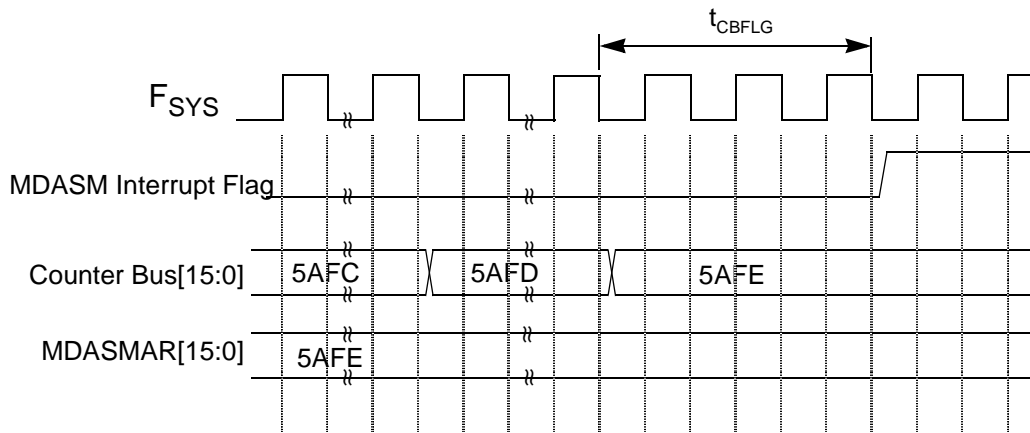
**Figure G-47 MDASM Input Pin to MDASM interrupt Flag Timing Diagram**



**Figure G-48 MDASM Minimum Output Pulse Width Timing Diagram**



**Figure G-49 Counter Bus to MDASM Output Pin Change Timing Diagram**



**Figure G-50 Counter Bus to MDASM Interrupt Flag Setting Timing Diagram**

## G.21.4 MPIO SM Timing Characteristics



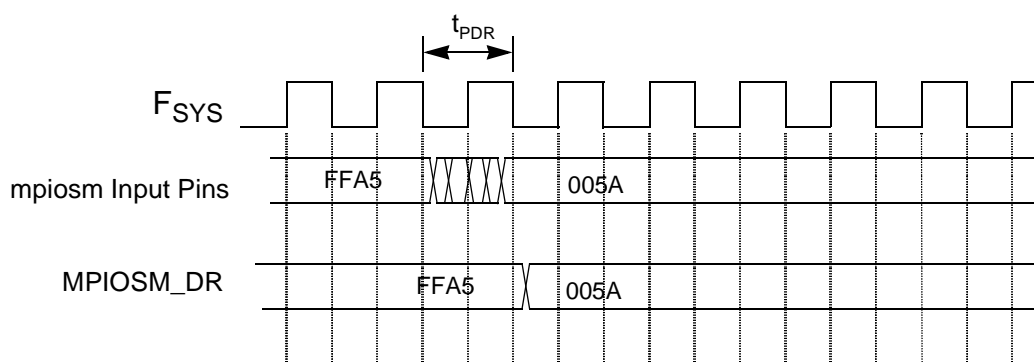
### Table G-23 MPIO SM Timing Characteristics

(All delays are in system clock periods.)

Characteristic	Symbol	Min	Max
<b>Input Mode</b>			
MPIO SM Input Pin Period	$t_{PPER}$	— <sup>1</sup>	—
MPIO SM Pin Low Time	$t_{PLO}$	— <sup>1</sup>	—
MPIO SM Pin High Time	$t_{PHI}$	— <sup>1</sup>	—
Input Pin to MPIO SM_DR Delay	$t_{PDR}$	0	1
<b>Output mode</b>			
Output Pulse Width <sup>2</sup>	$t_{PULW}$	— <sup>2</sup>	—

#### NOTES:

1. The minimum input pin period, pin low and pin high times depend on the rate at which the MPIO SM\_DR register is polled at.
2. The minimum output pulse width depends on how quickly the CPU updates the value inside the MPIO SM\_DR register.



$F_{SYS}$  is the internal system clock for the IMB3 bus.

### Figure G-51 MPIO SM Input Pin to MPIO SM\_DR (Data Register) Timing Diagram

