SECTION 18
DUAL-PORT TPU RAM (DPTRAM)

The dual-port RAM module with TPU microcode storage support (DPTRAM) consists of a control register block and a 6-Kbyte array of static RAM, which can be used either as a microcode storage for TPU or as a general-purpose memory.

The DPTRAM module acts as a common memory on the IMB3 and allows the transfer of data to the two TPU3 modules. Therefore, the DPTRAM interface includes an IMB3 bus interface and two TPU3 interfaces. When the RAM is being used in microcode mode, the array is only accessible to the TPU3 via a separate local bus, and not via the IMB3.

The dual-port TPU3 RAM (DPTRAM) is intended to serve as fast, two-clock access, general-purpose RAM memory for the MCU. When used as general-purpose RAM, this module is accessed via the MCU's internal bus.

The DPTRAM Module is powered by VDDL in normal operation. The entire array may be used as standby RAM if standby power is supplied via the VDDSRAM pin of the MCU. VDDSRAM must be supplied by an external source.

The DPTRAM may also be used as the microcode control store for up to two TPU3 modules when placed in a special emulation mode. In this mode the DPTRAM array may only be accessed by either or both of the TPU3 units simultaneously via separate emulation buses, and not via the IMB3.

The DPTRAM contains a multiple input signature calculator (MISC) in order to provide RAM data corruption checking. The MISC reads each RAM address and generates a 32-bit data-dependent signature. This signature can then be checked by the host.

The DPTRAM supports soft defects detection (SDD).

18.1 Features

- Six Kbytes of static RAM
- Only accessible by the CPU if neither TPU3 is in emulation mode
- Low-power stop operation
  - — Entered by setting the STOP bit in the DPTMCR
  - — Applies only to IMB3 accesses and not to accesses from either TPU3 interface
- TPU microcode mode
  - — The DPTRAM array acts as a microcode storage for the TPU module. This provides a means executing TPU code out of DPTRAM instead of programming it in the TPU ROM.
- Includes built in check logic which scans the array contents and calculates the RAM signature
- IMB3 bus interface

- Two TPU3 interface units
- Bytes, half-word or word accessible

18.2 DPTRAM Configuration and Block Diagram

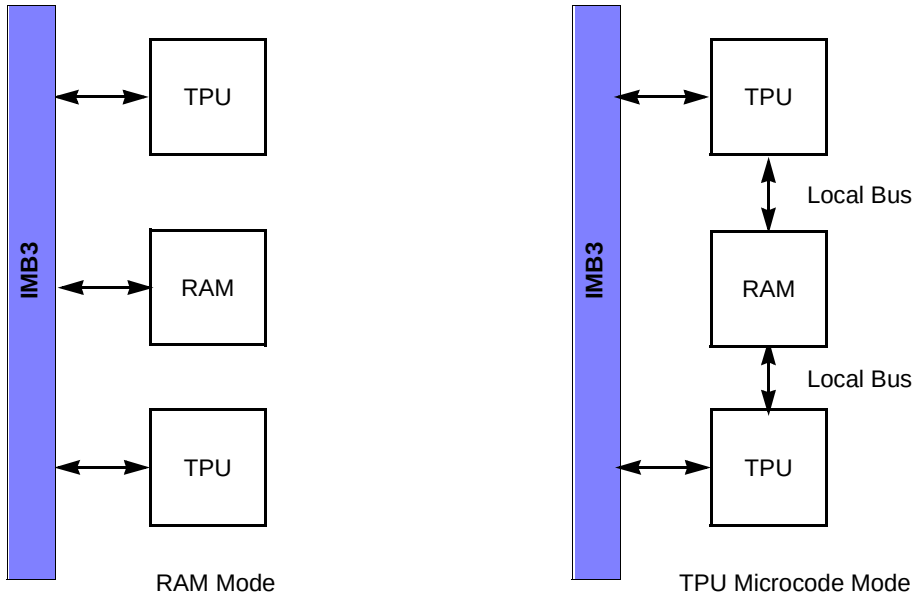

Figure 18-1 DPTRAM Configuration

18.3 Programming Model

The DPTRAM module consists of two separately addressable sections. The first is a set of memory-mapped control and status registers used for configuration (DPTMCR, RAMBAR, MISRH, MISRL, MISCNT) and testing (DPTTCR) of the DPTRAM array. The second section is the array itself.

All DPTRAM module control and status registers are located in supervisor data space. User reads or writes of these will result in a bus error.

When the TPU3 is using the RAM array for microcode control store, none of these control registers have any effect on the operation of the RAM array.

All addresses within the 64-byte control block will respond when accessed properly. Unimplemented addresses will return zeros for read accesses. Likewise, unimplemented bits within registers will return zero when read and will not be affected by write operations.

Table 18-1 shows the DPTRAM control and status registers. The addresses shown are offsets from the base address for the module. Refer to **1.3 MPC555 Address Map** to locate the DPTRAM control block in the MPC555 address map.

Table 18-1 DPTRAM Register Map

R/W Access	Address	Register	Reset Value
Supv R/W	0x30 0000	DPT RAM Module Configuration Register (DPTRMCR) See **Table 18-2** for bit descriptions.	0x0100
Test	0x30 0002	Test Configuration Register (DPTTCR)	0x0000
Supv R/W	0x30 0004	RAM Base Address Register (RAMBAR) See **Table 18-3** for bit descriptions.	0x0001
Supv Read Only	0x30 0006	Multiple Input Signature Register High (MISRH) See **18.3.4 MISR High (MISRH) and MISR Low (MISRL)** for bit descriptions.	0x0000
Supv Read Only	0x30 0008	Multiple Input Signature Register Low (MISRL) See **18.3.4 MISR High (MISRH) and MISR Low (MISRL)** for bit descriptions.	0x0000
Supv Read Only	0x30 000A	Multiple Input Signature Counter (MISCNT) See **18.3.5 MISC Counter (MISCNT)** for bit descriptions.	Last memory address

The DPTRAM array occupies the 6-Kbyte block. In the MPC555, the array must be located at the address 0x30 2000. Refer to **Figure 1-3** and **Figure 18-2**.

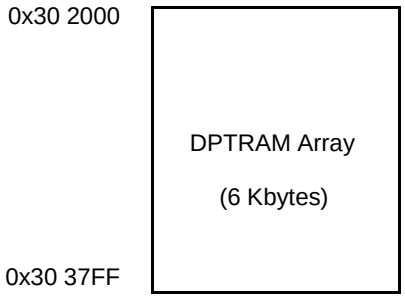

Figure 18-2 DPTRAM Memory Map

18.3.1 DPTRAM Module Configuration Register (DPTMCR)

This register defines the basic configuration of the DPTRAM module. The DPTMCR contains bits to configure the DPT RAM module for stop operation and for proper access rights to the array. The register also contains the MISC control bits.

DPTMCR — DPT Module Configuration Register **0x30 0000**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
STOP	NOT USED				MISF	MISEN	RASP	Reserved							
RESET:															
0					0	0	1	0	0	0	0	0	0	0	0

Table 18-2 DPTMCR Bit Settings

Bit(s)	Name	Description
0	STOP	Low power stop (sleep) mode 0 = DPTRAM clocks running 1 = DPTRAM clocks shut down Only the STOP bit in the DPTMCR may be accessed while the STOP bit is asserted. Accesses to other DPTRAM registers may result in unpredictable behavior. Note also that the STOP bit should be set and cleared independently of the other control bits in this register to guarantee proper operation. Changing the state of other bits while changing the state of the STOP bit may result in unpredictable behavior. Refer to **18.4.4 Stop Operation** for more information.
1:4	—	Reserved
5	MISF	Multiple input signature flag. MISF is readable at any time. This flag bit should be polled by the host to determine if the MISC has completed reading the RAM. If MISF is set, the host should read the MISRH and MISRL registers to obtain the RAM signature. 0 = First signature not ready 1 = MISC has read entire RAM. Signature is latched in MISRH and MISRL and is ready to be read.
6	MISEN	Multiple input signature enable. MISEN is readable and writable at any time. The MISC will only operate when this bit is set and the MPC555 is in TPU3 emulation mode. When enabled, the MISC will continuously cycle through the RAM addresses, reading each and adding the contents to the MISR. In order to save power, the MISC can be disabled by clearing the MISEN bit. 0 = MISC disabled 1 = MISC enabled
7	RASP	Ram area supervisor/user program/data. The RAM array may be placed in supervisor or unrestricted Space. When placed in supervisor space, (RASP = 1), only a supervisor may access the array. If a supervisor program is accessing the array, normal read/write operation will occur. If a user program is attempting to access the array, the access will be ignored and the address may be decoded externally. 0 = Both supervisor and user access to RAM allowed 1 = Supervisor access only to RAM allowed
8:15	—	Reserved

18.3.2 DPTRAM Test Register

RAMTST — Test Register **0x30 0002**

RAMTST is used only during factory testing of the MCU.

18.3.3 Ram Base Address Register (RAMBAR)

The RAMBAR register is used to specify the 16 MSBs of the starting DPT RAM array location in the memory map. In the MPC555, this register must be programed to the value 0xFFA0.

This register can be written only once after a reset. This prevents runaway software from inadvertently re-mapping the array. Since the locking mechanism is triggered by the first write after reset, the base address of the array should be written in a single operation. Writing only one half of the register will prevent the other half from being written.

Soft reset has no effect on this register.

RAMBAR — RAM Array Base Address Register **0x30 0004**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	Reserved				RAMDS
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 18-3 RAMBAR Bit Settings

Bit(s)	Name	Description
0:10	A[8:18]	RAM array base address. These bits specify the 11 high-order bits (address lines ADDR[8:18] in little-endian notation) of the 24-bit base address of the RAM array. This allows the array to be placed on a 8-Kbyte boundary anywhere in the memory map. It is the users responsibility not to overlap the RAM array memory map with other modules on the chip. On the MPC555 the value 0xFFA0 must be used.
11:14	—	Reserved. (Bits 11:12 represent A[12:11] in DPTRAM implementation that require them.)
15	RAMDS	RAM disabled. RAMDS is a read-only status bit. The RAM array is disabled after a master reset since the RAMBAR register may be incorrect. When the array is disabled, it will not respond to any addresses on the IMB3. Access to the RAM control register block is not affected when the array is disabled. RAMDS is cleared by the DPTRAM module when a base address is written to the array address field of RAMBAR. RAMDS = 0: RAM enabled RAMDS = 1: RAM disabled

18.3.4 MISR High (MISRH) and MISR Low (MISRL)

The MISRH and MISRL together contain the 32-bit RAM signature calculated by the MISC. These registers are read-only and should be read by the host when the MISF bit in the MCR is set. Note that the naming of the D[31:0] bits represents little-endian bit encoding.

Exiting TPU3 emulation mode results in the reset of both MISRH and MISRL

MISRH — Multiple Input Signature Register High **0x30 0006**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MISRL — Multiple Input Signature Register Low **0x30 0008**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

18.3.5 MISC Counter (MISCNT)

The MISCNT contains the address of the current MISC memory access. This registers is read-only. Note that the naming of the A[31:0] bits represents little-endian bit encoding.

Exiting TPU3 emulation mode or clearing the MISEN bit in the DPTMCR results in the reset of this register.

MISCNT — MISC Counter **0x30 000A**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	RESERVED		
RESET:															
Last Memory Address															

18.4 Operation

The DPTRAM module has several modes of operation. The following sections describe DPTRAM operation in each of these modes.

18.4.1 Normal Operation

In normal operation, the DPTRAM is powered by VDDL and may be accessed via the IMB3 by a bus master.

Read or write accesses of 8, 16, or 32 bits are supported. In normal operation, neither TPU3 accesses the array, nor do they have any effect on the operation of the DPTRAM module.

18.4.2 Standby Operation

The DPTRAM array uses a separate power supply VDDSRAM to maintain the contents of the DPTRAM array during a power-down phase.

When the RAM array is powered by the VDDSRAM pin of the MCU, access to the RAM array is blocked. Data read from the RAM array during this condition cannot be guaranteed. Data written to the DPTRAM may be corrupted if switching occurs during a write operation.

In order to guarantee valid DPTRAM data during power-down, external low voltage inhibit circuitry (external to the MCU) must be designed to force the RESET pin of the MCU into the active state before VDDL drops below its normal limit. This is necessary to inhibit spurious writes to the DPTRAM during power-down.

18.4.3 Reset Operation

When a synchronous reset occurs, a bus master is allowed to complete the current access. Thus a write bus cycle (byte or half word) that is in progress when a synchronous reset occurs will be completed without error. Once a write already in progress has been completed, further writes to the RAM array are inhibited.

NOTE

A word (32-bit) write will be completed coherently only if the reset occurs during the second (16-bit) write bus cycle. If reset occurs during the first write bus cycle, only the first half word will be written to the RAM array and the second write will not be allowed to occur. In this case, the word data contained in the DPTRAM will not be coherent. The first half word will contain the most significant half of the new word information and the second half word will contain the least significant half of the old word information.

If a reset is generated by an asynchronous reset such as the loss of clocks or software watchdog time-out, the contents of the RAM array are not guaranteed. (Refer to **SECTION 7 RESET** for a description of MPC555 reset sources, operation, control, and status.)

Reset will also reconfigure some of the fields and bits in the DPTRAM control registers to their default reset state. See the description of the control registers to determine the effect of reset on these registers.

18.4.4 Stop Operation

Setting the STOP control bit in the DPTMCR causes the module to enter its lowest power-consuming state. The DPTMCR can still be written to allow the STOP control bit to be cleared.

In stop mode, the DPTRAM array cannot be read or written. All data in the array is retained. The BIU continues to operate to allow the CPU to access the STOP bit in the DPTMCR. The system clock remains stopped until the STOP bit is cleared or the DPTRAM module is reset.

The STOP bit is initialized to logical zero during reset. Only the STOP bit in the DPTMCR can be accessed while the STOP bit is asserted. Accesses to other DPTRAM registers may result in unpredictable behavior. Note also that the STOP bit should be set and cleared independently of the other control bits in this register to guarantee proper operation. Changing the state of other bits while changing the state of the STOP bit may result in unpredictable behavior.

Switching to VDDSRAM occurs if VDDL drops below its specified value when the RAM module is in stop mode.

The DPTRAM will not enter stop mode if either or both of the TP1EMM or TP2EMM signals are asserted, indicating TPU3 emulation mode.

18.4.5 Freeze Operation

The FREEZE line on the IMB3 has no effect on the DPTRAM module. When the freeze line is set, the DPTRAM module will operate in its current mode of operation. If the DPTRAM module is not disabled, (RAMDS = 0), it may be accessed via the IMB3. If the DPTRAM array is being used by the TPU in emulation mode, the DPTRAM will still be able to be accessed by the TPU microengine.

18.4.6 TPU3 Emulation Mode Operation

To emulate TPU3 time functions, the user stores the microinstructions required for all time functions to be used, in the RAM array. This must be done with the DPTRAM in its normal operating mode and accessible from the IMB3. After the time functions are stored in the array, the user places one or both of the TPU3 units in emulation mode. The RAM array is then controlled by the TPU3 units and disconnected from the IMB3.

To use the DPTRAM for microcode accesses, set the EMU bit in the corresponding TPU3 module configuration register. Through the auxiliary buses, the TPU3 units can access word instructions simultaneously at a rate of up to 40 MHz.

When the RAM array is being used by either or both of the TPU3 units, all accesses via the IMB3 are disabled. The control registers have no effect on the RAM array. Accesses to the array are ignored, allowing an external RAM to replace the function of the general-purpose RAM array.

The contents of the RAM are validated using a multiple input signature calculator (MISC). MISC reads of the RAM are performed only when the MPC555 is in emulation mode and the MISC is enabled (MISEN = 1 in the DPTMCR).

Refer to **17.3.6 Emulation Support** for more information in TPU3 and DPTRAM operation in emulation mode.

18.5 Multiple Input Signature Calculator (MISC)

The integrity of the RAM data is ensured through the use of a MISC. The RAM data is read in reverse address order and a unique 32-bit signature is generated based on the output of these reads. MISC reads are performed when one of the TPU3 modules does not request back-to-back accesses to the RAM provided that the MISEN bit in the MPC555 MCR is set.

The MISC generates the DPTRAM signature based on the following polynomial:

$$G(x) = 1 + x + x^2 + x^{22} + x^{31}$$

After the entire RAM has been read and a signature has been calculated, the MISC sets the MISF bit in the MPC555 MCR. The host should poll this bit and enter a handling routine when the bit is found to be set.

The signature should be then read from the MISRH and MISRL registers and the host determines if it matches the predetermined signature.

The MISRH and MISRL registers are updated each time the MISC completes reading the entire RAM regardless of whether or not the previous signature has been read or not. This ensures that the host reads the most recently generated signature.

The MISC can be disabled by clearing the MISEN bit in the MPC555 MCR. Note that the reset state of the MPC555 MISEN is disabled.