SECTION 1
OVERVIEW

The MPC555 is a member of Motorola's MPC500 PowerPC™ RISC Microcontroller family. The MPC555 offers the following features:

- PowerPC core with floating-point unit
- 26 Kbytes fast RAM and 6 Kbytes TPU microcode RAM
- 448 Kbytes flash EEPROM with 5-V programming
- 5-V I/O system
- Serial system: queued serial multi-channel module (QSMCM), dual CAN 2.0B controller modules (TouCAN™)
- 50-channel timer system: dual time processor units (TPU3), modular I/O system (MIOS1)
- 32 analog inputs: dual queued analog-to-digital converters (QADC64)
- Submicron HCMOS (CDR1) technology
- 272-pin plastic ball grid array (PBGA) packaging
- 40-MHz operation, -40° C to 125° C with dual supply (3.3 V, 5 V).

NOTE

Throughout this manual references to 3 V refer to the nominal supply voltage of 3.3 V.)

1.1 Block Diagram

Figure 1-1 is a block diagram of the MPC555.

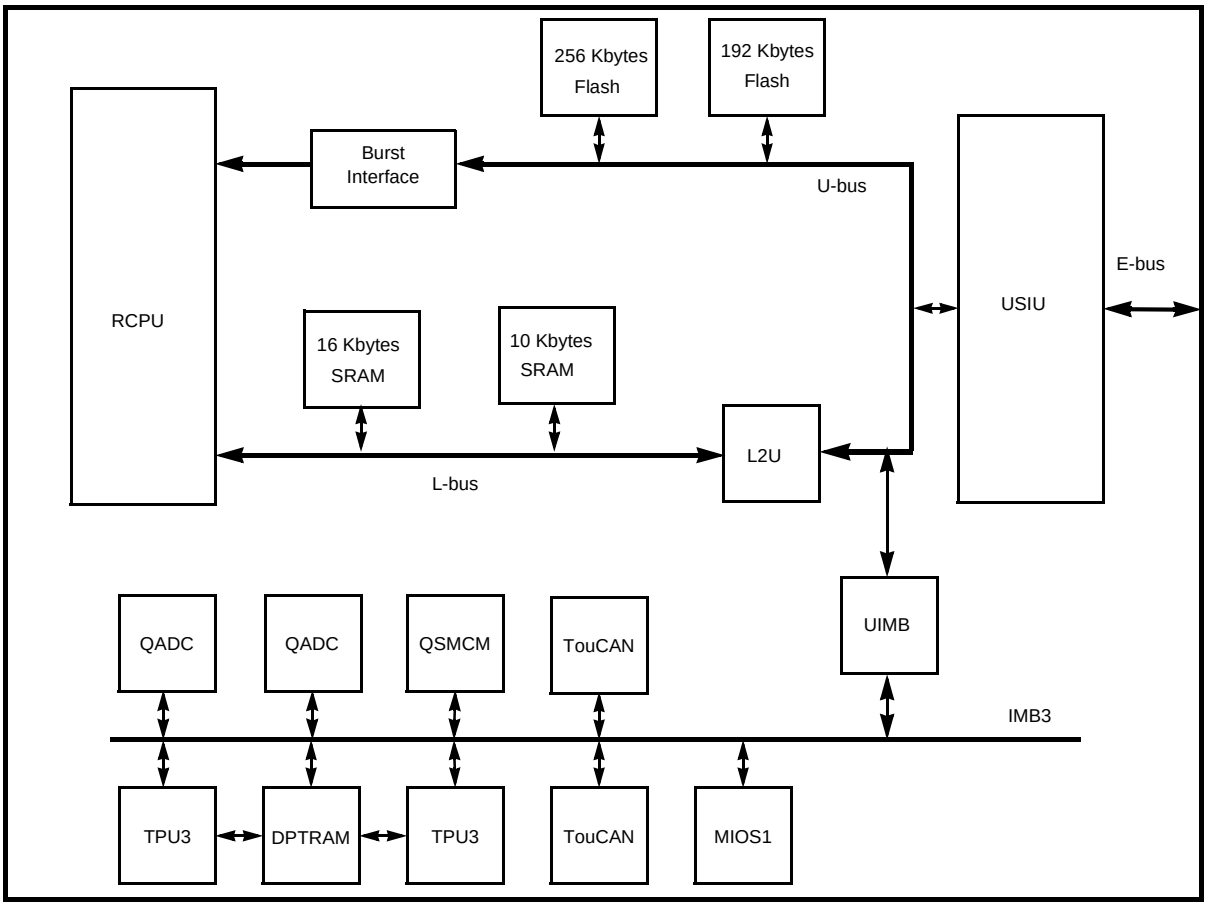

Figure 1-1 MPC555 Block Diagram

1.2 MPC555 Features

Features of each module on the MPC555 are listed below.

1.2.1 RISC MCU Central Processing Unit (RCPU)

- 32-bit PowerPC architecture (compliant with PowerPC Architecture Book 1)
- Core performance measured at 52.7 K MIPS (Dhrystone 2.1) @ 40 MHz.

NOTE

This assumes the RCPU core is running in “normal” mode and show cycles is turned off (ISCT_SER of the ICTRL register is set to 111). See **Table 21-21**.

- Fully static, low power operation
- Integrated floating-point unit
- Precise exception model
- Extensive system development support
  - — On-chip watchpoints and breakpoints
  - — Program flow tracking
  - — On-chip emulation (OnCE™) development interface

1.2.2 Four-Bank Memory Controller

- Works with SRAM, EPROM, flash EEPROM, and other peripherals
- Byte write enables
- 32-bit address decodes with bit masks
- Memory transfer start (MTS): This pin is the transfer start signal to access a slave's external memory by an external bus master

1.2.3 U-Bus System Interface Unit (USIU)

- Clock synthesizer
- Power management
- Reset controller
- PowerPC decrementer and time base
- Glueless interface to SRAMs and burstable FLASHs
- Real-time clock register
- Periodic interrupt timer
- Hardware bus monitor and software watchdog timer
- Interrupt controller that supports up to eight external and eight internal interrupts
- IEEE 1149.1 JTAG test access port
- External bus interface
  - — 24 address pins, 32 data pins
  - — Supports multiple master designs
  - — Four-beat transfer bursts, two-clock minimum bus transactions
  - — Tolerates 5-V inputs, provides 3.3-V outputs

1.2.4 Flexible Memory Protection Unit

- Four instruction regions and four data regions
- 4-Kbyte to 16-Mbyte region size support
- Default attributes available in one global entry
- Attribute support for speculative accesses

1.2.5 448 Kbytes of CDR MoneT Flash EEPROM Memory (CMF)

- One 256-Kbyte and one 192-Kbyte module
- Page read mode
- Block (32-Kbyte) erasable
- External 4.75-V to 5.25-V program and erase power supply

1.2.6 26 Kbytes of Static RAM

- One 16-Kbyte and one 10-Kbyte module
- Fast (one-clock) access
- Keep-alive power
- Soft defect detection (SDD)

1.2.7 General-Purpose I/O Support

- Address (24) and data (32) pins can be used for general-purpose I/O in single-chip mode

- 9 general-purpose I/O pins in MIOS1 unit
- Many peripheral pins can be used for general-purpose I/O when not used for primary function
- 5-V outputs

1.2.8 Two Time Processor Units (TPU3)

- Each TPU3 module provides these features:
  - — A dedicated micro-engine operates independently of the RCPU
  - — 16 independent programmable channels and pins
  - — Each channel has an event register consisting of a 16-bit capture register, a 16-bit compare register and a 16-bit comparator
  - — Nine pre-programmed timer functions are available
  - — Any channel can perform any time function
  - — Each timer function can be assigned to more than one channel
  - — Two timer count registers with programmable prescalers
  - — Each channel can be synchronized to one or both counters
  - — Selectable channel priority levels
  - — 5-V outputs
- 6-Kbyte dual port TPU RAM (DPTRAM) is shared by the two TPU3 modules for TPU microcode

1.2.9 18-Channel Modular I/O System (MIOS1)

- Ten double action submodules (DASMs)
- Eight dedicated PWM sub-modules (PWMSMs)
- Two 16-bit modulus counter submodules (MCSMs)
- Two parallel port I/O submodules (PIOSM)
- 5-V outputs

1.2.10 Two Queued Analog-to-Digital Converter Modules (QADC)

Each QADC provides:

- Up to 16 analog input channels, using internal multiplexing
- Up to 41 total input channels, using internal and external multiplexing
- 10-bit A/D converter with internal sample/hold
- Typical conversion time of 10 µsec (100,000 samples per second)
- Two conversion command queues of variable length
- Automated queue modes initiated by:
  - — External edge trigger/level gate
  - — Software command
- 64 result registers
- Output data that is right- or left-justified, signed or unsigned

1.2.11 Two CAN 2.0B Controller Modules (TouCANs)

Each TouCAN provides these features:

- Full implementation of CAN protocol specification, version 2.0 A and B

- Each module has 16 receive/transmit message buffers of 0 to 8 bytes data length
- Global mask register for message buffers 0 to 13
- Independent mask registers for message buffers 14 and 15
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- 16-bit free-running timer for message time-stamping
- Low power sleep mode with programmable wake-up on bus activity
- Programmable I/O modes
- Maskable interrupts
- Independent of the transmission medium (external transceiver is assumed)
- Open network architecture
- Multimaster concept
- High immunity to EMI
- Short latency time for high-priority messages
- Low power sleep mode with programmable wakeup on bus activity

1.2.12 Queued Serial Multi-Channel Module (QSMCM)

- Queued serial peripheral interface (QSPI)
  - — Provides full-duplex communication port for peripheral expansion or interprocessor communication
  - — Up to 32 preprogrammed transfers, reducing overhead
  - — Has 160-byte queue
  - — Programmable transfer length: from eight to 16 bits, inclusive
  - — Synchronous interface with baud rate of up to system clock / 4
  - — Four programmable peripheral-select pins support up to 16 devices
    - Wrap-around mode allows continuous sampling of a serial peripheral for efficient interfacing to serial A/D converters
- Two serial communications interfaces (SCI). Each SCI offers these features:
  - — UART mode provides NRZ format and half- or full-duplex interface
  - — 16 register receive buffer and 16 register transmit buffer (SCI1)
  - — Advanced error detection and optional parity generation and detection
  - — Word length programmable as eight or nine bits
  - — Separate transmitter and receiver enable bits and double buffering of data
  - — Wakeup functions allow the CPU to run uninterrupted until either a true idle line is detected or a new address byte is received
  - — External source clock for baud generation
  - — Multiplexing of transmit data pins with discrete outputs and receive data pins with discrete inputs

1.3 MPC555 Address Map

The internal memory map is organized as a single 4-Mbyte block. The user can assign this block to one of eight locations by programming a register in the USIU. The eight possible locations are the first eight 4-Mbyte memory blocks starting with address 0x0000 0000. (Refer to **Figure 1-2**). The programmability of the internal memory map location allows the user to implement a multiple-chip system.

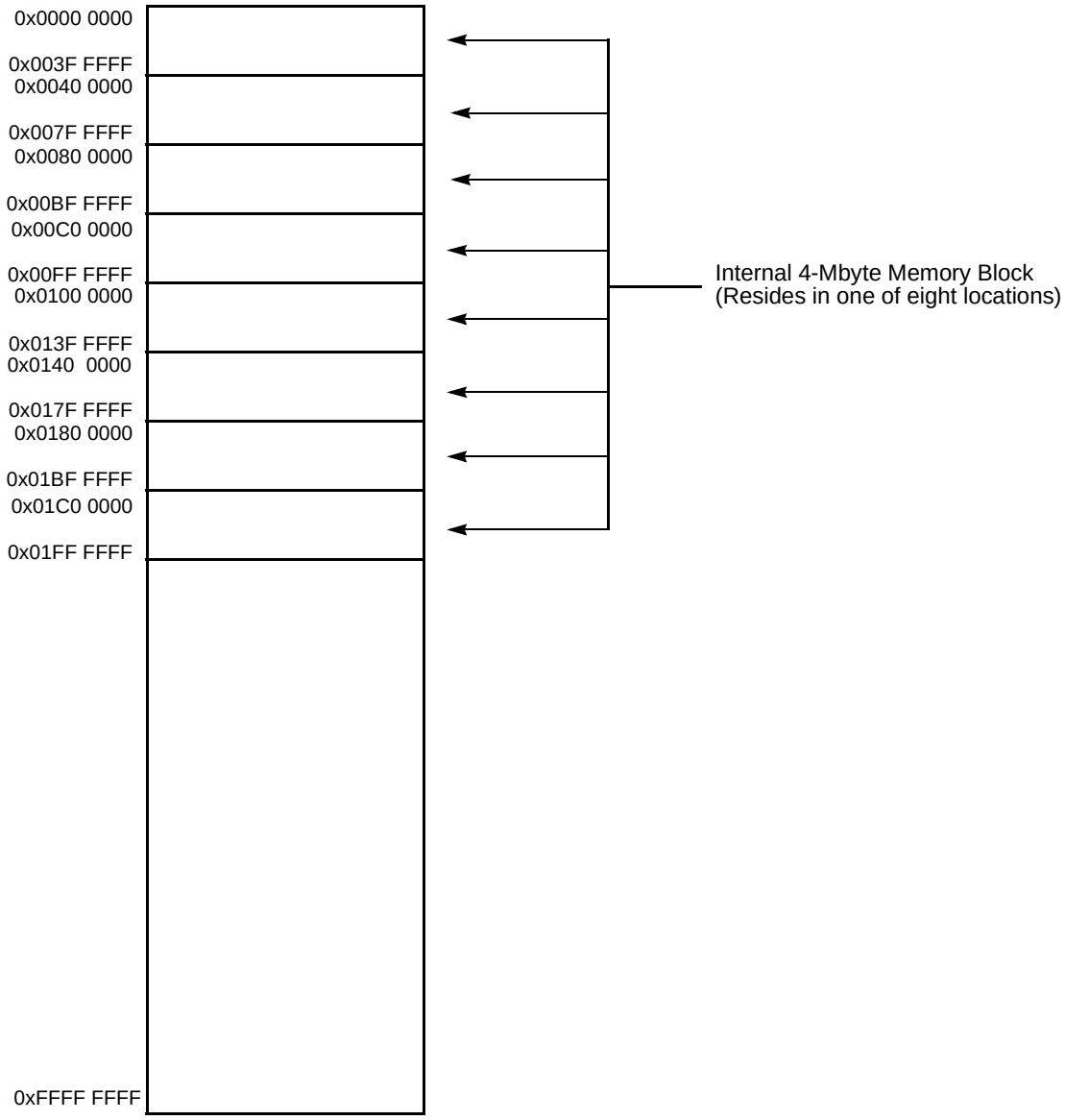

Figure 1-2 MPC555 Memory Map

The internal memory space is divided into the following sections:

- Flash memory (448 Kbytes)
- Static RAM memory (26 Kbytes)
- Control registers and IMB2 modules (64 Kbytes):
  - — USIU and flash control registers
  - — UIMB interface and IMB2 modules
  - — SRAM control registers

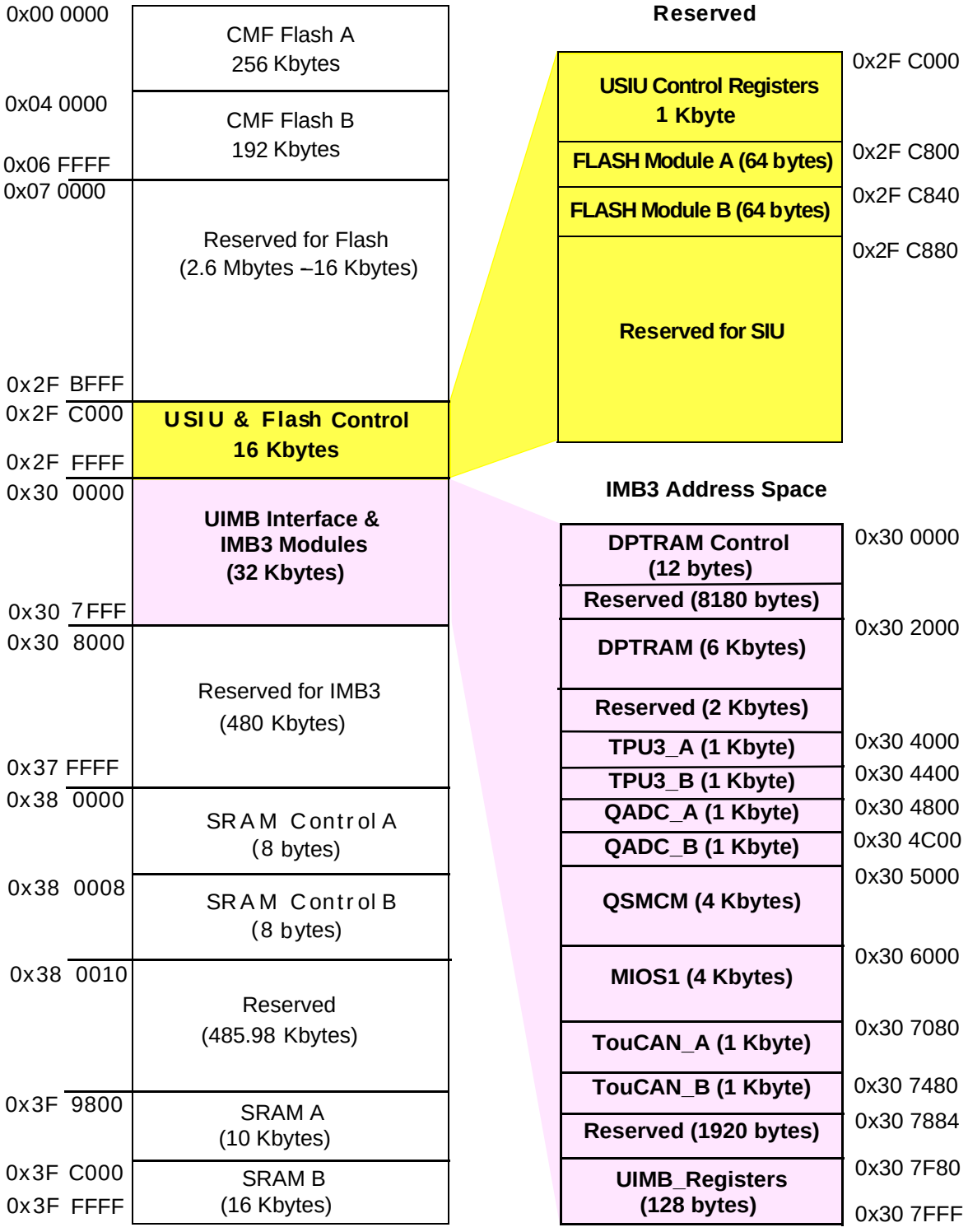

Figure 1-3 MPC555 Internal Memory Map