SECTION 20
STATIC RANDOM ACCESS MEMORY (SRAM)

The MPC555 contains two static random access memory (SRAM) modules: a 16-Kbyte module and a 10-Kbyte module. The SRAM modules provide the microcontroller unit (MCU) with fast (one cycle access), general-purpose memory. The SRAM can be read or written as either bytes, half words, or words.

Each SRAM module is built with a series of 4-Kbyte blocks and occupies a continuous block of memory. For a RAM size array block of less than 4 Kbytes (e.g., the 2-Kbyte array in the 10-Kbyte SRAM module), the remaining 2 Kbytes are unimplemented and unusable.

The SRAM modules are accessible to the CPU and other bus masters via the L-bus on the CPU chip. To improve access time, each SRAM module resides on a separate bus interface unit (BIU). Each BIU has its own module control register.

20.1 Features

- One-cycle access
- Byte, half-word, or word read/write accesses
- Individual protection control bits provided for 4-Kbyte block boundaries
  - — read only region
  - — data only region
  - — user/supervisor
- Two-cycle access for power savings
- Low power standby operation for data retention
  - — VDDI = 0, no read/writes to the SRAM; VDDSRAM = 3.3 V to retain data
- Supports pipelining

20.2 Block Diagram

Figure 20-1 shows the major components of an SRAM module.

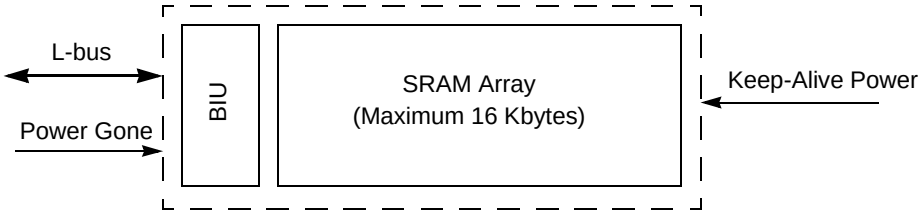

Figure 20-1 SRAM Block Diagram

20.3 Programming Model

The SRAM modules consist of two separately addressable sections the array itself, and a set of registers used for configuration and testing of the SRAM array. The registers are located in the SRAM control register block, shown in **Figure 20-2**. See also **Figure 1-3** for the entire MPC555 memory map.

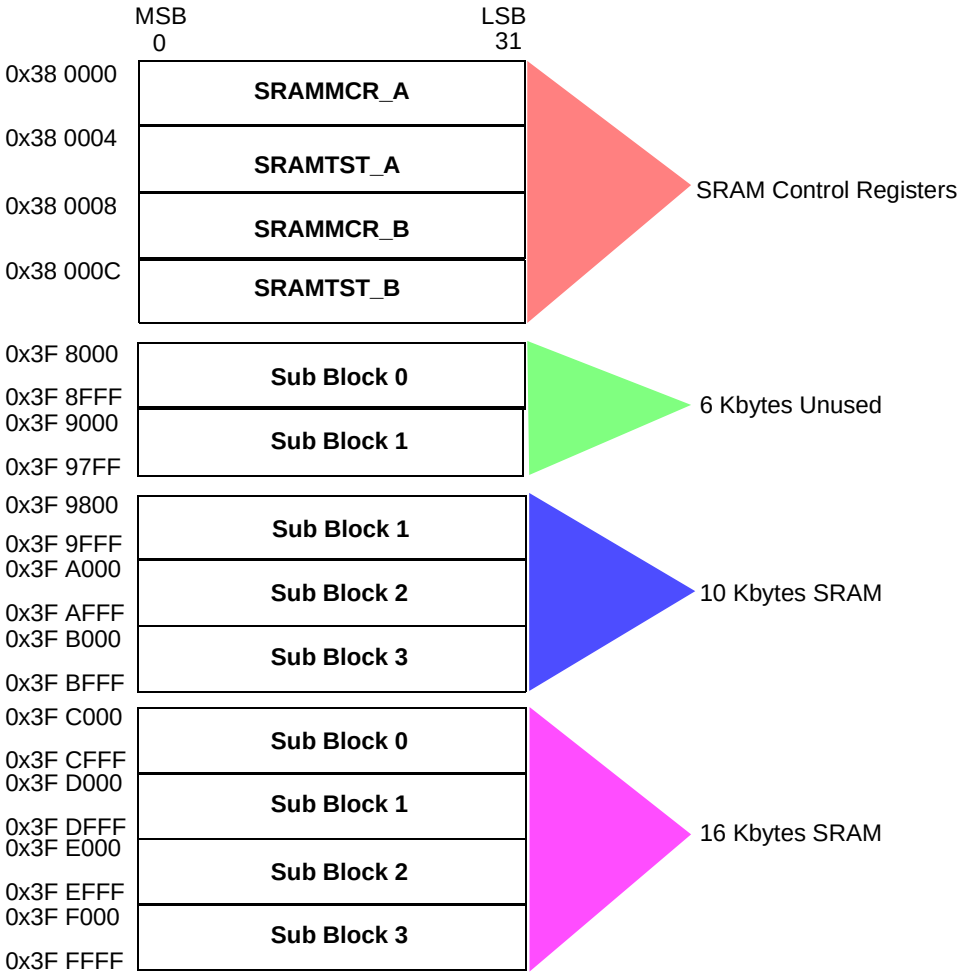

Figure 20-2 SRAM Memory Map

The control block for each of the two SRAM modules contains one control register for configuring the array and one control register for use in testing.

20.3.1 SRAM Module Configuration Register (SRAMMCR)

Each SRAM module configuration register contains bits for setting access rights to the array. **Table 20-1** provides definitions for the bits.

SRAMMCR — SRAM Module Configuration Register **0x38 0000**
0x38 0008

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
LCK	DIS	2CY	RESERVED												
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
RESERVED				R0	D0	S0	R1	D1	S1	R2	D2	S2	R3	D3	S3
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 20-1 SRAMMCR Bit Settings

Bit(s)	Name	Description
0	LCK	Lock bit. This bit can be set only once and cleared only by reset. 0 = Writes to the SRAMMCR are accepted 1 = Writes to the SRAMMCR are ignored
1	DIS	Module disable 0 = SRAM module is enabled 1 = SRAM module is disabled. Module can be subsequently re-enabled by software setting this bit or by reset. Attempts to read SRAM array when it is disabled result in internal $\overline{\text{TEA}}$ assertion.
2	2CY	Two-cycle mode 0 = SRAM module is in single-cycle mode (normal operation) 1 = SRAM module is in two-cycle mode. In this mode, the first cycle is used for decoding the address, and the second cycle is used for accepting or providing data. This mode provides some power savings while keeping the memory active.
3:19	—	Reserved
20, 23, 26, 29	Rx (x = 0, 1, 2, 3)	Read only. R0 controls the highest 4-Kbyte block (lowest address) of the SRAM array; R3 controls the lowest block (highest address). 0 = 4-Kbyte block is readable and writable 1 = 4-Kbyte block is read only. Attempts to write to this space result in internal $\overline{\text{TEA}}$ assertion.
21, 24, 27, 30	Dx (x = 0, 1, 2, 3)	Data only. D0 controls the highest 4-Kbyte block (lowest address) of the SRAM array; D3 controls the lowest block (highest address). 0 = 4-Kbyte block can contain data or instructions 1 = 4-Kbyte block contains data only. Attempts to load instructions from this space result in internal $\overline{\text{TEA}}$ assertion.
22, 25, 28, 31	Sx (x = 0, 1, 2, 3)	Supervisor only. S0 controls the highest 4-Kbyte block (lowest address) of the SRAM array; S3 controls the lowest block (highest address). 0 = 4-Kbyte block is placed in unrestricted space 1 = 4-Kbyte block is placed in supervisor space. Attempts to access this space from the user privilege level result in internal $\overline{\text{TEA}}$ assertion.

20.3.2 SRAM Test Register (SRAMTST)

SRAMTST — SRAM Test Register **0x38 0004, 0x38 000C**

The SRAM test register is used for factory testing only.