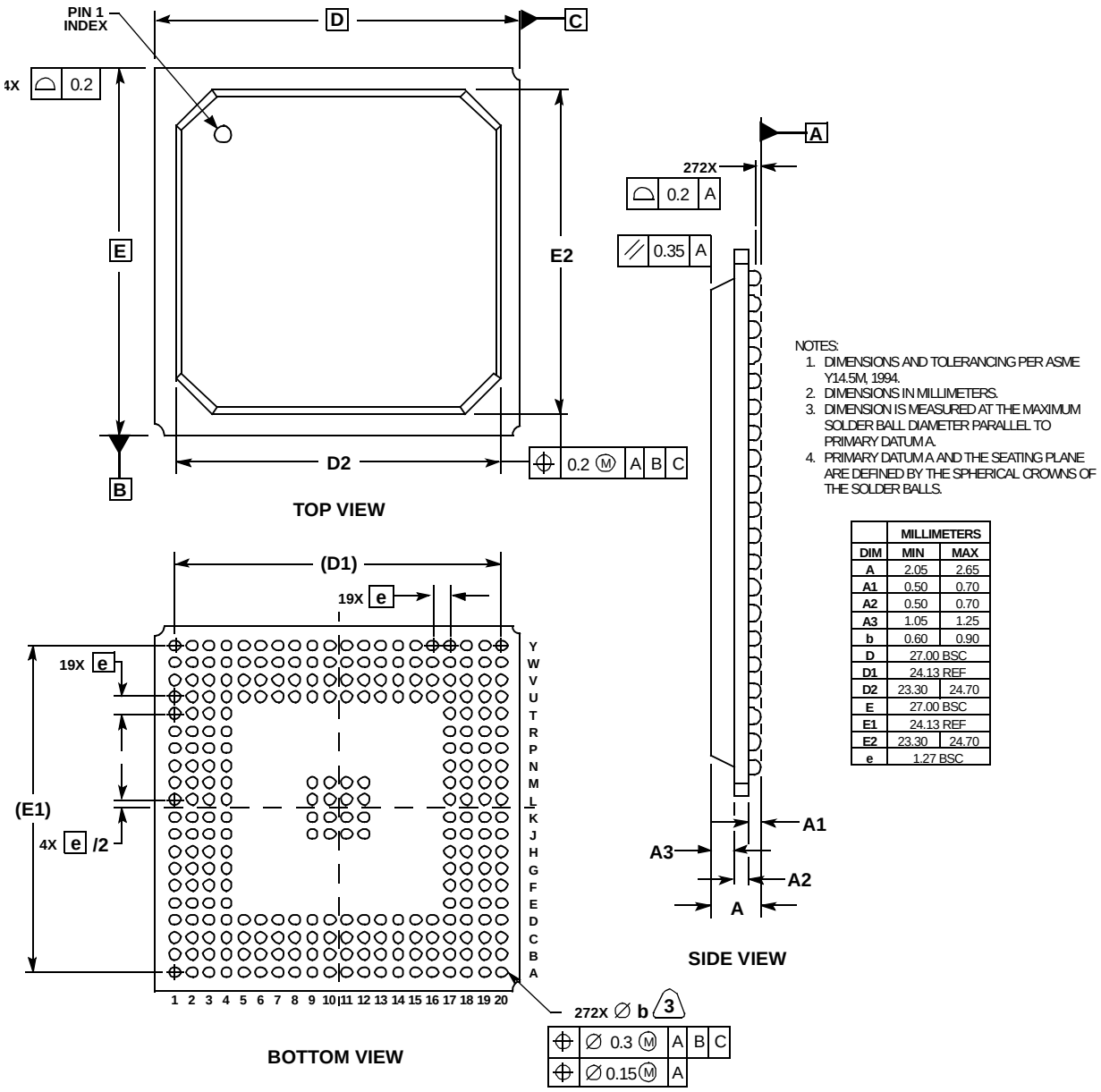
SECTION 2
SIGNAL DESCRIPTIONS

2.1 Packaging and Pinout Descriptions

Figure 2-1 gives the case configuration and packaging information for the MPC555. **Figure 2-2** gives the MPC555 pinout data. **Table 2-1** gives an overview of the pins on the MPC555.



	MILLIMETERS	
DIM	MIN	MAX
A	2.05	2.65
A1	0.50	0.70
A2	0.50	0.70
A3	1.05	1.25
b	0.60	0.90
D	27.00 BSC	
D1	24.13 REF	
D2	23.30	24.70
E	27.00 BSC	
E1	24.13 REF	
E2	23.30	24.70
e	1.27 BSC	

CASE 1135A–01
ISSUE A

Figure 2-1 MPC555 Case Dimensions and Packaging

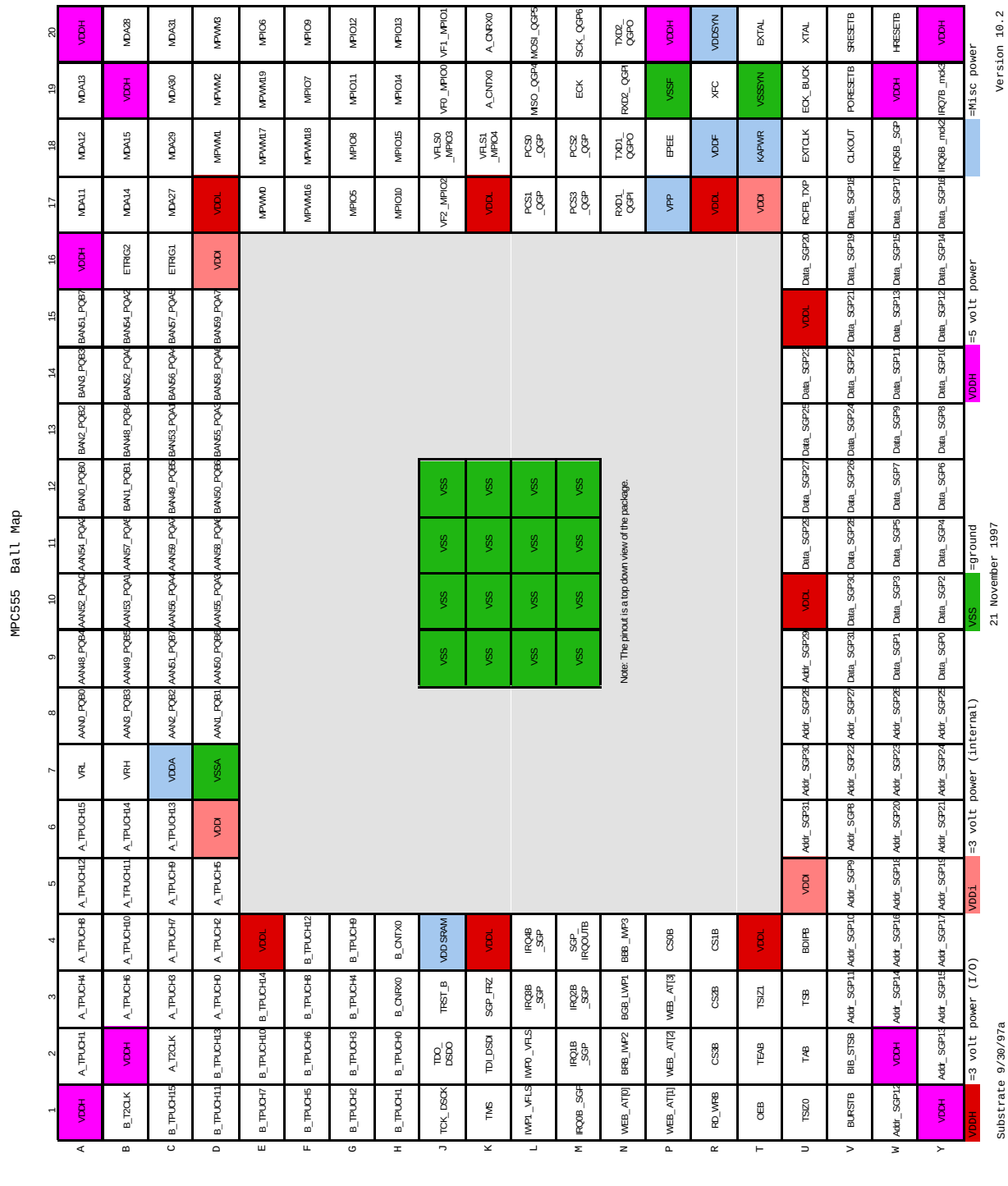


Figure 2-2 MPC555 Pinout Data

Table 2-1 MPC555 Pin Functions for 272-Pin PBGA

Functional Group	Signals[1]	Pins	3 V / 5 V[2]
24 Address lines (16-Mbyte address space)	ADDR[8:31]/SGPIOA[8:31]	24	3-V / 5-V GPIO
32-bit data bus	DATA[0:31]/SGPIOD[0:31]	32	
External interrupts	$\overline{\text{IRQ}}$[0]/SGPIOC[0]	8	3-V / 5-V GPIO
	$\overline{\text{IRQ}}$[1]/$\overline{\text{RSV}}$/SGPIOC[1]		
	$\overline{\text{IRQ}}$[2]/$\overline{\text{CR}}$/SGPIOC[2]/MTS		
	$\overline{\text{IRQ}}$[3]/$\overline{\text{KR}}$/$\overline{\text{RETRY}}$/SGPIOC[3]		
	$\overline{\text{IRQ}}$[4]/AT[2]/SGPIOC[4]		
	$\overline{\text{IRQ}}$[5]/SGPIOC[5]/MODCK[1][3]		
	$\overline{\text{IRQ}}$[6:7]/MODCK[2:3][3]		
Bus control	TSIZ[0:1]	11	3 V
	RD/$\overline{\text{WR}}$		
	$\overline{\text{BURST}}$		
	$\overline{\text{BDIP}}$		
	$\overline{\text{TS}}$		
	$\overline{\text{TA}}$		
	$\overline{\text{TEA}}$		
	$\overline{\text{RSTCONF}}$/TEXP[3]		
	$\overline{\text{OE}}$		
	$\overline{\text{BI}}$/$\overline{\text{STS}}$		
General purpose chip select machine (multiplexed with development and debug support)	$\overline{\text{CS}}$[0:3]	8	3 V
	$\overline{\text{WE}}$[0:3]/$\overline{\text{BE}}$[0:3]/AT[0:3]		
Power-on reset and reset configuration	$\overline{\text{PORESET}}$[3]	3	3 V
	$\overline{\text{HRESET}}$[3]		
	$\overline{\text{SRESET}}$[3]		
Development and debug support	SGPIOC[6]/FRZ/$\overline{\text{PTR}}$	5	3-V / 5-V GPIO
	SGPIOC[7]/$\overline{\text{IRQOUT}}$/LWP[0]		
	$\overline{\text{BG}}$/VF[0]/LWP[1]		
	$\overline{\text{BR}}$/VF[1]/IWP[2]		
	$\overline{\text{BB}}$/VF[2]/IWP[3]		
JTAG and debug port	TMS	7	3 V
	TDI/DSDI		
	TCK/DSCK		
	TDO/DSDO		
	$\overline{\text{TRST}}$		
	IWP[0:1]/VFLS[0:1]		
Clocks and PLL	XTAL[3]	5	3 V
	EXTAL[3]		
	CLKOUT		
	EXTCLK[3]		
	XFC		
	ENGCLK/BUCLK	1	5 V

Table 2-1 MPC555 Pin Functions for 272-Pin PBGA (Continued)

Functional Group	Signals[1]	Pins	3 V / 5 V[2]
QSMCM	PCS0/ $\overline{SS}$/QGPIO[0]	12	5 V
	PCS[1:3]/QGPIO[1:3]		
	MISO/QGPIO[4]		
	MOSI/QGPIO[5]		
	SCK/QGPIO[6]		
	TXD[1:2]/QGPO[1:2]		
	RXD[1:2]/QGPI[1:2]		
	ECK		
MIOS	MDA[11], [13]	18	5 V
	MDA[12], [14]		
	MDA[15], [27:31]		
	MPWM[0:3], [16:19]		
General-Purpose I/O from MIOS	VF[0:2]/MPIO32B[0:2]	5	3-V / 5-V GPIO
	VFLS[0:1]/MPIO32B[3:4]		
	MPIO32B[5:15]	11	5 V
TPU	A_TPUCH[0:15], B_TPUCH[0:15]	34	5 V
	A_T2CLK, B_T2CLK		
QADC	ETRIG[1:2]	34	5 V
	A_AN0/ANW/PQB0, B_AN0/ANW/PQB0		
	A_AN1/ANX/PQB1, B_AN1/ANX/PQB1		
	A_AN2/ANY/PQB2, B_AN2/ANY/PQB2		
	A_AN3/ANZ/PQB3, B_AN3/ANZ/PQB3		
	A_AN[48:51]/PQB[4:7], B_AN[48:51]/PQB[4:7]		
	A_AN[52:54]/MA[0:2]/PQA[0:2], B_AN[52:54]/MA[0:2]/PQA[0:2]		
	A_AN[55:56]/PQA[3:4], B_AN[55:56]/PQA[3:4]		
	A_AN[57:59]/PQA[5:7], B_AN[57:59]/PQA[5:7]		
TouCAN	A_CNTX0, B_CNTX0, A_CNRX0, B_CNRX0	4	5 V
Flash EEPROM	E_{PEE}	1	3 V
Supplies			
Ground	VSS, VSSF, VSSSYN	18	
Analog Ground	VSSA, VRL	2	
Low Voltage Supply	VDDI, VDDL, VDDSRAM, VDDSYN, KAPWR[3], VDDF	16	3 V
High voltage Supply	VDDH, VDDA, VRH	12	5 V
Programming Voltage	VPP	1	3-V / 5-V

NOTES:
1. "/" implies that the corresponding functions are multiplexed on the pin
2. All inputs are 5 V friendly. All 5 V outputs are slow slew rate except for SCI transmit pins.
3. These pins are powered by KAPWR (Keep Alive Power Supply).

2.2 Pin Functionality

The pad ring supports 234 functional pins (284 including all power and ground). Some pins serve multiple functions. The pad characteristics for each pin are described in **Table 2-2**. This table contains the following columns:

- Pin – List of functional (signal) names for each pin. (For actual pin names, see **2.7 Pin Names and Abbreviations**.
- Function – Name of function (signal). Each pin supports one or more functions, and each function (signal) name is a separate entry in the table.
- Driver Type – Type of driver that is used to drive the pin (for output functionality). Types of output drivers are:
  - — Totem pole (TP). This driver type uses a push pull scheme to drive the pin. These pins can be driven high or low or can be three-stated. Care must be taken to ensure that there is no contention on this pin (for example, an external driver driving the pin high while an internal driver is driving it low).
  - — Open drain (OD). This driver type uses an open drain approach to drive the pins. Pins with an OD driver can be either driven low or three-stated. This driver scheme is typically used for pins that could potentially be asserted by multiple modules.
  - — Active negated (ANG). This driver type fully drives a low level. A high level is driven and then released. A pull-up resistor may be needed on this type of output.
- Receiver Type – Type of receiver used for the pin. Some inputs need to have a synchronizer to prevent latching a metastable signal at the pins. Such requirements are indicated in this column with the abbreviation “synch.” Another possible entry is “glitch filter.” It is added to reset signals.
- Direction – Direction of the pin for each function it supports. The possible directions are input (I), output (O) and bi-directional (I/O).
- Voltage – Voltage requirement for each function of a pin. There are two supply voltages: 5 V and 3 V.
- Slew rate – Timing needed from the 5-V drivers. The options are with slew rate (typically 200/50 ns with 50 pF load) or fast 5-V driver.
- Drive strength – Drive strength for 3-V drivers of the output load. For all 3-V outputs, the drive strength is 25/50 pF. For two pads (clkout and engclk) the drive strength is 45/90 pF.
- Pad Type – Functional pad structure used for a pin. For pad type descriptions, see **2.5 Pad Types**.

Table 2-2 Pin Functionality Table

Pin	Function	Type		Direction[1]	Voltage	Slew Rate ns / 50 pF	Drive Strength (pF)	Pad Type
		Driver	Receiver					
USIU								
ADDR[8:31]/ SGPIOA[8:31]	ADDR[8:31]	TP	—	I/O	3 V	—	25 / 50	J
	SGPIOA[8:31]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	
DATA[0:31]/ SGPIOD[0:31]	DATA[0:31]	TP	—	I/O	3 V	—	25 / 50	JD
	SGPIOD[0:31]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	
$\overline{\text{IRQ[0]}}$/ SGPIOC[0]	$\overline{\text{IRQ[0]}}$	—	Hysteresis, Synch	I	3 V	—	—	IH
	SGPIOC[0]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	
$\overline{\text{IRQ[1]}}$/$\overline{\text{RSV}}$/ SGPIOC[1]	$\overline{\text{IRQ[1]}}$	—	Hysteresis, Synch	I	3 V	—	—	IH
	$\overline{\text{RSV}}$	TP	—	O	3 V	—	25 / 50	
	SGPIOC[1]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	
$\overline{\text{IRQ[2]}}$/$\overline{\text{CR}}$/ $\overline{\text{SGPIOC[2]}}$/$\overline{\text{MTS}}$	$\overline{\text{IRQ[2]}}$	—	Hysteresis, Synch	I	3 V	—	—	IH
	$\overline{\text{CR}}$	—	—	I	3 V	—	—	
	SGPIOC[2]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	
	MTS	TP	—	O	3 V	25 / 50	—	
$\overline{\text{IRQ[3]}}$/$\overline{\text{KR}}$, $\overline{\text{RETRY}}$/ SGPIOC[3]	$\overline{\text{IRQ[3]}}$	—	Hysteresis, Synch	I	3 V	—	—	IH
	$\overline{\text{KR}}$, $\overline{\text{RETRY}}$	TP	—	I/O	3 V	—	25 / 50	
	SGPIOC[3]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	
$\overline{\text{IRQ[4]}}$/AT[2]/ SGPIOC[4]	$\overline{\text{IRQ[4]}}$	—	Hysteresis, Synch	I	3 V	—	—	IH
	AT[2]	TP	—	O	3 V	—	25 / 50	
	SGPIOC[4]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	
$\overline{\text{IRQ[5]}}$/ SGPIOC[5]/ MODCK[1][2]	$\overline{\text{IRQ[5]}}$	—	Hysteresis, Synch	I	3 V	—	—	IH
	SGPIOC[5]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	
	MODCK[1]	—	—	I	3 V	—	—	

Table 2-2 Pin Functionality Table (Continued)

Pin	Function	Type		Direction[1]	Voltage	Slew Rate ns / 50 pF	Drive Strength (pF)	Pad Type
		Driver	Receiver					
IRQ[6:7]/ MODCK[2:3][2]	IRQ[6:7]	—	Hysteresis, Synch	I	3 V	—	—	CH
	MODCK[2:3]	—	—	I	3 V	—	—	
TSIZ[0:1]	TSIZ[0:1]	TP	—	I/O	3 V	—	25 / 50	F
RD/WR	RD/WR	TP	—	I/O	3 V	—	25 / 50	F
BURST	BURST	TP	—	I/O	3 V	—	25 / 50	F
BDIP	BDIP	TP	—	I/O	3 V	—	25 / 50	F
TS[3]	TS	ANG	—	I/O	3 V	—	25 / 50	E
TA[3]	TA	ANG	—	I/O	3 V	—	25 / 50	E
TEA	TEA	OD	—	I/O	3 V	—	25 / 50	E
RSTCONF/ TEXP[2]	RSTCONF	—	—	I	3 V	—	—	E
	TEXP	TP	—	O	3 V	—	25 / 50	
OE	OE	TP	—	O	3 V	—	25 / 50	A
BI/STS	BI[3]	ANG	—	I/O	3 V	—	25 / 50	E
	STS	TP	—	O	3 V	—	25 / 50	
CS[0:3]	CS[0:3]	TP	—	O	3 V	—	25 / 50	A
WE[0:3]/BE[0:3]/ AT[0:3]	WE[0:3]/BE[0:3]	TP	—	O	3 V	—	25 / 50	F
	AT[0:3]	TP	—	O	3 V	—	25 / 50	
PORESET[2]	PORESET	—	Hysteresis Glitch filter	I	3 V	—	—	CNH
HRESET[2]	HRESET	OD	Hysteresis Glitch filter	I/O	3 V	—	25 / 50	EOH
SRESET[1,2]	SRESET	OD	Hysteresis Glitch filter	I/O	3 V	—	25 / 50	EOH
SGPIOC[6]/FRZ/ PTR	SGPIOC[6]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	I
	FRZ	TP	—	O	3 V	—	25 / 50	
	PTR	TP	—	O	3 V	—	25 / 50	
SGPIOC[7]/ IRQOUT/LWP[0]	SGPIOC[7]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	I
	IRQOUT	TP	—	O	3 V	—	25 / 50	
	LWP[0]	TP	—	O	3 V	—	25 / 50	

Table 2-2 Pin Functionality Table (Continued)

Pin	Function	Type		Direction[1]	Voltage	Slew Rate ns / 50 pF	Drive Strength (pF)	Pad Type
		Driver	Receiver					
$\overline{BG}$/ VF[0]/ LWP[1]	$\overline{BG}$	TP	—	I/O	3 V	—	25 / 50	G
	VF[0]	TP	—	O	3 V	—	25 / 50	
	LWP[1]	TP	—	O	3 V	—	25 / 50	
$\overline{BR}$/ VF[1]/ IWP[2]	$\overline{BR}$	TP	—	I/O	3 V	—	25 / 50	G
	VF[1]	TP	—	O	3 V	—	25 / 50	
	IWP[2]	TP	—	O	3 V	—	25 / 50	
$\overline{BB}$/ VF[2]/ IWP[3]	$\overline{BB}$[3]	ANG	—	I/O	3 V	—	25 / 50	G
	VF[2]	TP	—	O	3 V	—	25 / 50	
	IWP[3]	TP	—	O	3 V	—	25 / 50	
IWP[0:1]/ VFLS[0:1]	IWP[0:1]	TP	—	O	3 V	—	25 / 50	A
	VFLS[0:1]	TP	—	O	3 V	—	25 / 50	
TMS	TMS	—	—	I	3 V	—	—	C
TDI/DSDI	TDI	—	—	I	3 V	—	—	C
	DSDI	—	—	I	3 V	—	—	
TCK/DSCK	TCK	—	—	I	3 V	—	—	D
	DSCK	—	—	I	3 V	—	—	
TDO/DSDO	TDO	TP	—	O	3 V	—	25 / 50	A
	DSDO	TP	—	O	3 V	—	25 / 50	
$\overline{TRST}$	$\overline{TRST}$	—	—	I	3 V	—	—	C
XTAL[2]	XTAL	TP	—	O	3 V	—	—	—
EXTAL[2]	EXTAL	—	—	I	3 V	—	—	—
XFC	XFC	—	—	I/O	3 V	—	—	—
CLKOUT	CLKOUT	TP	—	O	3 V	—	45 / 90	B
EXTCLK[2]	EXTCLK	—	—	I	3 V	—	—	—
ENGCLK/BUCLK	ENGCLK	TP	—	O	5 V	—	45 / 90	S
	BUCLK	TP	—	O	5 V	—	45 / 90	
QSMCM								
PCS0/ $\overline{SS}$/QGPIO[0]	PCS0	TP/OD	Synch/ No Synch	I/O	5 V	50 / fast	—	O
	$\overline{SS}$	TP/OD	Synch/ No Synch	I/O	5 V	50 / fast	—	
	QGPIO[0]	TP/OD	Synch/ No Synch	I/O	5 V	50 / fast	—	

Table 2-2 Pin Functionality Table (Continued)

Pin	Function	Type		Direction[1]	Voltage	Slew Rate ns / 50 pF	Drive Strength (pF)	Pad Type
		Driver	Receiver					
PCS[1:3]/ QGPIO[1:3]	PCS[1:3]	TP/OD	Synch	I/O	5 V	50 / fast	—	O
	QGPIO[1:3]	TP/OD	Synch	I/O	5 V	50 / fast	—	
MISO/QGPIO[4]	MISO	TP/OD	Synch/ No Synch	I/O	5 V	50 / fast	—	O
	QGPIO[4]	TP/OD	Synch/ No Synch	I/O	5 V	50 / fast	—	
MOSI/QGPIO[5]	MOSI	TP/OD	Synch/ No Synch	I/O	5 V	50 / fast	—	O
	QGPIO[5]	TP/OD	Synch/ No Synch	I/O	5 V	50 / fast	—	
SCK/QGPIO[6]	SCK	TP/OD	Synch/ No Synch	I/O	5 V	50 / fast	—	O
	QGPIO[6]	TP/OD	Synch/ No Synch	I/O	5 V	50 / fast	—	
TXD[1:2]/ QGPO[1:2]	TXD[1:2]	TP/OD	—	O	5 V	200 / fast	—	Q
	QGPO[1:2]	TP/OD	—	O	5 V	200 / fast	—	
RXD[1:2]/ QGPI[1:2]	RXD[1:2]	—	—	I	5 V	—	—	R
	QGPI[1:2]	—	—	I	5 V	—	—	
ECK	ECK	—	—	I	5 V	—	—	R
MIOS								
MDA[11:15]	MDA[11:15]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	P
MDA[27:31]	MDA[27:31]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	P
MPWM[0:3], [16:19]	MPWM[0:3], [16:19]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	P
VF[0:2]/ MPIO32B[0:2]	VF[0:2]	TP	—	O	3 V	—	25 / 50	H
	MPIO32B[0:2]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	
VFLS[0:1]/ MPIO32B[3:4]	VFLS[0:1]	TP	—	O	3 V	—	25 / 50	H
	MPIO32B[3:4]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	
MPIO32B[5:15]	MPIO32B[5:15]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	O
TPU_A/TPU_B								
A_TPUCH[0:15]	TPUCH[0:15]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	P

Table 2-2 Pin Functionality Table (Continued)

Pin	Function	Type		Direction[1]	Voltage	Slew Rate ns / 50 pF	Drive Strength (pF)	Pad Type
		Driver	Receiver					
A_T2CLK	T2CLK	TP	Hysteresis Synch	I/O	5 V	200 / fast	—	P
B_TPUCH[0:15]	TPUCH[0:15]	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	P
B_T2CLK	T2CLK	TP	Hysteresis, Synch	I/O	5 V	200 / fast	—	P
QADC_A/QADC_B								
ETRIG[1:2]	ETRIG[1:2]	—	Synch	I	5 V	—	—	N
AN0/ ANW/ PQB0	AN0	—	Analog	I	5 V	—	—	M
	ANW	—	Analog	I	5 V	—	—	
	PQB0	—	Hysteresis, Synch	I	5 V	—	—	
AN1/ANX/PQB1	AN1	—	Analog	I	5 V	—	—	M
	ANX	—	Analog	I	5 V	—	—	
	PQB1	—	Hysteresis, Synch	I	5 V	—	—	
AN2/ANY/PQB2	AN2	—	Analog	I	5 V	—	—	M
	ANY	—	Analog	I	5 V	—	—	
	PQB2	—	Hysteresis, Synch	I	5 V	—	—	
AN3/ANZ/PQB3	AN3	—	Analog	I	5 V	—	—	M
	ANZ	—	Analog	I	5 V	—	—	
	PQB3	—	Hysteresis, Synch	I	5 V	—	—	
AN[48:51]/ PQB[4:7]	AN[48:51]	—	Analog	I	5 V	—	—	M
	PQB[4:7]	—	Hysteresis, Synch	I	5 V	—	—	
AN[52:54]/ MA[0:2]/PQA[0:2]	AN[52:54]	—	Analog	I	5 V	—	—	L
	MA[0:2]	OD	—	O	5 V	—	—	
	PQA[0:2]	OD	Hysteresis, Synch	I/O	5 V	—	—	
AN[55:56]/ PQA[3:4]	AN[55:56]	—	Analog	I	5 V	—	—	L
	PQA[3:4]	OD	Hysteresis, Synch	I/O	5 V	—	—	

Table 2-2 Pin Functionality Table (Continued)

Pin	Function	Type		Direction[1]	Voltage	Slew Rate ns / 50 pF	Drive Strength (pF)	Pad Type
		Driver	Receiver					
AN[57:59]/ PQA[5:7]	AN[57:59]	—	Analog	I	5 V	—	—	L
	PQA[5:7]	OD	Hysteresis, Synch	I/O	5 V	—	—	
AN0/ANW/PQB0	AN0	—	Analog	I	5 V	—	—	M
	ANW	—	Analog	I	5 V	—	—	
	PQB0	—	Hysteresis, Synch	I	5 V	—	—	
AN1/ANX/PQB1	AN1	—	Analog	I	5 V	—	—	M
	ANX	—	Analog	I	5 V	—	—	
	PQB1	—	Hysteresis, Synch	I	5 V	—	—	
AN2/ANY/PQB2	AN2	—	Analog	I	5 V	—	—	M
	ANY	—	Analog	I	5 V	—	—	
	PQB2	—	Hysteresis, Synch	I	5 V	—	—	
AN3/ANZ/PQB3	AN3	—	Analog	I	5 V	—	—	M
	ANZ	—	Analog	I	5 V	—	—	
	PQB3	—	Hysteresis, Synch	I	5 V	—	—	
AN[48:51]/ PQB[4:7]	AN[48:51]	—	Analog	I	5 V	—	—	M
	PQB[4:7]	—	Hysteresis, Synch	I	5 V	—	—	
AN[52:54]/ MA[0:2]/PQA[0:2]	AN[52:54]	—	Analog	I	5 V	—	—	L
	MA[0:2]	OD	—	O	5 V	—	—	
	PQA[0:2]	OD	Hysteresis, Synch	I/O	5 V	—	—	
AN[55:56]/ PQA[3:4]	AN[55:56]	—	Analog	I	5 V	—	—	L
	PQA[3:4]	OD	Hysteresis, Synch	I/O	5 V	—	—	
AN[57:59]/ PQA[5:7]	AN[57:59]	—	Analog	I	5 V	—	—	L
	PQA[5:7]	OD	Hysteresis, Synch	I/O	5 V	—	—	
TOUCAN_A/TOUCAN_B								
A_CNTX0	CNTX0_A	TP/OD	—	O	5 V	50 / fast	—	Q
B_CNTX0	CNTX0_B	TP/OD	—	O	5 V	50 / fast	—	Q

Table 2-2 Pin Functionality Table (Continued)

Pin	Function	Type		Direction[1]	Voltage	Slew Rate ns / 50 pF	Drive Strength (pF)	Pad Type
		Driver	Receiver					
A_CNRX0	CNRX0_A	—	Synch / No Synch	I	5 V	—	—	R
B_CNRX0	CNRX0_B	—	Synch / No Synch	I	5 V	—	—	R
CMF								
EPEE	EPEE	—	Sequencer	I	3 V	—	—	K
VPP	VPP	—	—	I	5 V	—	—	—
Global Power Supplies								
VDDA	VDDA	—	—	I	5 V	—	—	—
VDDF	VDDF	—	—	I	3 V	—	—	—
VDDL	VDDL	—	—	I	3 V	—	—	—
VDDH	VDDH	—	—	I	5 V	—	—	—
VDDI	VDDI	—	—	I	3 V	—	—	—
VDDSYN	VDDSYN	—	—	I	3 V	—	—	—
VRH	VRH	—	—	I	5 V	—	—	—
VRL	VRL	—	—	I	—	—	—	—
VSSA	VSSA	—	—	I	—	—	—	—
VSSF	VSSF	—	—	I	—	—	—	—
VSSSYN	VSSSYN	—	—	I	—	—	—	—
KAPWR[2]	KAPWR	—	—	I	3 V	—	—	—
VDDSRAM	VDDSRAM	—	—	I	3 V	—	—	—
VSS	VSS	—	—	I	—	—	—	—

NOTES:
1. All inputs are 5-V friendly. All 5-V outputs are slow slew rate. The QSMCM and TouCAN pins have some slew rate control, but are faster than the general/purpose I/O and timer pins.
2. These pins are powered by KAPWR (Keep Alive Power Supply).
3. This pin is an active negate signal and may need an external pull-up resister.

2.3 Signal Descriptions

The pad ring supports 234 functional pins (284 including all power and ground). Each pin and the functionality it supports are described in this section. All references to timing in this document are numbers that are expected for a typical case process with a 50-pF load at 25^{o}C. The supply voltages are assumed to be typical, as well: 5 V or 3.3 V. The 5-V supply is generally referred to as the 5-V supply, and the 3.3-V supply is referred to as the 3-V supply in this section.

2.3.1 USIU Pads

2.3.1.1 ADDR[8:31]/SGPIOA[8:31]

Pin Name: addr_sgpioa[8:31] (24 pins)

Address Bus – Specifies the physical address of the bus transaction. The address is driven onto the bus and kept valid until a transfer acknowledge is received from the slave. ADDR8 is the most significant signal for this bus.

SGPIO – This function allows the pins to be used as general purpose inputs/outputs.

2.3.1.2 DATA[0:31]/SGPIOD[0:31]

Pin Name: data_sgpiod[0:31] (32 pins)

Data Bus – Provides the general purpose data path between the chip and all other devices. Although the data path is a maximum of 32 bits wide, it can be sized to support 8-, 16-, or 32-bit transfers. DATA[0] is the MSB of the data bus.

SGPIO – This function allows the pins to be used as general purpose inputs/outputs.

2.3.1.3 $\overline{\text{IRQ[0]}}$/SGPIOC[0]

Pin Name: irq0_b_sgpioc0

Interrupt Request – One of the eight external lines that can request, by means of the internal interrupt controller, a service routine from the RCPU. IRQ0 is a nonmaskable interrupt (NMI).

SGPIO – This function allows the pins to be used as general purpose inputs/outputs.

2.3.1.4 $\overline{\text{IRQ[1]}}$/RSV_B/SGPIOC[1]

Pin Name: irq1_b_rsv_b_sgpioc1

Interrupt Request – One of the eight external lines that can request, by means of the internal interrupt controller, a service routine from the RCPU.

Reservation – This line used together with the address bus to indicate that the internal core initiated a transfer as a result of a STWCX or a LWARX instruction.

SGPIO – This function allows the pins to be used as general purpose inputs/outputs.

2.3.1.5 $\overline{\text{IRQ[2]}}$/CR_B/SGPIOC[2]/$\overline{\text{MTS}}$

Pin Name: irq2_b_cr_b_sgpioc2_mts

Interrupt Request – One of the eight external lines that can request, by means of the internal interrupt controller, a service routine from the RCPU.

Cancel Reservation – Instructs the chip to clear its reservation, some other master has touched its reserved space. An external bus snooper would assert this signal.

SGPIO – This function allows the pins to be used as general purpose inputs/outputs.

Memory Transfer Start – This pin is the transfer start signal from the MPC555 memory controller to allow external memory access by an external bus master.

2.3.1.6 IRQ[3]/KR/RETRY/SGPIOC[3]

Pin Name: irq3_b_kr_b_retry_b_sgpioc3

Interrupt Request – One of the eight external lines that can request, by means of the internal interrupt controller, a service routine from the RCPU.

Kill Reservation – In case of a bus cycle initiated by a STWCX instruction issued by the CPU core to a non-local bus on which the storage reservation has been lost, this signal is used by the non-local bus interface to back-off the cycle.

Retry – Indicates to a master that the cycle is terminated but should be repeated. As an input, it is driven by the external slave to retry a cycle.

SGPIO – This function allows the pins to be used as general purpose inputs/outputs.

2.3.1.7 IRQ[4]/AT[2]/SGPIOC[4]

Pin Name: irq4_b_at2_sgpioc4

Interrupt Request – One of the eight external lines that can request, by means of the internal interrupt controller, a service routine from the RCPU.

Address Type – A bit from the address type bus which indicates one of the 16 “address types” to which the address applies. The address type signals are valid at the rising edge of the clock in which the Special Transfer Start ($\overline{\text{STS}}$) is asserted.

SGPIO – This function allows the pins to be used as general purpose inputs/outputs.

2.3.1.8 IRQ[5]/SGPIOC[5]/MODCK[1]

Pin Name: irq5_b_sgpioc5_modck1

Interrupt Request – One of the eight external lines that can request, by means of the internal interrupt controller, a service routine from the RCPU.

SGPIO – This function allows the pins to be used as general purpose inputs/outputs.

Mode Clock [1] – Sampled at the negation of $\overline{\text{PORESET}}$ in order to configure the phase-locked loop (PLL)/clock mode of operation.

2.3.1.9 IRQ[6:7]/MODCK[2:3]

Pin Name: irq6_b_modck2 - irq7_b_modck3 (2 pins)

Interrupt Request – One of the eight external lines that can request, by means of the internal interrupt controller, a service routine from the RCPU.

Mode Clock [2:3] – Sampled at the negation of $\overline{\text{PORESET}}$ in order to configure the PLL/clock mode of operation.

2.3.1.10 TSIZ[0:1]

Pin Name: tsiz0 - tsiz1 (2 pins)

Transfer size – Indicates the size of the requested data transfer in the current bus cycle.

2.3.1.11 RD/$\overline{\text{WR}}$

Pin Name: rd_wr_b

Read/Write – Indicates the direction of the data transfer for a transaction. A logic one indicates a read from a slave device; a logic zero indicates a write to a slave device.

2.3.1.12 $\overline{\text{BURST}}$

Pin Name: burst_b

Burst Indicator – Indicates whether the current transaction is a burst transaction or not.

2.3.1.13 $\overline{\text{BDIP}}$

Pin Name: bdip_b

Burst data in progress – Indicates to the slave that there is a data beat following the current data beat.

2.3.1.14 $\overline{\text{TS}}$

Pin Name: ts_b

Transfer Start – Indicates the start of a bus cycle that transfers data to/from a slave device. This signal is driven by the master only when it gained the ownership of the bus. Every master should negate this signal before the bus relinquish. Every master should negate this signal before the bus is relinquished. This pin is an active negate signal and may need an external pull-up resistor to ensure proper operation and signal timing specifications.

2.3.1.15 $\overline{\text{TA}}$

Pin Name: ta_b

Transfer Acknowledge – This line indicates that the slave device addressed in the current transaction has accepted the data transferred by the master (write) or has driven the data bus with valid data (read). The slave device negates the TA_B signal after the end of the transaction and immediately three-state it to avoid contentions on the line if a new transfer is initiated addressing other slave devices. This pin is an

active negate signal and may need an external pull-up resistor to ensure proper operation and signal timing specifications.

2.3.1.16 $\overline{\text{TEA}}$

Pin Name: tea_b

Transfer Error Acknowledge – This signal indicates that a bus error occurred in the current transaction. The MCU asserts this signal when the bus monitor does not detect a bus cycle termination within a reasonable amount of time. The assertion of $\overline{\text{TEA}}$ causes the termination of the current bus cycle, regardless of the state of $\overline{\text{TEA}}$. An external pull-up device is required to negate $\overline{\text{TEA}}$ quickly, before a second error is detected. That is, the pin must be pulled up within one clock cycle of the time it was three-stated by the MPC555.

2.3.1.17 $\overline{\text{RSTCONF}}$/TEXP

Pin Name: rstconf_b_texp

Reset Configuration – Input. This input line is sampled by the chip during the assertion of the $\overline{\text{HRESET}}$ signal in order to sample the reset configuration. If the line is asserted, the configuration mode will be sampled from the external data bus. When this line is negated, the configuration mode adopted by the chip will be the default one.

Timer Expired – This output line reflects the status of the TEXPS bit in the PLPRCR register in the USIU. This indicates an expired timer value.

2.3.1.18 $\overline{\text{OE}}$

Pin Name: oe_b

Output Enable – This output line is asserted when a read access to an external slave controlled by the GPCM in the memory controller is initiated by the chip.

2.3.1.19 $\overline{\text{BI}}$/$\overline{\text{STS}}$

Pin Name: bi_b_sts_b

Burst Inhibit – This bi-directional, active low, three-state line indicates that the slave device addressed in the current burst transaction is not able to support burst transfers. When the chip drives out the signal for a specific transaction, it asserts or negates $\overline{\text{BI}}$ during the transaction according to the value specified by the user in the appropriate control registers. Negation of the signal occurs after the end of the transaction followed by the immediate three-state. This pin is an active negate signal and may need an external pull-up resistor to ensure proper operation and signal timing specifications.

Special Transfer Start – This output signal is driven by the chip to indicate the start of a transaction on the external bus or signals the beginning of an internal transaction in showcycle mode.

2.3.1.20 CS[0:3]

Pin Name: cs0_b - cs3_b (4 pins)

Chip Select – These output signals enable peripheral or memory devices at programmed addresses if defined appropriately in the memory controller. CS0 can be configured to be the global chip select for the boot device.

2.3.1.21 WE[0:3]/BE[0:3]/AT[0:3]

Pin Name: we_b_at[0:3](4 pins)

Write Enable[0:3]/Byte Enable[0:3] – This output line is asserted when a write access to an external slave controlled by the GPCM in the memory controller is initiated by the chip. It can be optionally be asserted on all read and write accesses. See WEBS bit definition in **Table 10-7**. WE0/BE0 is asserted if the data lane DATA[0:7] contains valid data to be stored by the slave device. WE1/BE1 is asserted if the data lane DATA[8:15] contains valid data to be stored by the slave device. WE2/BE2 is asserted if the data line DATA[16:23] contains valid data to be stored by the slave device. WE3/BE3 is asserted if the data lane DATA[24:31] contains valid data to be stored by the slave device.

Address Type – Indicates one of the 16 address types to which the address applies. The address type signals are valid at the rising edge of the clock in which the Special Transfer Start (STS) is asserted.

2.3.1.22 PORESET

Pin Name: poreset_b

Power on Reset – This pin should be activated as a result of a voltage failure on the keep-alive power pins. The pin has a glitch detector to ensure that low spikes of less than 20 ns are rejected. The internal PORESET signal is asserted only if PORESET is asserted for more than 100 ns. See **SECTION 7 RESET** for more details on timing.

2.3.1.23 HRESET

Pin Name: hreset_b

Hard Reset – The chip can detect an external assertion of HRESET only if it occurs while the chip is not asserting reset. After negation of HRESET or SRESET is detected, a 16 cycles period is taken before testing the presence of an external reset. The internal HRESET signal is asserted only if HRESET is asserted for more than 100 ns. To meet external timing requirements, an external pull-up device is required to negate HRESET. See **SECTION 7 RESET** for more details on timing.

2.3.1.24 SRESET

Pin Name: sreset_b

Soft Reset – The chip can detect an external assertion of SRESET only if it occurs while the chip is not asserting reset. After negation of HRESET or SRESET is

detected, a 16-cycle period is taken before testing the presence of an external soft reset. To meet external timing requirements, an external pull-up device is required to negate $\overline{\text{SRESET}}$. See **SECTION 7 RESET** for more details on timing.

2.3.1.25 SGPIOC[6]/FRZ/$\overline{\text{PTR}}$

Pin Name: sgpioc6_frz_ptr_b

SGPIO – This function allows the pins to be used as general purpose inputs/outputs.

Freeze – Indicates that the RCPU is in debug mode.

Program Trace – Indicates an instruction fetch is taking place in order to allow program flow tracking.

2.3.1.26 SGPIOC[7]/$\overline{\text{IRQOUT}}$/LWP[0]

Pin Name: sgpioc7_irqout_b_lwp0

SGPIO – This function allows the pins to be used as general purpose inputs/outputs.

Interrupt Out – Indicates that an interrupt has been requested to all external devices.

Load/Store Watchpoint 0 – This output line reports the detection of a data watchpoint in the program flow executed by the RCPU. See **SECTION 21 DEVELOPMENT SUPPORT** for more details.

2.3.1.27 $\overline{\text{BG}}$/VF[0]/LWP[1]

Pin Name: bg_b_vf0_lwp1

Bus Grant – Indicates external data bus status. Is asserted low when the arbiter of the external bus grants to the specific master the ownership of the bus.

Visible Instruction Queue Flush Status – This output line together with VF1 and VF2 is output by the chip when a program instructions flow tracking is required by the user. VF report the number of instructions flushed from the instruction queue in the internal core. See **SECTION 21 DEVELOPMENT SUPPORT** for more details.

Load/Store Watchpoint – This output line reports the detection of a data watchpoint in the program flow executed by the RCPU.

2.3.1.28 $\overline{\text{BR}}$/VF[1]/IWP[2]

Pin Name: br_b_vf1_iwp2

Bus Request – Indicates that the data bus has been requested for external cycle.

Visible Instruction Queue Flush Status – This output line together with VF1 and VF2 is output by the chip when a program instructions flow tracking is required by the user. VF report the number of instructions flushed from the instruction queue in the internal core. See **SECTION 21 DEVELOPMENT SUPPORT** for more details.

Instruction Watchpoint 2 – This output line reports the detection of an instruction watchpoint in the program flow executed by the RCPU.

2.3.1.29 $\overline{BB}$/VF[2]/IWP[3]

Pin Name: bb_b_vf2_iwp3

Bus Busy – Indicates that the master is using the bus. This pin is an active negate signal and may need an external pull-up resistor to ensure proper operation and signal timing specifications.

Visible Instruction Queue Flush Status – This output line together with VF0 and VF1 is output by the chip when a program instructions flow tracking is required by the user. VF report the number of instructions flushed from the instruction queue in the internal core.

Instruction Watchpoint 3 – This output line reports the detection of an instruction watchpoint in the program flow executed by the internal core.

2.3.1.30 IWP[0:1]/VFLS[0:1]

Pin Name: iwp0_vfls0 - iwp1_vfls1 (2 pins)

Instruction Watchpoint – These output lines report the detection of an instruction watchpoint in the program flow executed by the RCPU.

Visible History Buffer Flush Status – These signals are output by the chip to enable program instruction flow tracking. They report the number of instructions flushed from the history buffer in the RCPU. See **SECTION 21 DEVELOPMENT SUPPORT** for details.

2.3.1.31 TMS

Pin Name: tms

Test Mode Select – This input controls test mode operations for on-board test logic (JTAG).

2.3.1.32 TDI/DSDI

Pin Name: tdi_dsdi

Test Data In – This input is used for serial test instructions and test data for on-board test logic (JTAG).

Development Serial Data Input – This input line is the data in for the debug port interface. See **SECTION 21 DEVELOPMENT SUPPORT** for details.

2.3.1.33 TCK/DSCK

Pin Name: tck_dsck

Test Clock – This input provides a clock for on-board test logic (JTAG).

Development Serial Clock – This input line is the clock for the debug port interface. See **SECTION 21 DEVELOPMENT SUPPORT** for details.

2.3.1.34 TDO/DSDO

Pin Name: tdo_dsdo

Test Data Out – This output is used for serial test instructions and test data for on-board test logic (JTAG).

Development Serial Data Output – This output line is the data-out line of the debug port interface. See **SECTION 21 DEVELOPMENT SUPPORT** for details.

2.3.1.35 $\overline{\text{TRST}}$

Pin Name: trst_b

Test Reset – This input provides asynchronous reset to the test logic (JTAG).

For non-JTAG test applications, $\overline{\text{TRST}}$ should be connected to ground or $\overline{\text{PORESET}}$ via an external resistor.

2.3.1.36 XTAL

Pin Name: xtal

XTAL – This output line is one of the connections to an external crystal for the internal oscillator circuitry.

2.3.1.37 EXTAL

Pin Name: extal

EXTAL – This line is one of the connections to an external crystal for the internal oscillator circuitry. If this pin is unused, it must be grounded.

2.3.1.38 XFC

Pin Name: xfc

External Filter Capacitance – This input line is the connection pin for an external capacitor filter for the PLL circuitry.

2.3.1.39 CLKOUT

Pin Name: clkout

Clock Out – This output line is the clock system frequency. The CLKOUT drive strength can be configured to full strength, half strength, or disabled. The drive strength is configured using the COM[0:1] bits in the SCCR register in the USIU.

2.3.1.40 EXTCLK

Pin Name: extclk

EXTCLK – Input. This is the external frequency source for the chip. If this is unused, the pin must be grounded.

2.3.1.41 VDDSYN

Pin Name: vddsyn

VDDSYN – This is the power supply of the PLL circuitry.

2.3.1.42 VSSSYN

Pin Name: vsssyn

VSSSYN – This is the power supply of the PLL circuitry.

2.3.1.43 ENGCLK/BUCLK

Pin Name: engclk_buclk

ENGCLK – This is the engineering clock output. Drive strength can be configured to full strength, half strength or disabled. The drive strength is configured using the EECLK[0:1] bits in the SCCR register in the SIU.

BUCLK – When the chip is in limp mode, it is operating from a less precise on-chip ring oscillator to allow the system to continue minimum functionality until the system clock is fixed. This backup clock can be seen externally based on the values of the EECLK[0:1] bits in the SCCR register in the USIU.

2.3.2 QSMCM PADS

2.3.2.1 PCS0/SS/QGPIO[0]

Pin Name: pcs0_ss_b_qgpio0

PCS0 – This signal provides QSPI peripheral chip select 0.

$\overline{\text{SS}}$ – Assertion of this bi-directional signal places the QSPI in slave mode.

QSPI GPIO[0] – When this pin is not needed for a QSPI application it can be configured as a general purpose input/output.

2.3.2.2 PCS(1:3)/QGPIO[1:3]

Pin Name: pcs1_qgpio1 - pcs3_qgpio3 (3 pins)

PCS[1:3] – These signals provide three QSPI peripheral chip selects.

QGPIO[1:3] – When these pins are not needed for QSPI applications they can be configured as a general purpose input/output.

2.3.2.3 MISO/QGPIO[4]

Pin Name: miso_qgpio4

Master-In Slave-Out (MISO) – This bi-directional signal furnishes serial data input to the QSPI in master mode, and serial data output from the QSPI in slave mode.

QGPIO[4] – When this pin is not needed for a QSPI application it can be configured as a general purpose input/output.

2.3.2.4 MOSI/QGPIO[5]

Pin Name: mosi_qgpio5

Master-Out Slave-In (MOSI) – This bi-directional signal furnishes serial data output from the QSPI in master mode and serial data input to the QSPI in slave mode.

QGPIO[5] – When this pin is not needed for a QSPI application it can be configured as a general purpose input/output.

2.3.2.5 SCK/QGPIO[6]

Pin Name: sck_qgpio6

SCK – This bi-directional signal furnishes the clock from the QSPI in master mode or furnishes the clock to the QSPI in slave mode.

QGPIO[6] – When this pin is not needed for a QSPI application, it can be configured as a general purpose input/output. When the QSPI is enabled for serial transmitting, the pin can *not* function as a GPIO.

2.3.2.6 TXD[1:2]/QGPO[1:2]

Pin Name: txd1_qgpo1 - txd2_qgpo2 (2 pins)

Transmit Data – These output signals are the serial data outputs from the SCI1 and SCI2.

QSCI GPO[1:2] – When these pins are not needed for a SCI applications, they can be configured as general-purpose outputs. When the transmit enable bit in the SCI control register is set to a logic 1, these pins can *not* function as general purpose outputs

2.3.2.7 RXD[1:2]/QGPI[1:2]

Pin Name: rxd1_qgpi1 - rxd2_qgpi2 (2 pins)

Receive Data – These input signals furnish serial data inputs to the SCI1 and SCI2.

QSCI GPI[1:2] – When these pins are not needed for SCI applications they can be configured as general purpose inputs. When the receive enable bit in the SCI control register is set to a logic 1, these pins can *not* function as general purpose inputs.

2.3.2.8 ECK

Pin Name: eck

External Baud Clock (EBCK) – This signal provides an external baud clock used by SCI1 and SCI2.

2.3.3 MIOS PADS

2.3.3.1 MDA[11], [13]

Pin Name: mda11, mda13 (2 pins)

Double Action – Each of these pins provide a path for two 16-bit input captures and two 16-bit output compares.

Clock Input – Each of these pins provide a clock input to the modulus counter submodule. MDA11 can be used as the clock input to the MMCSM6 modulus counter. MDA13 can be used as the clock input to the MMCSM22 modulus counter.

2.3.3.2 MDA[12], [14]

Pin Name: mda12, mda14, (2 pins)

Double Action – Each of these pins provide a path for two 16-bit input captures and two 16-bit output compares.

Load Input – Each of these pins provide a load input to the modulus counter submodule. MDA12 can be used as the load input to the MMCSM6 modulus counter. MDA14 can be used as the load input to the MMCSM22 modulus counter.

2.3.3.3 MDA[15], [27:31]

Pin Name: mda15, mda27 - mda31 (6 pins)

Double Action – Each of these pins provide a path for two 16-bit input captures and two 16-bit output compares.

2.3.3.4 MPWM[0:3], [16:19]

Pin Name: mpwm0 - mpwm3, mpwm16 - mpwm19 (8 pins)

Pulse Width Modulation – These pins provide variable pulse width output signals at a wide range of frequencies.

2.3.3.5 VF[0:2]/MPIO32B[0:2]

Pin Name: vf0_mpio32b0 - vf2_mpio32b2 (3 pins)

Visible Instruction Queue Flush Status – These lines output by the chip when Program instruction flow tracking is required by the user. VF reports the number of instructions flushed from the instruction queue in the internal core.

MIOS GPIO – This function allows the pins to be used as general-purpose inputs/outputs.

2.3.3.6 VFLS[0:1]/MPIO32B[3:4]

Pin Name: vfls0_mpio32b3 - vfls1_mpio32b4 (2 pins)

Visible History Buffer Flush Status – These signals are output by the chip to allow program instruction flow tracking. They report the number of instructions flushed from the history buffer in the RCPU. See **SECTION 21 DEVELOPMENT SUPPORT** for details.

MIOS GPIO – This function allows the pins to be used as general purpose inputs/ outputs.

2.3.3.7 MPIO32B[5:15]

Pin Name: mpio32b5 - mpio32b15 (11 pins)

MIOS GPIO – This function allows the pins to be used as general purpose inputs/ outputs.

2.3.4 TPU_A/TPU_B PADS

2.3.4.1 TPUCH[0:15]

Pin Name: a_tpuch0 - a_tpuch15 (16 pins for first TPU), b_tpuch0 - b_tpuch15 (16 pins for second TPU)

TPU Channels – These signals provide each TPU with 16 input/output programmable timed events.

2.3.4.2 T2CLK

Pin Name: a_t2clk (1 pin for first TPU), b_t2clk (1 pin for second TPU)

T2CLK – This signal is used to clock or gate the timer count register 2 (TCR2) within the TPU. This pin is an output-only in special test mode.

2.3.5 QADC_A/QADC_B PADS

2.3.5.1 ETRIG[1:2]

Pin Name: etrig1 - etrig2

ETRIG – These are the external trigger inputs to the QADC_A and QADC_B modules. ETRIG[1] can be configured to be used by both QADC_A and QADC_B. Likewise, ETRIG[2] can be used for both QADC_B and QADC_A. The trigger input pins are associated with the scan queues.

2.3.5.2 AN[0]/ANW/PQB[0]

Pin Name: a_an0_anw_pqb0 (1 pin for first QADC), b_an0_anw_pqb0 (1 pin for second QADC)

Analog Channel (AN0) – Internally multiplexed input-only analog channels. Passed on as a separate signal to the QADC.

Multiplexed Analog Input (ANW) – Externally multiplexed analog input.

Port (PQB0) – Input-only port. This is a 5-V input. This path is synchronized in the pad. The input is level-shifted before it is sent internally to the QADC.

2.3.5.3 AN[1]/ANX/PQB[1]

Pin Name: a_an1_anx_pqb1 (1 pin for first QADC), b_an1_anx_pqb1 (1 pin for second QADC)

Analog Channel (AN1) – Internally multiplexed input-only analog channels. Passed on as a separate signal to the QADC.

Multiplexed Analog Input (ANX) – Externally multiplexed analog input.

Port (PQB1) – Input-only port. This is a 5-V input. This path is synchronized in the pad. The input is level-shifted before being sent internally to the QADC.

2.3.5.4 AN[2]/ANY/PQB[2]

Pin Name: a_an2_any_pqb2 (1 pin for first QADC), b_an2_any_pqb2 (1 pin for second QADC)

Analog Channel (AN2) – Internally multiplexed input-only analog channel. The input is passed on as a separate signal to the QADC.

Multiplexed Analog Input (ANY) – Externally multiplexed analog input.

Port (PQB2) – Input-only port. This is a 5-V input. This path is synchronized in the pad. The input is level-shifted before it is sent internally to the QADC.

2.3.5.5 AN[3]/ANZ/PQB[3]

Pin Name: a_an3_anz_pqb3 (1 pin for first QADC), b_an3_anz_pqb3 (1 pin for second QADC)

Analog Input (AN3) – Internally multiplexed input-only analog channel. The input is passed on as a separate signal to the QADC.

Multiplexed Analog Input (ANZ) – Externally multiplexed analog input.

Port (PQB3) – Input-only port. This is a 5-V input. This path is synchronized in the pad. The input is level-shifted before it is sent internally to the QADC.

2.3.5.6 AN[48:51]/PQB[4:7]

Pin Name: a_an48_pqb4 – a_an51_pqb7 (4 pins for first QADC), b_an48_pqb4 – b_an51_pqb7 (4 pins for second QADC).

Analog Input (AN[48:51]) – Analog input channel. The input is passed on as a separate signal to the QADC.

Port (PQB[4:7]) – Input-only port. Has a synchronizer with an input enable and clock. The input is level-shifted before it is sent internally to the QADC.

2.3.5.7 AN[52:54]/MA[0:2]/PQA[0:2]

Pin Name: a_an52_ma0_pqa0 – a_an54_ma2_pqa2 (3 pins for first QADC), b_an52_ma0_pqa0 – b_an54_ma2_pqa2 (3 pins for second QADC).

Analog Input (AN[52:54]) – Input-only. The input is passed on as a separate signal to the QADC.

Multiplexed Address (MA[0:2]) – Output. Provides a three-bit multiplexed address output to the external multiplexer chip to allow selection of one of the eight inputs.

Port (PQA[0:2]) – Bi-directional.

2.3.5.8 AN[55:59]/PQA[3:7]

Pin Name: a_an55_pqa3 - a_an59_pqa7 (5 pins for first QADC), b_an55_pqa3 – b_an59_pqa7 (5 pins for second QADC).

Analog Input (AN[55:59]) – Input-only. The input is passed on as a separate signal to the QADC.

Port (PQA[3:7]) – Bi-directional.

2.3.5.9 VRH

Pin Name: vrh

VRH – Input pin for high reference voltage for the QADC_A and QADC_B modules.

2.3.5.10 VRL

Pin Name: vrl

VRL – Input pin for low reference voltage for the QADC_A and QADC_B modules.

2.3.5.11 VDDA

Pin Name: vdda

VDDA – Power supply input to analog subsystems of the QADC_A and QADC_B modules.

2.3.5.12 VSSA

Pin Name: vssa

VSSA – Input. Ground level for analog subsystems of the QADC_A and QADC_B modules.

2.3.6 TOUCAN_A/TOUCAN_B PADS

2.3.6.1 CNTX0

Pin Name: a_cntx0 (1 pin for first CAN), b_cntx0 (1 pin for second CAN)

TouCAN Transmit Data 0 – This signal is the serial data output.

2.3.6.2 CNRX0

Pin Name: a_cnrx0 (1 pin for first CAN), b_cnrx0 (1 pin for second CAN)

TouCAN Receive Data – This signal furnishes serial input data.

2.3.7 CMF PADS

2.3.7.1 EPEE

Pin Name: epee

EPEE – Input. This control signal will externally control the program or erase operations.

2.3.7.2 VPP

Pin Name: vpp

VPP – Input. Flash supply voltage (5-V supply) used during program and erase operations of the CMF.

2.3.7.3 VDDF

Pin Name: vddf

VDDF – Flash core voltage input (3-V supply). This separate supply voltage is needed in order to reduce noise in the read path of CMF.

2.3.7.4 VSSF

Pin Name: vssf

VSSF – Flash core zero supply input. This separate supply is needed in order to reduce noise in the read path of CMF.

2.3.8 GLOBAL POWER SUPPLIES

2.3.8.1 VDDL

Pin Name: vddl

VDDL – 3-V voltage supply input.

2.3.8.2 VDDH

Pin Name: vddh

VDDH – 5-V voltage supply input.

2.3.8.3 VDDI

Pin Name: vddi

VDDI – 3-V voltage supply input for internal logic.

2.3.8.4 VSSI

Pin Name: vssi

VSSI – Zero supply input for internal logic. In packaged devices, VSSI is not a separate input from VSS.

2.3.8.5 KAPWR

Pin Name: kapwr

Keep-Alive Power – 3-V voltage supply input for the oscillator and keep-alive registers.

2.3.8.6 VDDSRAM

Pin Name: vddsram

SRAM Keep-Alive Power – 3-V voltage supply input for the SRAM.

2.3.8.7 VSS

Pin Name: vss

VSS – Ground level reference input.

2.4 Reset State

All input pins, with the exception of the power supply and clock related pins, are “weakly pulled” to a value during reset by a 130-microampere resistor based on certain conditions. In reset state all I/O pins become inputs, and all outputs except clkout, hreset_b, sreset_b, will be pulled only by the pull-up/pull-down.

2.4.1 Pin Functionality out of Reset

The functionality out of reset of some pins that support multiple functionality is defined in the SIUMCR through the reset configuration word. For details on which multiplexed pins are configured by the reset configuration word and how they are configured, refer to **7.5.2 Hard Reset Configuration Word**.

The 3-V related pins have selectable output buffer drive strengths which are controlled by the COM[0] bit in the USIU's system clock and reset control register (SCCR). The control is as follows:

0 = 3-V bus pins full drive (50-pF load)*
1 = 3-V bus pins reduced drive (25-pF load)

* The bus pin drive selectability definition is inverted from the selectability of the pin control in the PDMCR register (for the TPU, QADC, USIU (SGPIO), QSPI, TouCAN, QSCI, and MIOS pins).

2.4.2 Pad Module Configuration Register (PDMCR)

The slew rate and weak pull-up/pull-down characteristics of some pins are controlled by bits in the PDMCR. This register resides in the SIU memory map. The contents of the PDMCR are illustrated below. The $\overline{\text{PORESET}}$ signal resets all the PDMCR bits asynchronously.

PDMCR – Pad Module Configuration Register **0x2F C03C**

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SLRC0	SLRC1	SLRC2	SLRC3	Reserved		PRDS	SPRDS	Reserved							
HARD RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
RESERVED															
HARD RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 2-3 PDMCR Bit Settings

Bit(s)	Name	Description
0	SLRC0	SLRC0 controls the slew rate of the following modules: TPU, QADC, USIU (SGPIO). 0 = Slow slew rate for pins. Controls slew rate pins of 200 ns. 1 = Normal slew rate for pins
1	SLRC1	SLRC1 controls the slew rate of the QSPI and TouCAN modules. 0 = Slow slew rate for pins. Controls slew rate pins of 50 ns. 1 = Normal slew rate for pins
2	SLRC2	SLRC2 controls the slew rate of the QSCI module. 0 = Slow slew rate for pins. Controls slew rate pins of 200 ns. 1 = Normal slew rate for pins
3	SLRC3	SLRC3 controls the slew rate of the MIOS module. 0 = Slow slew rate for pins. Controls slew rate pins of 200 ns. 1 = Normal slew rate for pins
4:5	—	Reserved
6	PRDS	The PRDS bit is used to enable or disable the weak pull-up/pull-down devices in the pads related to SGPIO and all pads related to IMB modules. Table 2-4 illustrates which pins are affected by PRDS. 0 = Enable pull-up/pull-down devices 1 = Disable pull-up/pull-down devices

Table 2-3 PDMCR Bit Settings (Continued)

Bit(s)	Name	Description
7	SPRDS	The SPRDS bit is used to enable or disable the weak pull-up/pull-down devices in special 3-V only bus pads. **Table 2-4** illustrates which pins are affected by SPRDS. For more details on how this bit affects the pins see **2.4.7 Special Pull Resistor Disable Control (SPRDS)**. 0 = Enable pull-up/pull-down devices 1 = Disable pull-up/pull-down devices
8:31	—	Reserved

2.4.3 Pin State During Reset

During reset, the functionality of some pins is undetermined. Their functionality is based on the bits in the SIUMCR. Since the SIUMCR bits are undetermined during reset, there is no way of predicting how the pins will function. However, the pins must not cause any spurious conditions or consume an excessive amount of power during reset. To prevent these conditions, the pins need to have a defined reset state. **Table 2-4** describes the reset state of the pins based on pin functionality.

All pins are initialized to a “reset state” during reset. This state remains active until reset is negated or until software disables the pull-up or pull-down device based on the pin functionality. Upon assertion of the corresponding bits in the pin control registers and negation of reset, the pin acquires the functionality that was programmed.

2.4.4 Power-On Reset and Hard Reset

Power-on reset and hard reset affect the functionality of the pins out of reset. (During soft reset, the functionality of the pins is unaltered.) Upon assertion of the power-on reset signal ($\overline{\text{PORESET}}$) the functionality of the pin is not yet known. The pull-up or pull-down resistors are enabled. The reset configuration word configures the system, and towards the end of reset the pin functionality is known. Based upon pin functionality, the pull-up or pull-down devices are either disabled immediately at the negation of reset or remain enabled.

Hard reset can occur at any time, and there may be a bus cycle pending. For this reason, the bits in PDMCR that control the enabling and disabling of the pull-up or pull-down resistors in the pads are set or reset synchronously. ($\overline{\text{PORESET}}$ affects these bits asynchronously.) This causes the pull-up or pull-down resistors to be enabled at a time when they do not cause contention on the pins and are disabled before they can cause any contention on the pins.

2.4.5 Pull-Up and Pull-Down Enable and Disable for 5-V Only Pins

For 5-V only pins, the enabling and disabling of the pull-up and pull-down devices is controlled by the PRDS bit in PDMCR. If the bit is negated, the devices are active. If the bit is asserted, the devices are inactive.

2.4.6 Pull-Up and Pull-Down Enable and Disable for 3-V / 5-V Multiplexed Pins

Two signals are needed to enable or disable the pull-up/pull-down devices in the 3-V / 5-V multiplexed pads:

- The PRDS signal
- An encoded 3-V / 5-V select

2.4.6.1 $\overline{\text{PRDS}}$ Signal

The $\overline{\text{PRDS}}$ signal is derived from the PRDS bit in the PDMCR. A single signal controls all affected pads (all pads related to SGPIO and all pads related to the UIMB modules). The bit is reset by default (pull-ups enabled) and must be explicitly set by software after reset. The bit is reset immediately following power-on reset and by hard reset after data coherency. This bit is not affected by soft reset.

2.4.6.2 Encoded 3-V / 5-V Select

This signal selects between the 3-V functionality and the 5-V functionality of the pin. 5-V operation is selected until the function of the pin is determined (based on the reset configuration word) and $\overline{\text{PORESET}}$ is negated. At this point the 3-V / 5-V select signal assumes the intended state (high for 5 V and low for 3 V).

Upon hard reset assertion, if the 3-V / 5-V select line is in 3-V select mode, it remains in this mode until any external bus access completes. After this the 3-V / 5-V select signal switches to 5-V mode to enable the pull-ups. This ensures that there is no contention on the bus due to the pull-up being enabled. This signal is not affected by soft reset.

Each pad group has a 3-V / 5-V select signal. Internal to the pad, logic combines these signals to control the pull-up.

2.4.6.3 Examples

The combination of this 3-V / 5-V select signal and the resistor disable signal enables or disables the pull-up.The logic to enable the pull-up is:

$$\text{pull\_enable} = \overline{\text{PRDS}} \ \& \ \text{3-V / 5-V select}$$

For example, if a pin is configured a s a GPIO pin (5 V), The 3-V / 5-V select is high throughout reset. This causes the pull-up to be enabled. At the end of reset, the 3-V / 5-V select line remains high. The PRDS is high by default until cleared by software. This causes the pull-up to be enabled until software clears the PRDS bit in the PDMCR.

If a pin is configured as a bus pin (3 V), the 3 V / 5 V remains high throughout reset. This causes the pull-up to be enabled. At the end of reset, the 3-V / 5-V select line goes low. This causes the pull-up to be disabled, preventing any power loss if the MCU starts fetching from external memory immediately out of reset.

2.4.7 Special Pull Resistor Disable Control (SPRDS)

For the pins that support debug and opcode-tracking functionality, the pull-up and pull-down resistors are controlled by the SPRDS signal, which is somewhat like the encoded 3-V / 5-V select. During reset this signal is used synchronously to enable the pull-up resistors in the pads. On negation of reset, based on which functionality is

selected for the pins, this signal is set to disable the pull-up resistors or remains held in its reset state to indicate that the pull-ups are disabled only when the output driver is enabled.

For example, if a pin is configured as a bus arbitration pin, The SPRDS signal remains low throughout reset. This causes the pull-up to be enabled. When reset is released, SPRDS remains low. The output enable for the driver is negated by default. When the output driver is enabled, the pull-up is disabled.

When a pin is configured as an opcode-tracking or debug pin, SPRDS remains low throughout reset. This causes the pull-up to be enabled. When reset is released, SPRDS is asserted. This disables the pull-up resistor immediately. The output driver drives the pin to the required state after reset.

2.4.8 Pin Reset States

Table 2-4 summarizes the reset states of all the pins on the MPC555.

Table 2-4 Pin Reset State

Pin	Function	Port	Voltage	Reset State
USIU				
ADDR[8:31]/ SGPIOA[8:31]	ADDR[8:31]	I/O	3 V	PU5 until reset negates[1]
	SGPIOA[8:31]	IO	5 V	PU5 until PRDS is set
DATA[0:31]/ SGPIOD[0:31]	DATA[0:31]	I/O	3 V	PD until reset negates
	SGPIOD[0:31]	I/O	5 V	PD until PRDS is set
$\overline{\text{IRQ[0]}}$/SGPIOC[0]	$\overline{\text{IRQ[0]}}$	I	3 V	PU5 until reset negates[1]
	SGPIOC[0]	I/O	5 V	PU5 until PRDS is set
$\overline{\text{IRQ[1]}}$/ $\overline{\text{RSV}}$/SGPIOC[1]	$\overline{\text{IRQ[1]}}$	I	3 V	PU5 until reset negates[1]
	$\overline{\text{RSV}}$	O	3 V	PU5 until reset negates[1]
	SGPIOC[1]	I/O	5 V	PU5 until PRDS is set
$\overline{\text{IRQ[2]}}$/ $\overline{\text{CR}}$/SGPIOC[2]/ MTS	$\overline{\text{IRQ[2]}}$	I	3 V	PU5 until reset negates[1]
	$\overline{\text{CR}}$	I	3 V	PU5 until reset negates[1]
	SGPIOC[2]	I/O	5 V	PU5 until PRDS is set
	MTS	O	3 V	PU5 until PRDS negates
$\overline{\text{IRQ[3]}}$/ $\overline{\text{KR}}$, $\overline{\text{RETRY}}$/ SGPIOC[3]	$\overline{\text{IRQ[3]}}$	I	3 V	PU5 until reset negates[1]
	$\overline{\text{KR}}$, $\overline{\text{RETRY}}$	I/O	3 V	PU5 when driver not enabled[2]
	SGPIOC[3]	I/O	5 V	PU5 until PRDS is set
$\overline{\text{IRQ[4]}}$/ AT[2]/ SGPIOC[4]	$\overline{\text{IRQ[4]}}$	I	3 V	PU5 until reset negates[1]
	AT[2]	O	3 V	PU5 until reset negates[1]
	SGPIOC[4]	I/O	5 V	PU5 until PRDS is set

Table 2-4 Pin Reset State (Continued)

Pin	Function	Port	Voltage	Reset State
IRQ[5]/ SGPIOC[5]/ MODCK[1][3]	IRQ[5]	I	3 V	PU5 until reset negates[1]
	SGPIOC[5]	I/O	5 V	PU5 until PRDS is set
	MODCK[1]	I	3 V	PU5 until reset negates[1]
IRQ[6:7]/ MODCK[2:3][3]	IRQ[6:7]	I	3 V	PU3 until SPRDS is set
	MODCK[2:3]	I	3 V	PU3 until reset negates
TSIZ[0:1]	TSIZ[0:1]	I/O	3 V	PD when driver not enabled or until SPRDS is set
RD/WR	RD/WR	I/O	3 V	PU3 when driver not enabled or until SPRDS is set
BURST	BURST	I/O	3 V	PU3 when driver not enabled or until SPRDS is set
BDIP	BDIP	I/O	3 V	PU3 when driver not enabled or until SPRDS is set
TS[4]	TS	I/O	3 V	PU3 when driver not enabled or until SPRDS is set
TA[4]	TA	I/O	3 V	PU3 when driver not enabled or until SPRDS is set
TEA	TEA	I/O	3 V	PU3 when driver not enabled or until SPRDS is set An external pull-up is required in order to negate the pin in appropriate time
RSTCONF/TEXP[3]	RSTCONF	I	3 V	PU3 when driver not enabled or until SPRDS is set
	TEXP	O	3 V	
OE	OE	O	3 V	PU3 until reset negates
BI/STS	BI[4]	I/O	3 V	PU3 when driver not enabled or until SPRDS is set
	STS	O	3 V	
CS[0:3]	CS[0:3]	O	3 V	PU3 until reset negates
WE[0:3]/BE[0:3]/ AT[0:3]	WE[0:3]/BE[0:3]	O	3 V	PU3 when driver not enabled or until SPRDS is set
	AT[0:3]	O	3 V	
PORESET[3]	PORESET	I	3 V	—
HRESET[3]	HRESET	I/O	3 V	PU3 when driver not enabled or until SPRDS is set An external pull-up is required in order to negate the pin in appropriate time
SRESET[3]	SRESET	I/O	3 V	PU3 when driver not enabled or until SPRDS is set An external pull-up is required in order to negate the pin in appropriate time

Table 2-4 Pin Reset State (Continued)

Pin	Function	Port	Voltage	Reset State
SGPIOC[6]/ FRZ/ $\overline{\text{PTR}}$	SGPIOC[6]	I/O	5 V	PU5 until PRDS is set
	FRZ	O	3 V	PU5 until reset negates[1]
	$\overline{\text{PTR}}$	O	3 V	PU5 until reset negates[1]
SGPIOC[7/ $\overline{\text{IRQOUT}}$/LWP[0]	SGPIOC[7]	I/O	5 V	PU5 until PRDS is set
	$\overline{\text{IRQOUT}}$	O	3 V	PU5 until reset negates[1]
	LWP[0]	O	3 V	PU5 until reset negates[1]
$\overline{\text{BG}}$/ VF[0]/ LWP[1]	$\overline{\text{BG}}$	I/O	3 V	PU3 when driver not enabled or until SPRDS is set
	VF[0]	O	3 V	
	LWP[1]	O	3 V	
$\overline{\text{BR}}$/ VF[1]/ IWP[2]	$\overline{\text{BR}}$	I/O	3 V	PU3 when driver not enabled or until SPRDS is set
	VF[1]	O	3 V	
	IWP[2]	O	3 V	
$\overline{\text{BB}}$/ VF[2]/ IWP[3]	$\overline{\text{BB}}$[4]	I/O	3 V	PU3 when driver not enabled or until SPRDS is set
	VF[2]	O	3 V	
	IWP[3]	O	3 V	
IWP[0:1]/ VFLS[0:1]	IWP[0:1]	O	3 V	PU3 until reset negates
	VFLS[0:1]	O	3 V	
TMS	TMS	I	3 V	PU3 until SPRDS is set
TDI/ DSDI	TDI	I	3 V	PU3 until SPRDS is set
	DSDI	I	3 V	
TCK/ DSCK	TCK	I	3 V	PD until SPRDS is set
	DSCK	I	3 V	
TDO/ DSDO	TDO	O	3 V	PU3 until reset negates
	DSDO	O	3 V	
$\overline{\text{TRST}}$	$\overline{\text{TRST}}$	I	3 V	PU3 until SPRDS is set
XTAL[3]	XTAL	I	3 V	—
EXTAL[3]	EXTAL	I	3 V	—
XFC	XFC	I	3 V	—
CLKOUT	CLKOUT	O	3 V	—
EXTCLK[3]	EXTCLK	I	3 V	—
ENGCLK/ BUCLK	ENGCLK	O	5 V	—
	BUCLK	O	5 V	—

Table 2-4 Pin Reset State (Continued)

Pin	Function	Port	Voltage	Reset State
QSMCM				
PCS0/ $\overline{SS}$/ QGPIO[0]	PCS0	I/O	5 V	PU5 until PRDS is set
	$\overline{SS}$	I/O	5 V	
	QGPIO[0]	I/O	5 V	
PCS[1:3]/ QGPIO[1:3]	PCS[1:3]	I/O	5 V	PU5 until PRDS is set
	QGPIO[1:3]	I/O	5 V	
MISO/ QGPIO[4]	MISO	I/O	5 V	PU5 until PRDS is set
	QGPIO[4]	I/O	5 V	
MOSI/ QGPIO[5]	MOSI	I/O	5 V	PU5 until PRDS is set
	QGPIO[5]	I/O	5 V	
SCK/ QGPIO[6]	SCK	I/O	5 V	PU5 until PRDS is set
	QGPIO[6]	I/O	5 V	
TXD[1:2]/ QGPO[1:2]	TXD[1:2]	O	5 V	PU5 until PRDS is set
	QGPO[1:2]	O	5 V	
RXD[1:2]/ QGPI[1:2]	RXD[1:2]	I	5 V	PU5 until PRDS is set
	QGPI[1:2]	I	5 V	
ECK	ECK	I	5 V	PU5 until PRDS is set
MIOS				
MDA[4:13]	MDA[4:13]	I/O	5 V	PU5 until PRDS is set
MPWM[0:3], [16:19]	MPWM[0:3], [16:19]	I/O	5 V	PU5 until PRDS is set
VF[0:2]/ MPIO32B[0:2]	VF[0:2]	O	3 V	PU5 until PRDS is set
	MPIO32B[0:2]	I/O	5 V	
VFLS[0:1]/ MPIO32B[3:4]	VFLS[0:1]	O	3 V	PU5 until PRDS is set
	MPIO32B[3:4]	I/O	5 V	
MPIO32B[5:15]	MPIO32B[5:15]	I/O	5 V	PU5 until PRDS is set
TPU_A/TPU_B				
A: TPUCH[0:15]	TPUCH[0:15]	I/O	5 V	PU5 until PRDS is set
A: T2CLK	T2CLK	I/O	5 V	PU5 when driver not enabled[2]
B: TPUCH[0:15]	TPUCH[0:15]	I/O	5 V	PU5 until PRDS is set
B: T2CLK	T2CLK	I/O	5 V	PU5 when driver not enabled[2]
QADC_A/QADC_B				
ETRIG[1:2]	ETRIG[1:2]	I	5 V	PD

Table 2-4 Pin Reset State (Continued)

Pin	Function	Port	Voltage	Reset State
A: AN0/ANW/ PQB0	AN0	I	5 V	PU5 until PRDS is set
	ANW	I	5 V	PU5 until PRDS is set
	PQB0	I	5 V	PU5 until PRDS is set
A: AN1/ANX/ PQB1	AN1	I	5 V	PU5 until PRDS is set
	ANX	I	5 V	PU5 until PRDS is set
	PQB1	I	5 V	PU5 until PRDS is set
A: AN2/ANY/ PQB2	AN2	I	5 V	PU5 until PRDS is set
	ANY	I	5 V	PU5 until PRDS is set
	PQB2	I	5 V	PU5 until PRDS is set
A: AN3/ANZ/ PQB3	AN3	I	5 V	PU5 until PRDS is set
	ANZ	I	5 V	PU5 until PRDS is set
	PQB3	I	5 V	PU5 until PRDS is set
A: AN[48:51]/ PQB[4:7]	AN[48:51]	I	5 V	PU5 until PRDS is set
	PQB[4:7]	I	5 V	PU5 until PRDS is set
A: AN[52:54]/ MA[0:2]/PQA[0:2]	AN[52:54]	I	5 V	PU5 until PRDS is set
	MA[0:2]	I	5 V	PU5 until PRDS is set
	PQA[0:2]	I/O	5 V	PU5 until PRDS is set
A: AN[55:56]]/ PQA[3:4]	AN[55:56]	I	5 V	PU5 until PRDS is set
	PQA[3:4]	I/O	5 V	PU5 until PRDS is set
A: AN[57:59]/ PQA[5:7]	AN[57:59]	I	5 V	PU5 until PRDS is set
	PQA[5:7]	I/O	5 V	PU5 until PRDS is set
B: AN0/ANW/ PQB0	AN0	I	5 V	PU5 until PRDS is set
	ANW	I	5 V	PU5 until PRDS is set
	PQB0	I	5 V	PU5 until PRDS is set
B: AN1/ANX/ PQB1	AN1	I	5 V	PU5 until PRDS is set
	ANX	I	5 V	PU5 until PRDS is set
	PQB1	I	5 V	PU5 until PRDS is set
B: AN2/ANY/ PQB2	AN2	I	5 V	PU5 until PRDS is set
	ANY	I	5 V	PU5 until PRDS is set
	PQB2	I	5 V	PU5 until PRDS is set
B: AN3/ANZ/ PQB3	AN3	I	5 V	PU5 until PRDS is set
	ANZ	I	5 V	PU5 until PRDS is set
	PQB3	I	5 V	PU5 until PRDS is set

Table 2-4 Pin Reset State (Continued)

Pin	Function	Port	Voltage	Reset State
B: AN[48:51]/ PQB[4:7]	AN[48:51]	I	5 V	PU5 until PRDS is set
	PQB[4:7]	I	5 V	PU5 until PRDS is set
B: AN[52:54]/ MA[0:2]/PQA[0:2]	AN[52:54]	I	5 V	PU5 until PRDS is set
	MA[0:2]	I	5 V	PU5 until PRDS is set
	PQA[0:2]	I/O	5 V	PU5 until PRDS is set
B: AN[55:56]/ PQA[3:4]	AN[55:56]	I	5 V	PU5 until PRDS is set
	PQA[3:4]	I/O	5 V	PU5 until PRDS is set
B: AN[57:59]/ PQA[5:7]	AN[57:59]	I	5 V	PU5 until PRDS is set
	PQA[5:7]	I/O	5 V	PU5 until PRDS is set
VRH	VRH	I	5 V	—
VRL	VRL	I	—	—
VDDA	VDDA	I	5 V	—
VSSA	VSSA	I	—	—
TouCAN_A/TouCAN_B				
A: CNTX0	A_CNTX0	O	5 V	PU5 until PRDS is set
B: CNTX0	B_CNTX0	O	5 V	PU5 until PRDS is set
A: CNRX0	A_CNRX0	I	5 V	PU5 until PRDS is set
B: CNRX0	B_CNRX0	I	5 V	PU5 until PRDS is set
CMF				
EPEE	EPEE	I	3 V	PD
VPP	VPP	I	5 V	—
VDDF	VDDF	I	3 V	—
VSSF	VSSF	I	3 V	—
Global Power Supplies				
VDDL	VDDL	I	3 V	—
VDDH	VDDH	I	5 V	—
VDDI	VDDSI	I	3 V	—
VSSI	VSSI	I	3 V	—
KAPWR[3]	KAPWR	I	3 V	—
VDDSRAM	VDDSRAM	I	3 V	—
VDDSYN	VDDSYN	I	3 V	—
VSS	VSS	I	—	—
VSSSYN	VSSSYN	I	3 V	—

NOTES:

1. During reset, the output enable to the pad driver is negated and the PU3/PU5 is active. After reset is negated, the output enable is continuously enabled and the PU3 is disabled. The driver is responsible for driving a valid state on the pin.
2. Pull-up/pull-down is active when pin is defined as an input and/or during reset; therefore, output enable is negated. This also means that external pull-up/pull-down is *not* required unless specified.
3. These pins are powered by KAPWR (Keep-Alive Power Supply).
4. This pin is an active negate signal and may need an external pull-up resister.

2.5 Pad Types

There are different pad types based on functional characteristics. Even pads with the same functionality may be different due to different electrical characteristics. All 5-V inputs have hysteresis. There is no synchronization in the pads; it is all in the modules.

2.5.1 Pad Interface Signals

The pad interface consists of an internal interface and an external interface. The external interface is to the pin. The internal interface is the set of signals that interface the pad to the chip's internal logic. The following internal interface signals are used:

- Data – The line driven from an internal module of the chip to the pad. For bi-directional pins, the internal interface may be a single line for both input and output or two separate paths for input and output. The descriptions of individual pad types specify which.
- 3-V / 5-V select – Selects a 3-V or 5-V driver, for pads that support both. This signal is driven from the USIU.
- Output enable (OE) – Enables the output driver. For 3-V / 5-V pads, the appropriate driver is enabled based on the pin functionality selected.
- Input enable – Enables the receiver. For 3-V / 5-V pads, the appropriate receiver is enabled based on the pin functionality selected.
- Drive select – Selects the drive strength of the pad. For example, data pin drivers can be configured to drive a 25-pF load or a 50-pF load.
- Synchronizer clock – Some pins have synchronizer logic to handle metastable signals at the input of a pin. For pads that have synchronizers and support synchronized or normal data input, the corresponding interface signals to the internal logic are "Normal Data In" and "Sync Data In."
- Slew rate control – GPIO pins have slow slew rates, with edge rates in the range of 90 ns to 600 ns. The slew rate and weak pull-up/pull-down characteristics of these pins are controlled by bits in the PDMCR, see **2.4.2 Pad Module Configuration Register (PDMCR)**. For a description of PDMCR bits SLRC[0:3] that have controllable slew rates, see **Table 2-3**.
- Hysteresis input – Slow pads contains hysteresis input buffers to reduce the sensitivity to noises. The input hyst_sel is used to configure the pad to provide hysteresis according to the pad configuration.
- Open drain enable – For selected 3-V / 5-V pads, this signal determines the type of drive (open drain or totem pole) seen at the pin.
- Pull resistor disable select (PRDS) – Reflects the state of the PRDS bit in the pad module configuration register (PDMCR). This signal controls the pull-up/pull-down resistor for the SGPIO pins and the pins for the modules on the UIMB.

- Special pull resistor disable select (SPRDS) – Reflects the state of the SPRDS bit in the PDMCR. For pins that support bus arbitration functionality multiplexed with opcode-tracking and debug functionality, this signal controls the pull-up resistors.
- Analog – Analog input signals to the QADC. The corresponding digital interface signals are referred to as “Dig. In” and Dig. Out”.
- JTAG – Joint Test Access Group related signals that are used for connectivity tests at the board level. These signals are not shown in the pad block diagrams in this section. In addition, the effect of the pull-up/pull-down resistors is not illustrated in the pad block diagrams.

These interface signals are referred to in the following pad descriptions and shown in the pad diagrams.

2.5.2 Three-Volt Output Pad

The output driver of a 3-V output-only pad can be configured to drive a 25-pF or 50-pF load. There are two subtypes: one with a pull-up device and the other with a pull-down device. The SPRDS and OE signals enable the pull-up and pull-down resistors.

2.5.2.1 Type A Interface

This pad has a pull-up device to 3 V which can be conditionally turned off based on the value placed on OE. For a totem pole (push pull) pin with no three-state drive time, the OE can be connected to VDD, indicating a continuous drive. For a continuous drive, the pull-up can be disabled.

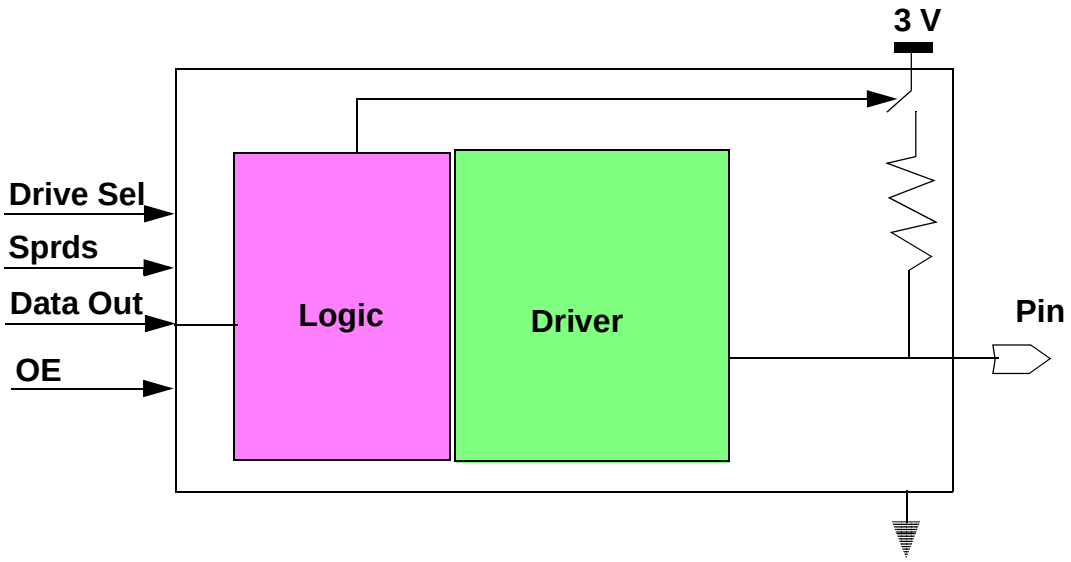


Figure 2-3 Type A Interface

2.5.2.2 Type B Interface (Clock Pad)

The pad has a capability to select the buffer for the appropriate load (45 or 90 pF). The OE input drives the totem pole output or three-states the output.

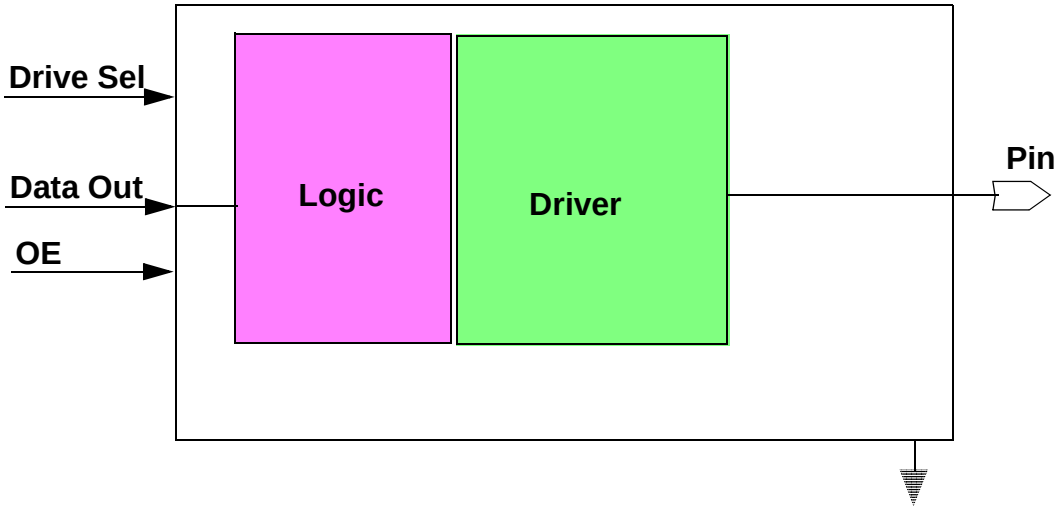


Figure 2-4 Type B Interface

2.5.3 Three-Volt Input Pad

Four subtypes are defined for the 3-V input-only pad: one with a pull-up resistor, one with a pull-up resistor and with or without hysteresis in the receiver, one with hysteresis (no resistor), and one with a pull-down resistor. The SPRDS signal may disable the pull-up or pull-down resistor.

2.5.3.1 Type C Interface

The type C interface has a 3-V input with a pull-up resistor.

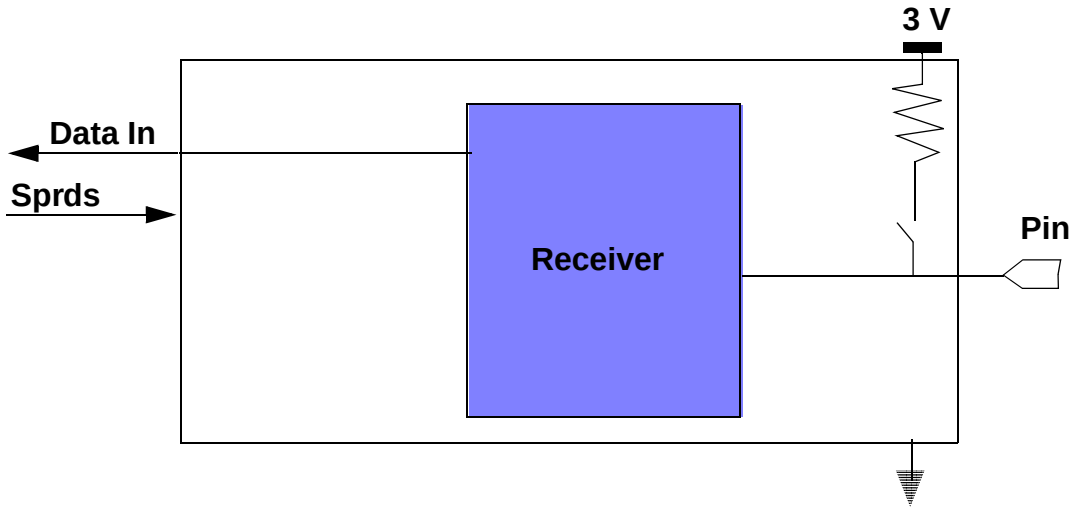


Figure 2-5 Type C Interface

2.5.3.2 Type CH Interface

Pad type CH has a 3-V input with hysteresis and a pull-up resistor. The hyst_sel signal selects the receiver with or without hysteresis.

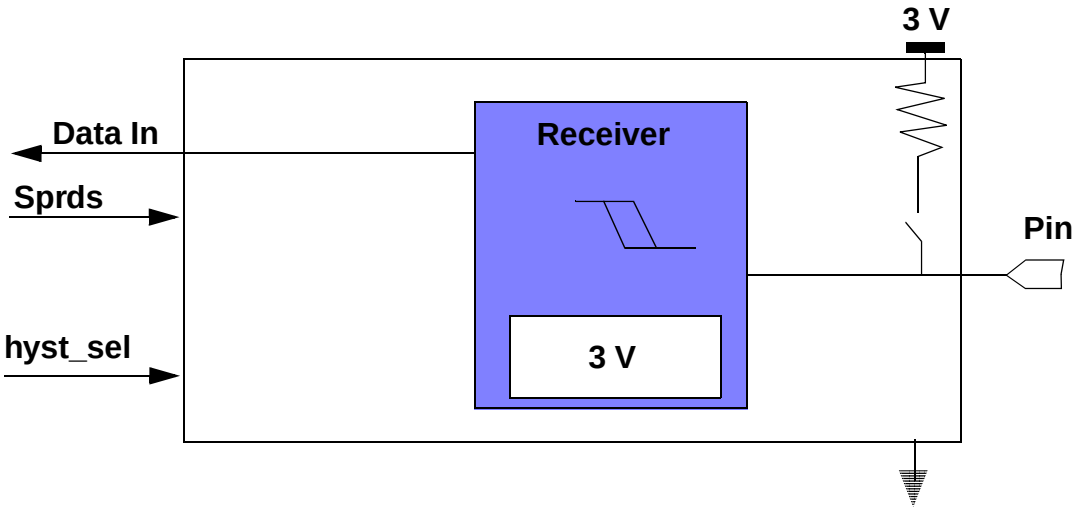


Figure 2-6 Type CH Interface

2.5.3.3 Type CNH Interface

The CNH pad type has a 3-V input with hysteresis but no pull-up or pull-down device.

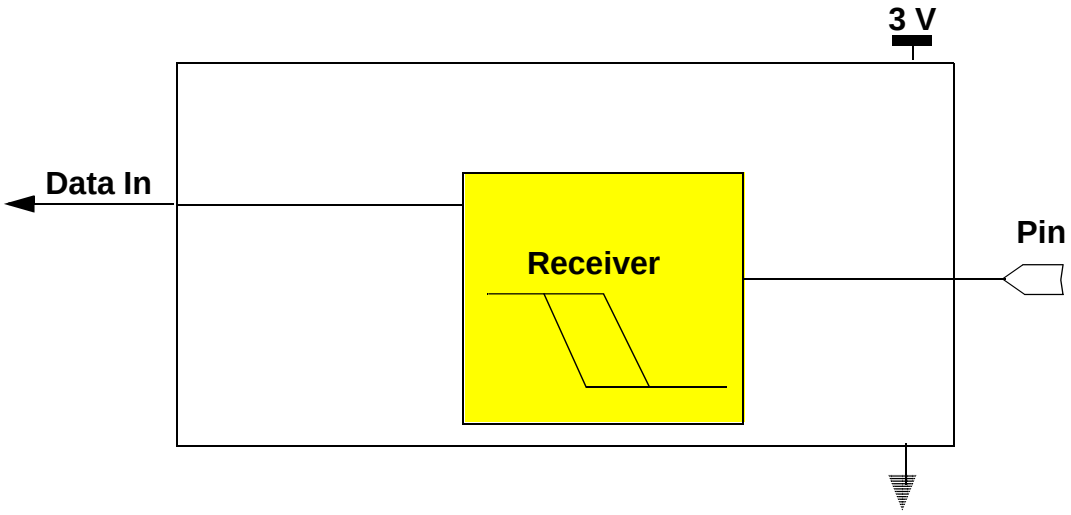


Figure 2-7 Type CNH Interface

2.5.3.4 Type D Interface

This type of pad has a 3-V input and an internal pull-down resistor.

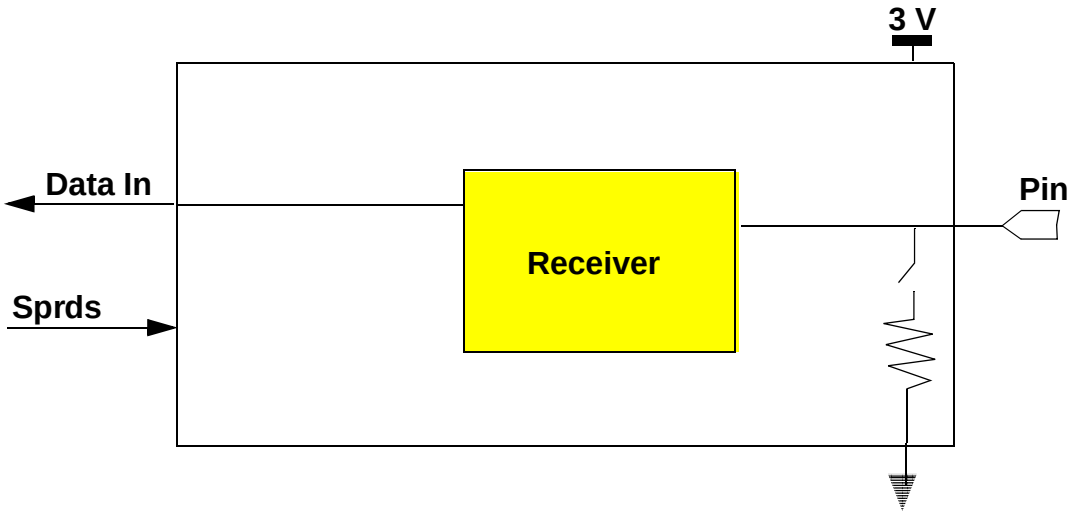


Figure 2-8 Type D Interface

2.5.4 Three-Volt Input/Output Pad

This is a 3-V bi-directional pad with a pull-up device. The drive strength for the output driver can be configured for either a 25-pF or a 50-pF load. The SPRDS and OE signals control the pull-up devices.

2.5.4.1 Type E Interface

In this pad type the data interface to the internal logic has separate paths for input and output. This pad also has a open drain enable input. For totem pole driven outputs, the signal is connected to VSS to disable the open-drain drive.

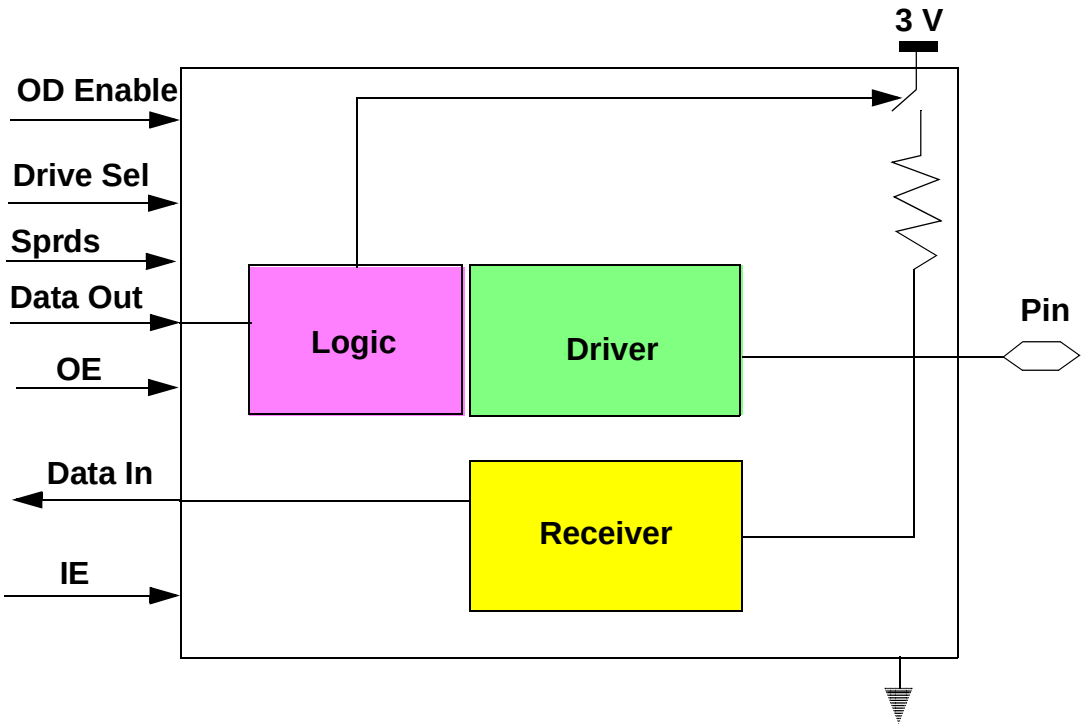


Figure 2-9 Type E Interface

2.5.4.2 Type EOH Interface

In this pad type the data interface to the internal logic has separate paths for input and output. The receiver has hysteresis. The pull-up is active when the driver is not enabled.

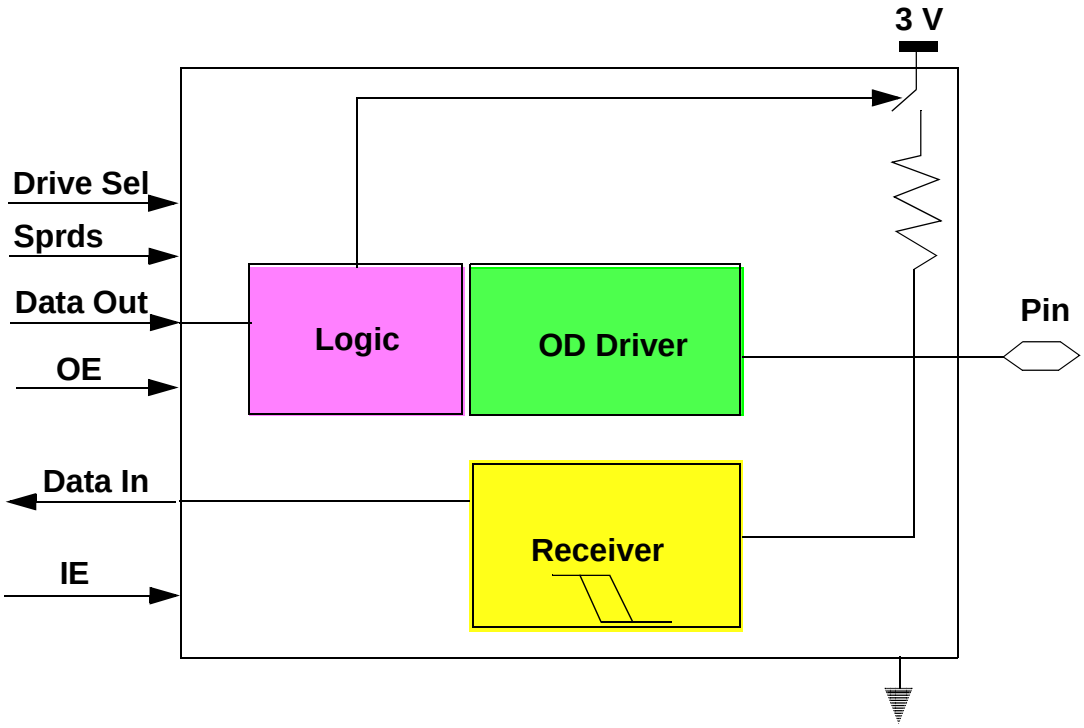


Figure 2-10 3-V Type EOH Interface

2.5.4.3 Type F Interface

In this pad type the data interface to the internal logic has the same path for both input and output. The pull-up is inactive when the driver is enabled.

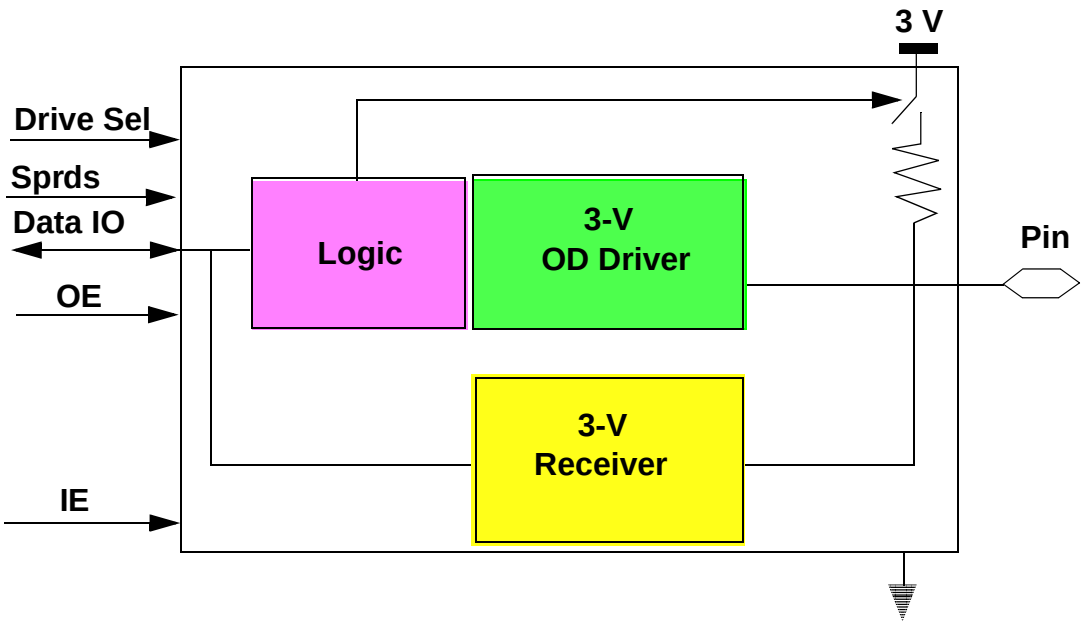


Figure 2-11 Type F Interface

2.5.4.4 Type G Interface

In this pad type the data interface to the internal logic has the same path for both input and output. This pad type also has the SPRDS signal as an input to disable the resistor when the pad is a non-bus function.

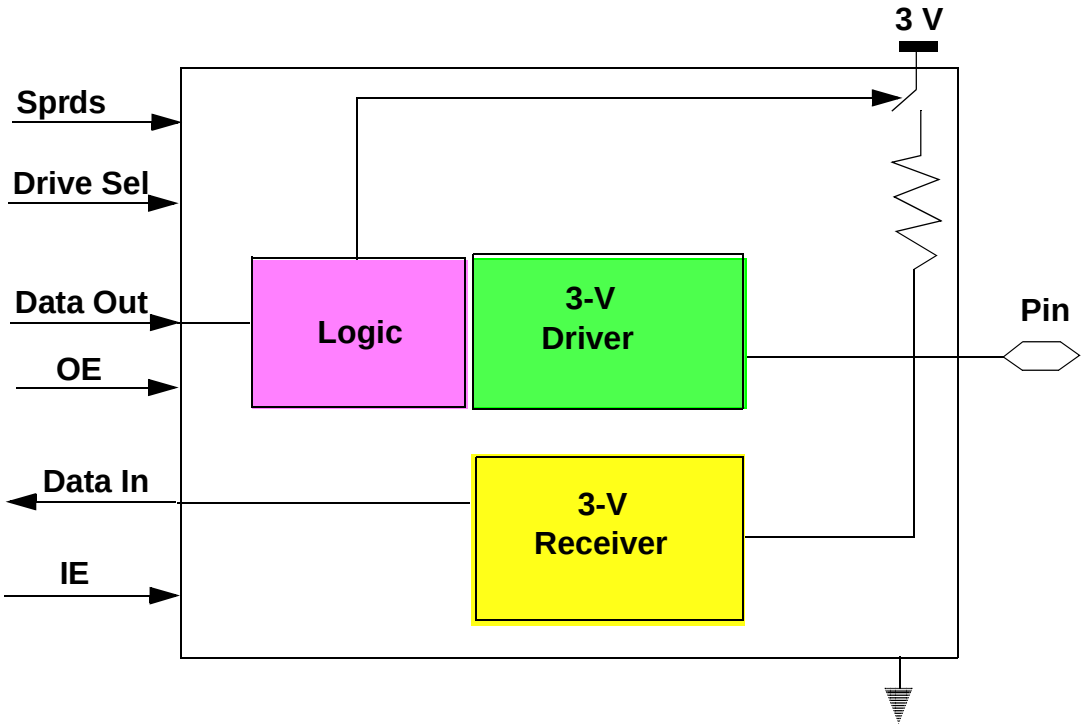


Figure 2-12 Type G Interface

2.5.5 Five-Volt Input/Output Pad

This pad type is for 5-V bi-directional pins. There is provision to pull the pin up to 5 V and logic to control when the pull-up is enabled. For a 5-V driver, the internal “Fast Mode” signal selects the slow or fast driver. All 5-V inputs have hyteresis.

2.5.5.1 Type H Interface

This pad has logic for a 3-V output function as well as a 5-V input-output function. A “3-V / 5-V sel” interface signal determines which driver gets selected.

This pad type has two separate data output paths. These paths are multiplexed onto the output pin based on the 3-V / 5-V select signal. This pad also has a dedicated synchronous input path.

If only one of the output paths is required, the other can be connected to ground. In this case, the 3-V / 5-V select signal must be tied to the appropriate value to disable the other path.

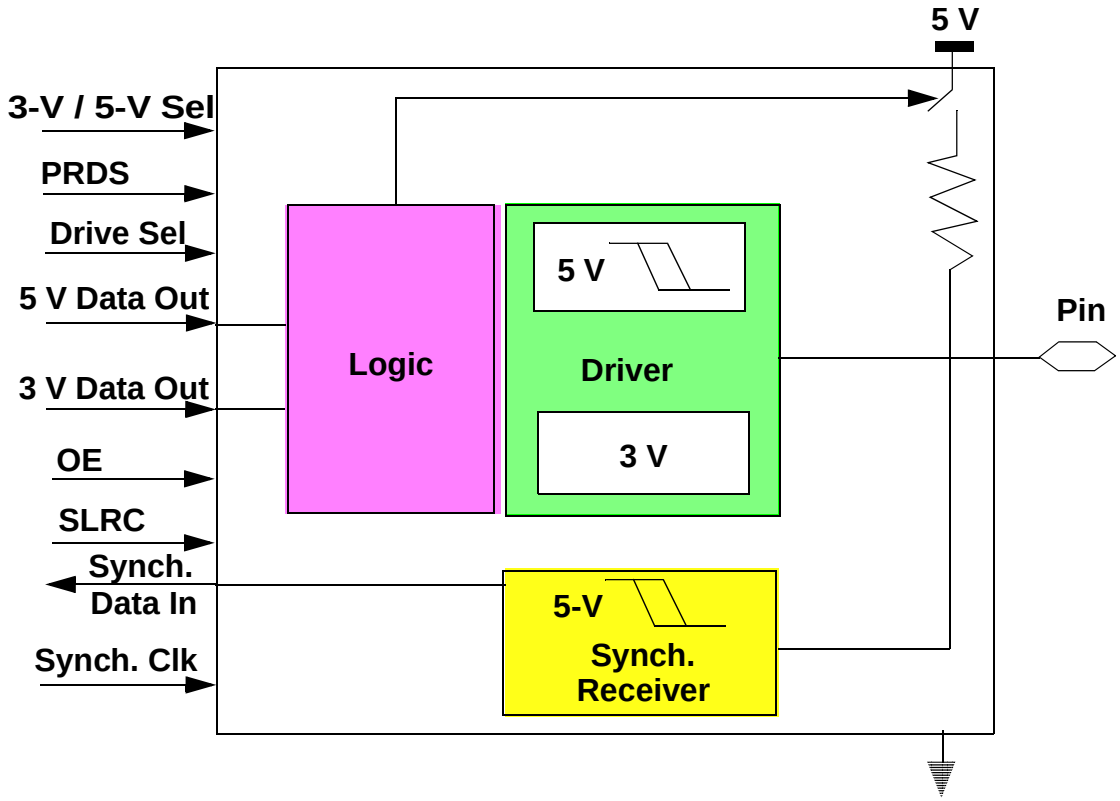


Figure 2-13 Type H Interface

2.5.5.2 Type I Interface

This pad has logic for a 3-V input/output function as well as a 5-V input/output function. A “3-V / 5-V sel” interface signal indicates which driver gets selected.The data interface to the internal logic has separate paths for input and output.

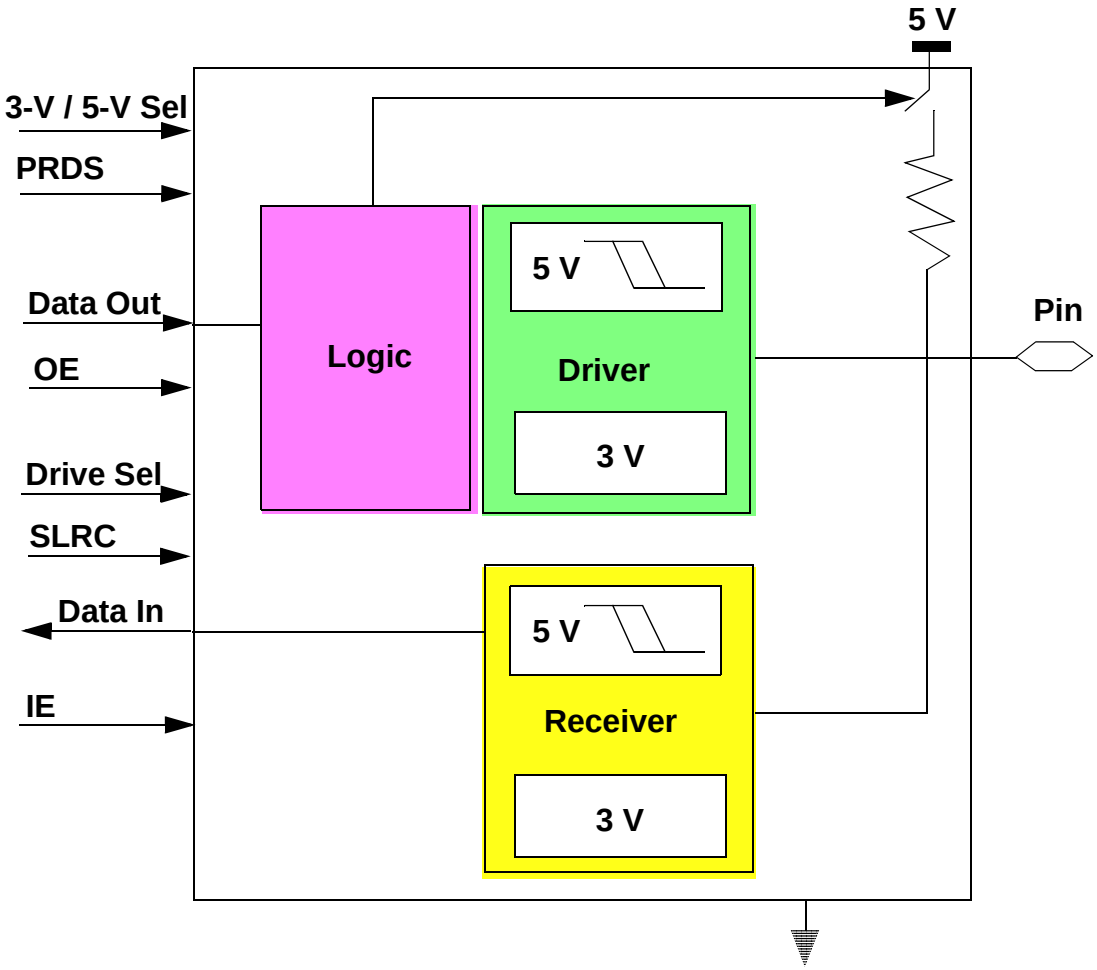


Figure 2-14 Type I Interface

2.5.5.3 Type IH Interface

This pad has logic for a 3-V input/output function as well as a 5-V input/output function. A “3-V / 5-V sel” interface signal determines which driver gets selected.

In this pad type the data interface to the internal logic has separate paths for input and output. The 3-V receiver has 2 possible paths: with or without hysteresis. The hyst_sel signal selects the appropriate path.

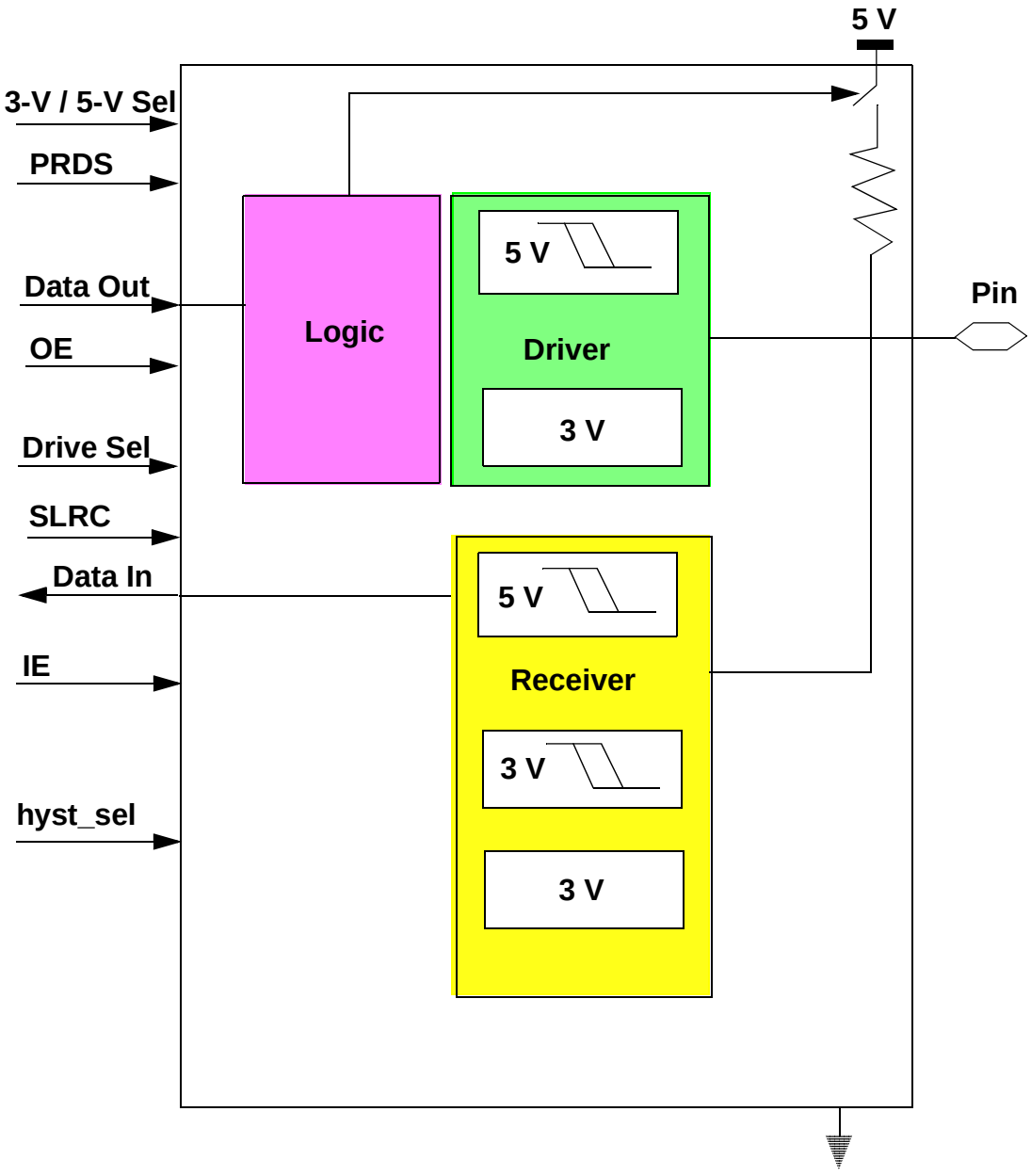


Figure 2-15 Type IH Interface

2.5.5.4 Type J Interface

This pad has logic for a 3-V input/output function as well as a 5-V input/output function. A “3-V / 5-V sel” interface signal indicates which driver gets selected. The data interface to the internal logic has the same path for both input and output.

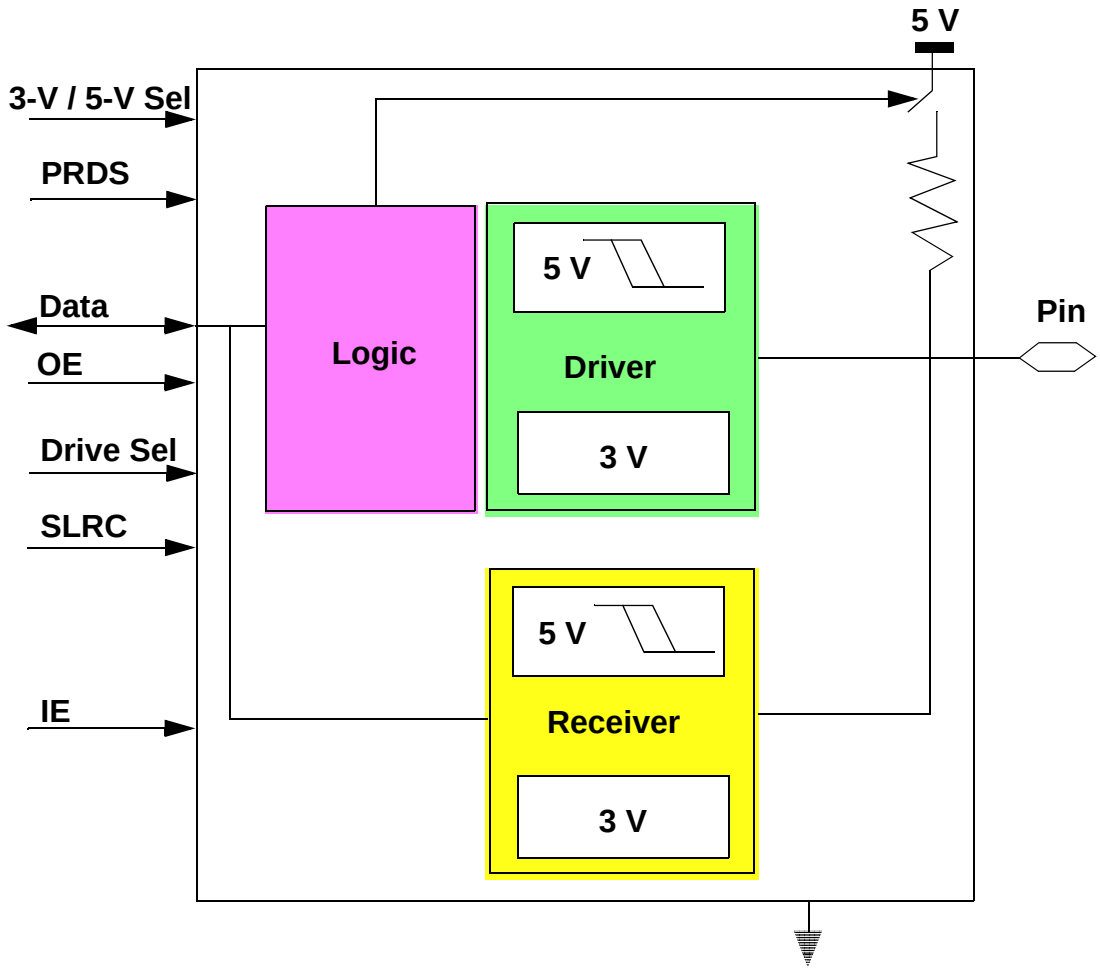


Figure 2-16 Type J Interface

2.5.5.5 Type JD Interface

This pad has logic for a 3-V input/output function as well as a 5-V input/output function. A “3-V / 5-V sel” interface signal indicates which driver gets selected.

The data interface to the internal logic has the same path for both input and output. The pad has a pull-down resistor which is activated by reset and/or PRDS.

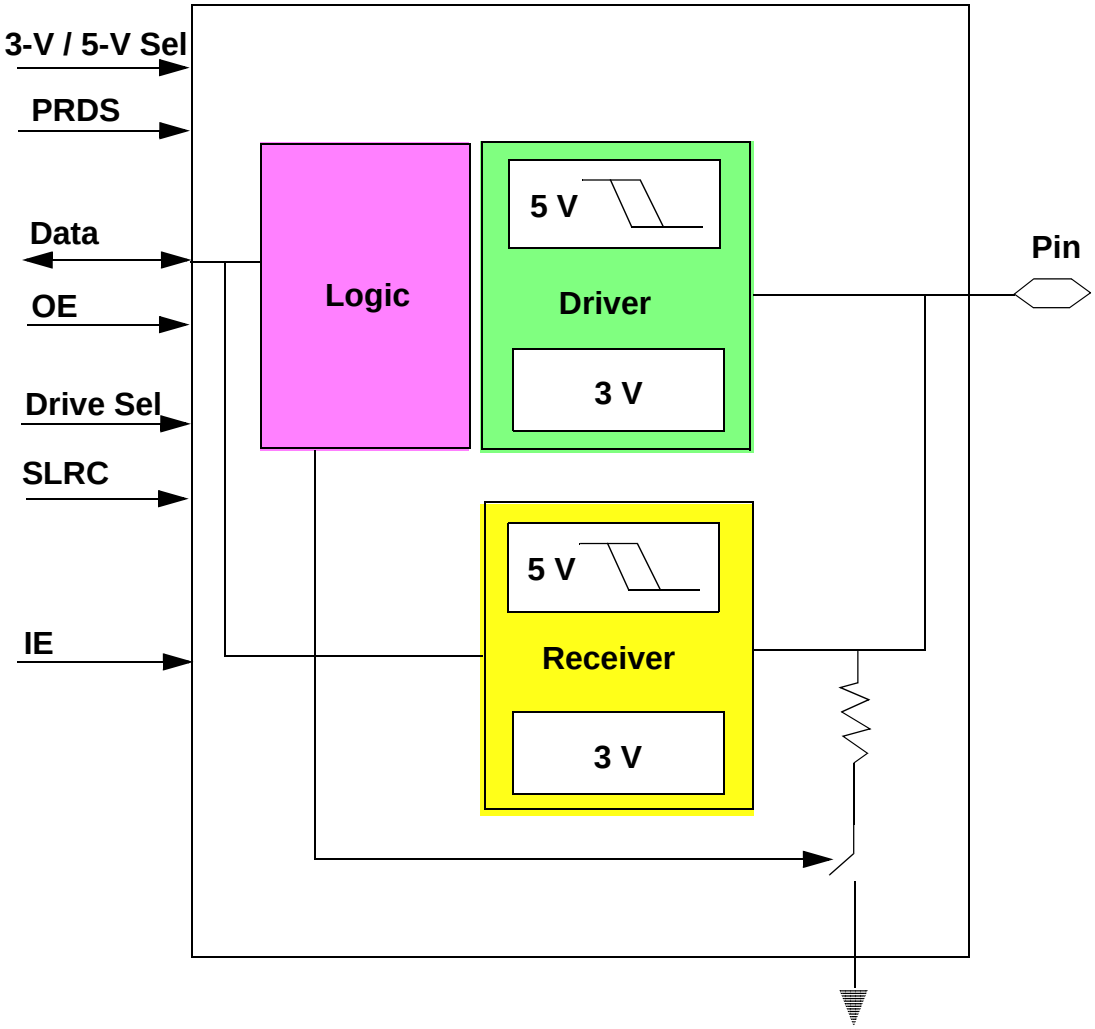


Figure 2-17 Type JD Interface

2.5.6 Type K Interface (EPEE Pad)

This pad has a pull-down device that is enabled at all times. The module checks to see that a transition to a new state on the pin is maintained for at least two clocks before the information is passed on internally to the sequencer implemented in the flash. The synchronizer clock to this pad is GCLK2.

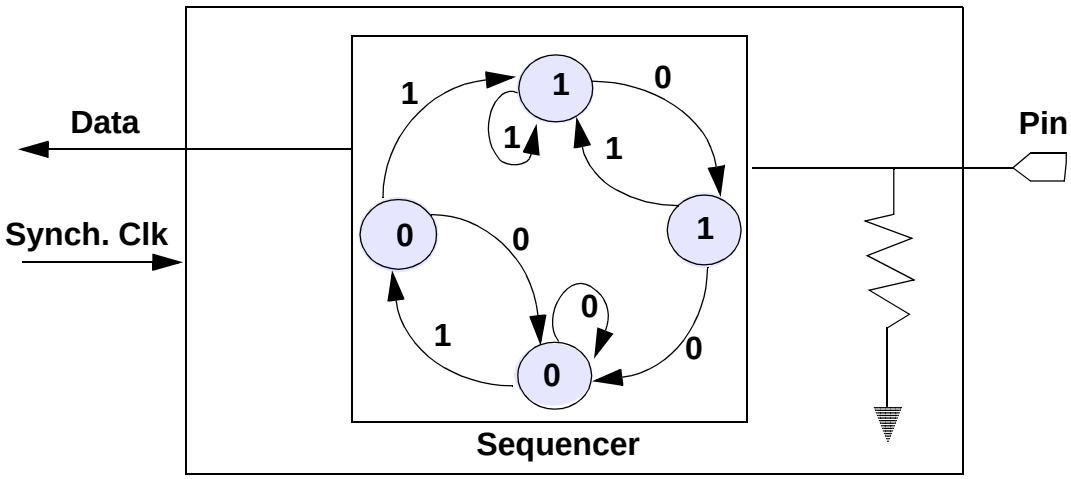


Figure 2-18 EPEE Pad (Type K)

2.5.7 Analog Pads

The 5-V analog pads interface to the QADC modules internally. They have separate analog and digital paths in the pad in order to implement the functionality that is multiplexed on the pin.

2.5.7.1 Type L Interface (QADC Port A)

This pad is used for interfacing to the port A of the QADC. The digital portion of the pad supports bi-directional operation. The receiver has a synchronizer. The digital input is level-shifted from 5 V to 3 V before it is sent internally to the QADC.

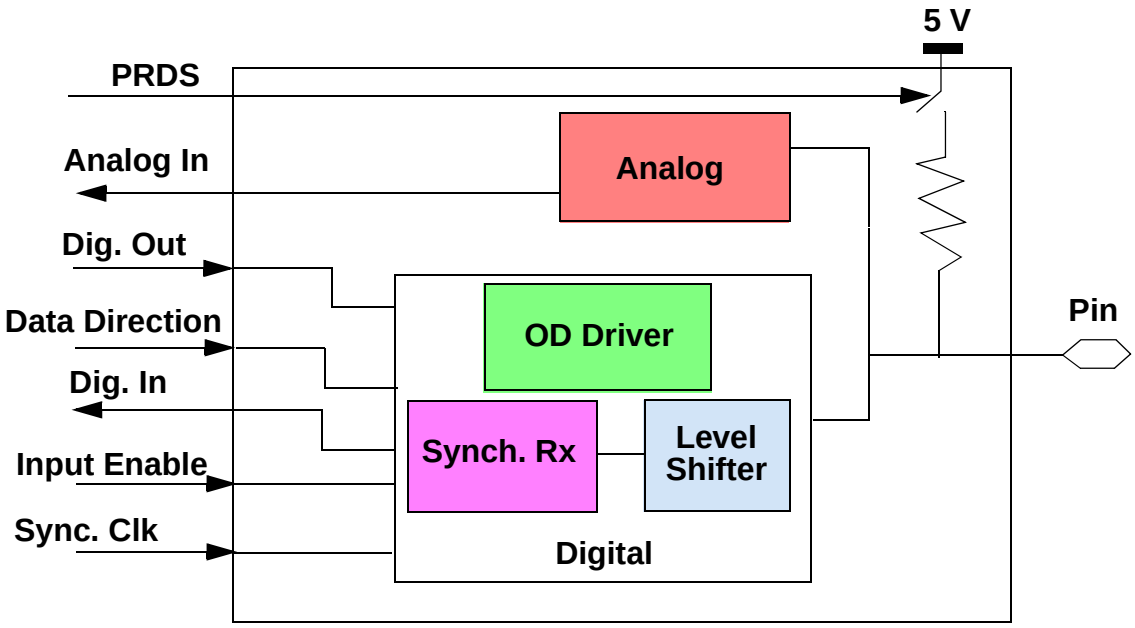


Figure 2-19 Type L Interface

2.5.7.2 Type M Interface (QADC Port B)

This pad is used for interfacing to port B of the QADC. This is an input-only pad. The receiver has a synchronizer. The digital input is level-shifted from 5 V to 3 V before it is sent internally to the QADC.

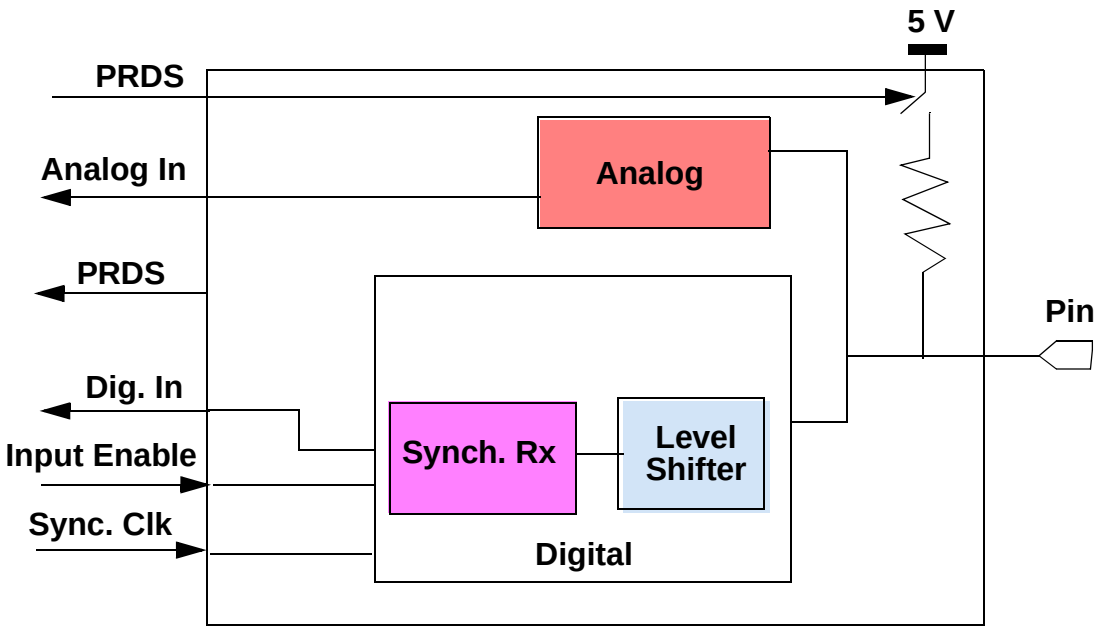


Figure 2-20 Type M Interface

2.5.7.3 Type N Interface (ETRIG)

This is the pad for the ETRIG function of the QADC. The input signal is level-shifted before being sent to the QADC module. The pad also serves as an output pad in test mode.

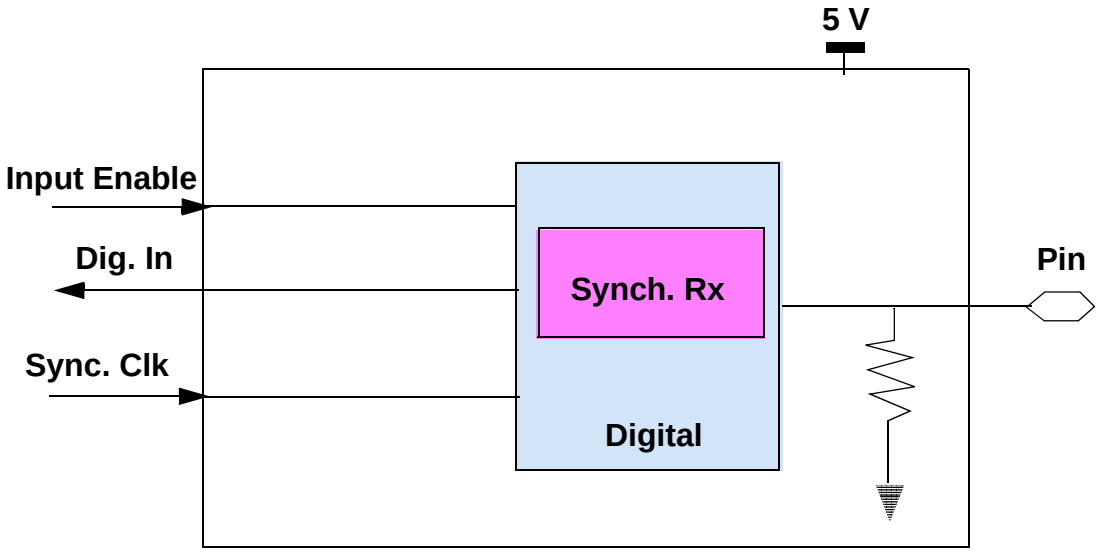


Figure 2-21 Type N Interface

2.5.8 Pads with Fast Mode

The type O pads (for interfacing to the QSMCM) and type P pads (for interfacing to the TPU and MIOS) have a fast mode provision.

2.5.8.1 Type O Interface (QSMCM Pads)

This pad is used for interfacing to the QSMCM. It is a 5-V, bi-directional pad and has provision for a fast mode in which the slow slew rate driver is bypassed and data is driven by a fast slew rate driver. When the pin is an input, the data can be driven either synchronously or asynchronously. A pull-up device is available which can be disabled using the PRDS signal.

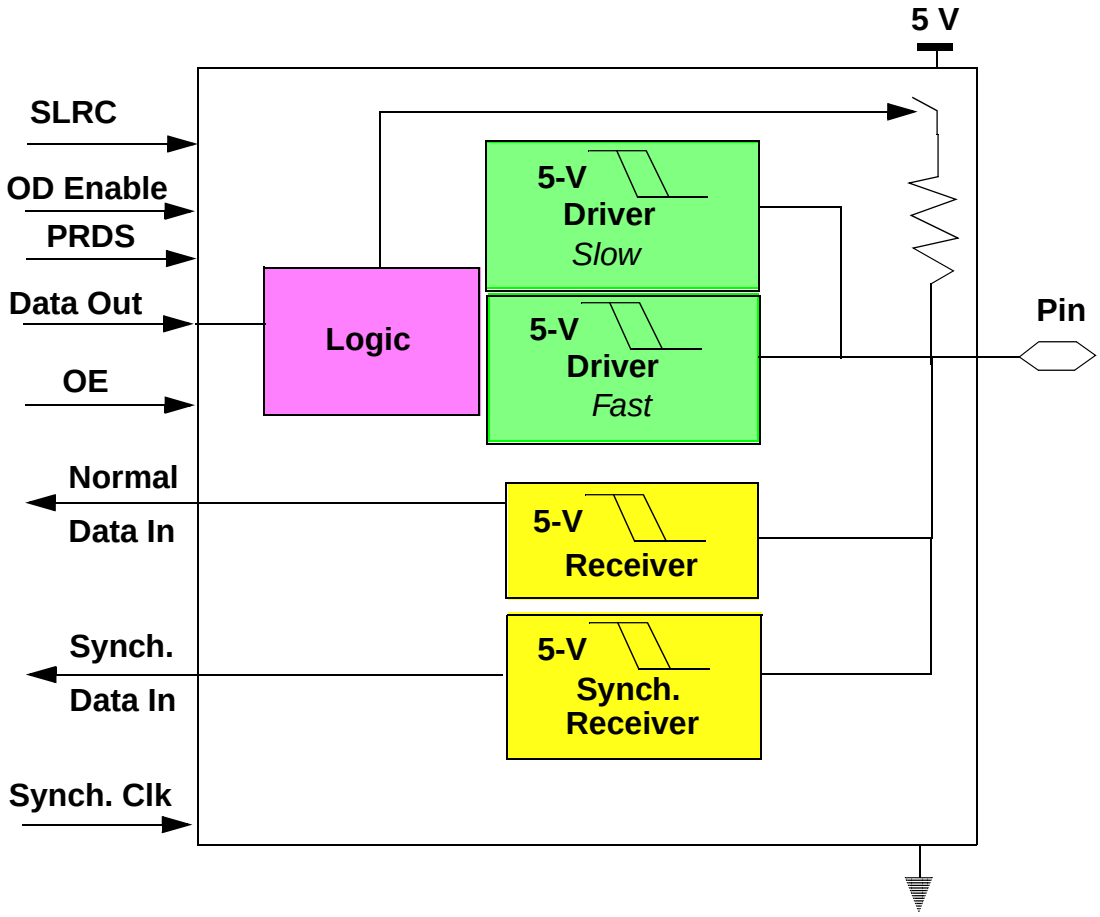


Figure 2-22 Type O Interface

2.5.8.2 Type P Interface (TPU and MIOS Pads)

This is a 5-V, bi-directional pad that has a fast mode provision like the QSMCM pads. The input path is always synchronous. The receiver has hysteresis in order to minimize the effect of noise on the pins. In addition, the receiver has a digital filter (somewhat like the sequencer for the EPEE pad) to check for a state on the pin for a particular number of clocks. The pad also has a pull-up device. Depending on the reset state (see **Table 2-4**) the pull-up may be controlled by the PRDS signal.

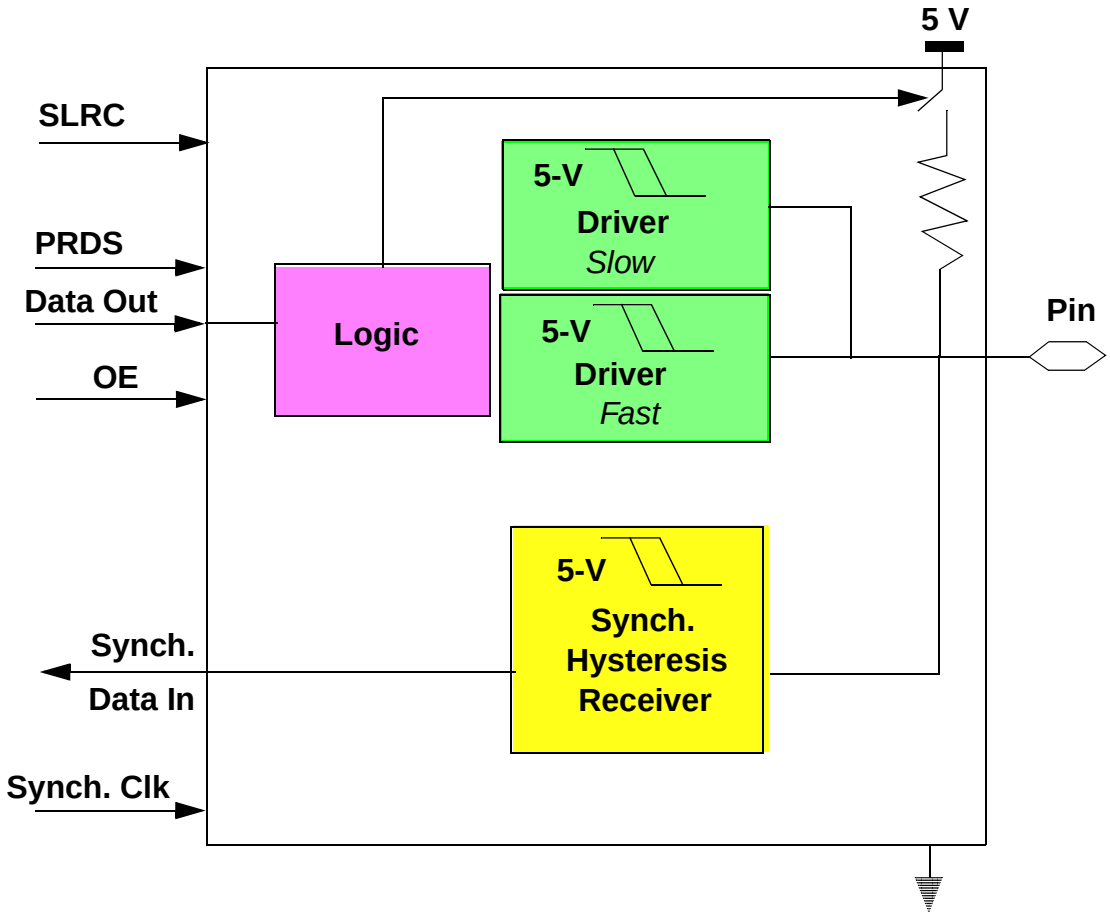


Figure 2-23 Type P Interface

2.5.9 5V Input, 5V Output Pads

These pads are 5-V only pads.

2.5.9.1 5V Output (Type Q)

This pad is a 5-V output-only pad with slow and fast drive capability. The driver is configureable to be either push pull or open drain using the OD enable signal. This pad type has a pull-up device that can be controlled using the PRDS signal.

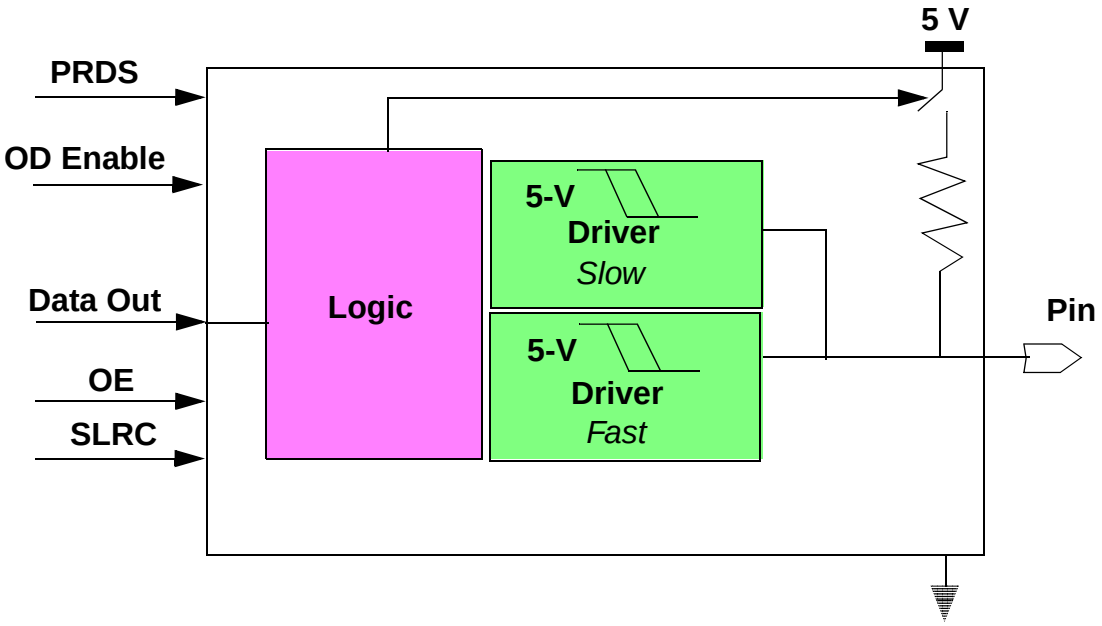


Figure 2-24 Type Q Interface

2.5.9.2 Type R Interface

This is a 5-V input-only pad with a synchronous and asynchronous receiver. Both synchronous and asynchronous data are driven in from the internal module that interfaces to this pad. A pull-up device can be controlled using the PRDS signal.

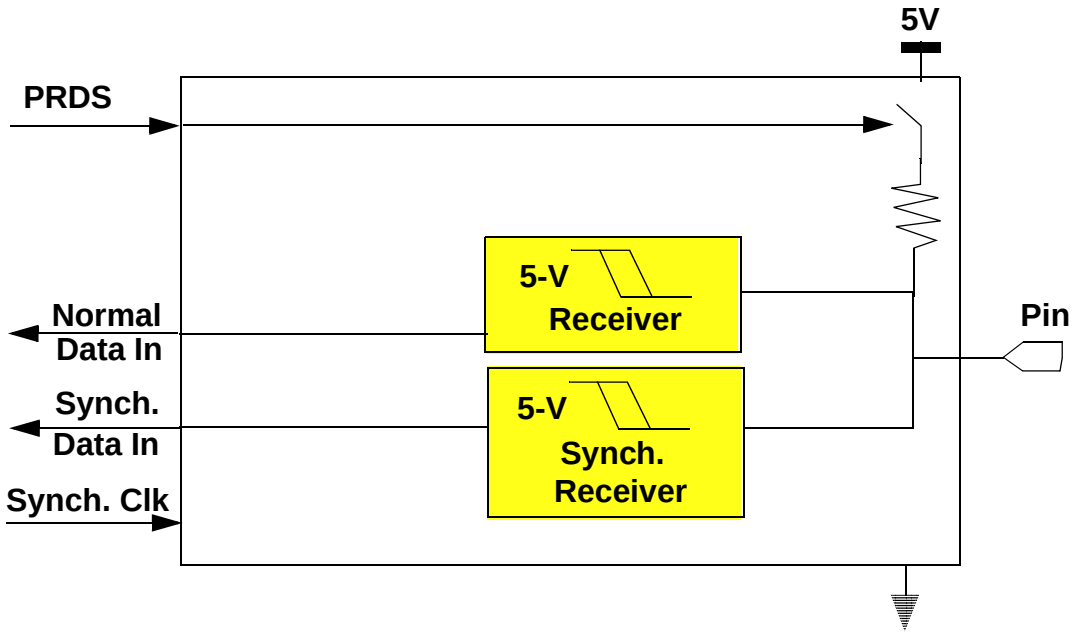


Figure 2-25 Type R Interface

2.5.9.3 5V Output for Clock Pad

This interface is used for a 5-V clock pad output. The drive select signal selects the buffer for a 45- or 90-pF load.

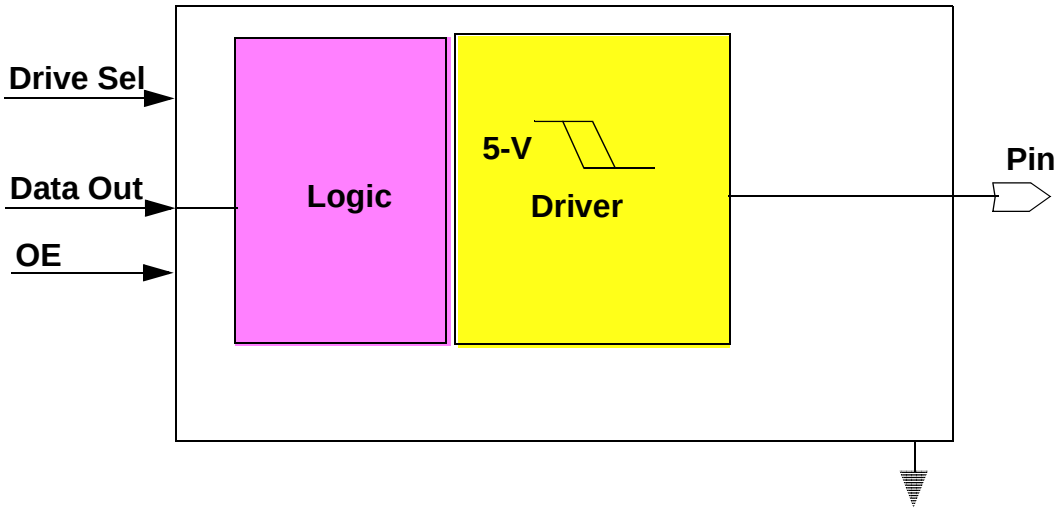


Figure 2-26 Type S Interface

2.6 Pad Groups

A pad group is a set of pins that exhibits similar functional characteristics. Within a group the individual pads may be of different types. The functionality of some pins is defined based on the control bits that are set in the SIUMCR from the reset configuration word. Refer to the section on pin functionality out of reset in the reset section of the document.

The following is a list of pad groups which were obtained based on the 3-V / 5-V selection from the information in the “pin configuration out of reset” tables. In other words, each group receives a different encoded 3-V / 5-V select signal.

Table 2-5 Pad Groups Based on 3-V / 5-V Select

Group	Pins
1	FRZ/PTR/SGPIOC[6], SGPIO[7]/$\overline{\text{IRQOUT}}$/LWP[0]
2	DATA[0:31]/SGPIOD[0:31]
3	ADDR[8:31]/SGPIOA[8:31]
4	$\overline{\text{IRQ[0]}}$/SGPIOC[0], $\overline{\text{IRQ[1]}}$/SGPIOC[1], $\overline{\text{IRQ[4]}}$/SGPIOC[4]
5	$\overline{\text{IRQ[2]}}$/SGPIOC[2], $\overline{\text{IRQ[3]}}$/SGPIOC[3], $\overline{\text{IRQ[5]}}$/SGPIOC[5]

All pins that drive 3 V have the provision to choose between drive strengths for a 25-pF load or a 50-pF load.

2.7 Pin Names and Abbreviations

The following table lists the recommended abbreviations for all the pins on the MPC555. The abbreviations can be used in applications for which the actual name is too long. For example, they can be used to on circuit boards to map the pin location on the boards.

Table 2-6 Pin Names and Abbreviations

Pin List	Pin Name	Abbreviation	Ball
ADDR[8:31]/SGPIOA[8:31]	addr_sgpioa[8]	addr_sgp[8]	V6
	addr_sgpioa[9]	addr_sgp[9]	V5
	addr_sgpioa[10]	addr_sgp[10]	V4
	addr_sgpioa[11]	addr_sgp[11]	V3
	addr_sgpioa[12]	addr_sgp[12]	W1
	addr_sgpioa[13]	addr_sgp[13]	Y2
	addr_sgpioa[14]	addr_sgp[14]	W3
	addr_sgpioa[15]	addr_sgp[15]	Y3
	addr_sgpioa[16]	addr_sgp[16]	W4
	addr_sgpioa[17]	addr_sgp[17]	Y4
	addr_sgpioa[18]	addr_sgp[18]	W5
	addr_sgpioa[19]	addr_sgp[19]	Y5
	addr_sgpioa[20]	addr_sgp[20]	W6
	addr_sgpioa[21]	addr_sgp[21]	Y6
	addr_sgpioa[22]	addr_sgp[22]	V7
	addr_sgpioa[23]	addr_sgp[23]	W7
	addr_sgpioa[24]	addr_sgp[24]	Y7
	addr_sgpioa[25]	addr_sgp[25]	Y8
	addr_sgpioa[26]	addr_sgp[26]	W8
	addr_sgpioa[27]	addr_sgp[27]	V8
	addr_sgpioa[28]	addr_sgp[28]	U8
	addr_sgpioa[29]	addr_sgp[29]	U9
	addr_sgpioa[30]	addr_sgp[30]	U7
	addr_sgpioa[31]	addr_sgp[31]	U6

Table 2-6 Pin Names and Abbreviations (Continued)

Pin List	Pin Name	Abbreviation	Ball
DATA[0:31]/SGPIOD[0:31]	data_sgpiod[0]	data_sgp[0]	Y9
	data_sgpiod[1]	data_sgp[1]	W9
	data_sgpiod[2]	data_sgp[2]	Y10
	data_sgpiod[3]	data_sgp[3]	W10
	data_sgpiod[4]	data_sgp[4]	Y11
	data_sgpiod[5]	data_sgp[5]	W11
	data_sgpiod[6]	data_sgp[6]	Y12
	data_sgpiod[7]	data_sgp[7]	W12
	data_sgpiod[8]	data_sgp[8]	Y13
	data_sgpiod[9]	data_sgp[9]	W13
	data_sgpiod[10]	data_sgp[10]	Y14
	data_sgpiod[11]	data_sgp[11]	W14
	data_sgpiod[12]	data_sgp[12]	Y15
	data_sgpiod[13]	data_sgp[13]	W15
	data_sgpiod[14]	data_sgp[14]	Y16
	data_sgpiod[15]	data_sgp[15]	W16
	data_sgpiod[16]	data_sgp[16]	Y17
	data_sgpiod[17]	data_sgp[17]	W17
	data_sgpiod[18]	data_sgp[18]	V17
	data_sgpiod[19]	data_sgp[19]	V16
	data_sgpiod[20]	data_sgp[20]	U16
	data_sgpiod[21]	data_sgp[21]	V15
	data_sgpiod[22]	data_sgp[22]	V14
	data_sgpiod[23]	data_sgp[23]	U14
	data_sgpiod[24]	data_sgp[24]	V13
	data_sgpiod[25]	data_sgp[25]	U13
	data_sgpiod[26]	data_sgp[26]	V12
	data_sgpiod[27]	data_sgp[27]	U12
	data_sgpiod[28]	data_sgp[28]	V11
	data_sgpiod[29]	data_sgp[29]	U11
	data_sgpiod[30]	data_sgp[30]	V10
	data_sgpiod[31]	data_sgp[31]	V9
$\overline{\text{IRQ[0]}}$/SGPIOC[0]	irq0_b_sgpioc0	irq0b_sgp	M1
$\overline{\text{IRQ[1]}}$/$\overline{\text{RSV}}$/SGPIOC[1]	irq1_b_rsv_b_sgpioc1	irq1b_sgp	M2
$\overline{\text{IRQ[2]}}$/CR/SGPIOC[2]/$\overline{\text{MTS}}$	irq2_b_cr_b_sgpioc2_mts	irq2b_sgp	M3
$\overline{\text{IRQ[3]}}$/$\overline{\text{KR}}$, $\overline{\text{RETRY}}$/SGPIOC[3]	irq3_b_kr_b_retry_b_sgpioc3	irq3b_sgp	L3
$\overline{\text{IRQ[4]}}$/AT[2]/SGPIOC[4]	irq4_b_at2_sgpioc4	irq4b_sgp	L4
$\overline{\text{IRQ[5]}}$/SGPIOC[5]/MODCK[1]	irq5_b_sgpioc5_modck1	irq5b_sgp	W18
$\overline{\text{IRQ[6:7]}}$/MODCK[2:3]	irq6_b_modck2	irq6b_mck2	Y18
	irq7_b_modck3	irq7b_mck3	Y19
TSIZ[0:1]	tsiz0	tsiz0	U1
	tsiz1	tsiz1	T3

Table 2-6 Pin Names and Abbreviations (Continued)

Pin List	Pin Name	Abbreviation	Ball
RD/ $\overline{WR}$	rd_wr_b	rd_wrb	R1
$\overline{BURST}$	burst_b	burstb	V1
$\overline{BDIP}$	bdip_b	bdipb	U4
$\overline{TS}$	ts_b	tsb	U3
$\overline{TA}$	ta_b	tab	U2
$\overline{TEA}$	tea_b	teab	T2
$\overline{RSTCONF}$/TEXP	rstconf_b_texp	rcfb_txp	U17
$\overline{OE}$	oe_b	oeb	T1
$\overline{BI}$/$\overline{STS}$	bi_b_sts_b	bib_stsb	V2
$\overline{CS[0:3]}$	cs0_b	cs0b	P4
	cs1_b	cs1b	R4
	cs2_b	cs2b	R3
	cs3_b	cs3b	R2
$\overline{WE[0:3]}$/$\overline{BE[0:3]}$/AT[0:3]	we_b_be_b_at[0]	web_at[0]	N1
	we_b_be_b_at[1]	web_at[1]	P1
	we_b_be_b_at[2]	web_at[2]	P2
	we_b_be_b_at[3]	web_at[3]	P3
$\overline{PORESET}$	poreset_b	poresetb	V19
$\overline{HRESET}$	hreset_b	hresetb	W20
$\overline{SRESET}$	sreset_b	sresetb	V20
SGPIOC[6]/FRZ/$\overline{PTR}$/	sgpioc6_frz_ptr_b	sgp_frz	K3
SGPIOC[7]/$\overline{IRQOUT}$/LWP[0]	sgpioc7_irqout_b_lwp0	sgp_irqoutb	M4
$\overline{BG}$/VF[0]/LWP[1]	bg_b_vf0_lwp1	bgb_lwp1	N3
$\overline{BR}$/VF[1]/IWP[2]	br_b_vf1_iwp2	brb_iwp2	N2
$\overline{BB}$/VF[2]/IWP[3]	bb_b_vf2_iwp3	bbb_iwp3	N4
IWP[0:1]/VFLS[0:1]	iwp0_vfls0	iwp0_vfls	L2
	iwp1_vfls1	iwp1_vfls	L1
TMS	tms	tms	K1
TDI/DSDI	tdi_dsdi	tdi_dsdi	K2
TCK/DSCK	tck_dsck	tck_dsck	J1
TDO/DSDO	tdo_dsdo	tdo_dsdo	J2
$\overline{TRST}$	trst_b	trst_b	J3
XTAL	xtal	xtal	U20
EXTAL	extal	extal	T20
XFC	xfc	xfc	R19
CLKOUT	clkout	clkout	V18
EXTCLK	extclk	extclk	U18
VDDSYN	vddsyn	vddsyn	R20
VSSSYN	vsssyn	vsssyn	T19
ENGCLK/BUCLK	engclk_buclk	eck_buck	U19

Table 2-6 Pin Names and Abbreviations (Continued)

Pin List	Pin Name	Abbreviation	Ball
QSMCM			
PCS0/$\overline{SS}$/QGPIO[0]	pcs0_ss_b_qgpio0	pcs0_qgp	L18
PCS[1:3]/QGPIO[1:3]	pcs1_qgpio1	pcs1_qgp	L17
	pcs2_qgpio2	pcs2_qgp	M18
	pcs3_qgpio3	pcs3_qgp	M17
MISO/QGPIO[4]	miso_qgpio4	miso_qgp4	L19
MOSI/QGPIO[5]	mosi_qgpio5	mosi_qgp5	L20
SCK/QGPIO[6]	sck_qgpio6	sck_qgp6	M20
TXD[1:2]/QGPO[1:2]	txd1_qgpo1	txd1_qgpo	N18
	txd2_qgpo2	txd2_qgpo	N20
RXD[1:2]/QGPI[1:2]	rxd1_qgpi1	rxd1_qgpi	N17
	rxd2_qgpi2	rxd2_qgpi	N19
ECK	eck	eck	M19
MIOS			
MDA[11:15]	mda11	mda11	A17
	mda12	mda12	A18
	mda13	mda13	A19
	mda14	mda14	B17
	mda15	mda15	B18
MDA[27:31]	mda27	mda27	C17
	mda28	mda28	B20
	mda29	mda29	C18
	mda30	mda30	C19
	mda31	mda31	C20
MPWM[0:3], [16:19]	mpwm0	mpwm0	E17
	mpwm1	mpwm1	D18
	mpwm2	mpwm2	D19
	mpwm3	mpwm3	D20
	mpwm16	mpwm16	F17
	mpwm17	mpwm17	E18
	mpwm18	mpwm18	F18
	mpwm19	mpwm19	E19
VF[0:2]/MPIO32B[0:2]	vf0_mpio32b0	vf0_mpio0	J19
	vf1_mpio32b1	vf1_mpio1	J20
	vf2_mpio32b2	vf2_mpio2	J17
VFLS[0:1]/MPIO32B[3:4]	vfls0_mpio32b3	vfls0_mpio3	J18
	vfls1_mpio32b4	vfls1_mpio4	K18

Table 2-6 Pin Names and Abbreviations (Continued)

Pin List	Pin Name	Abbreviation	Ball
MPIO32B[5:15]	mpio32b5	mpio5	G17
	mpio32b6	mpio6	E20
	mpio32b7	mpio7	F19
	mpio32b8	mpio8	G18
	mpio32b9	mpio9	F20
	mpio32b10	mpio10	H17
	mpio32b11	mpio11	G19
	mpio32b12	mpio12	G20
	mpio32b13	mpio13	H20
	mpio32b14	mpio14	H19
	mpio32b15	mpio15	H18
TPU_A/TPU_B			
A: TPUCH[0:15]	a_tpuch0	a_tpuch0	D3
	a_tpuch1	a_tpuch1	A2
	a_tpuch2	a_tpuch2	D4
	a_tpuch3	a_tpuch3	C3
	a_tpuch4	a_tpuch4	A3
	a_tpuch5	a_tpuch5	D5
	a_tpuch6	a_tpuch6	B3
	a_tpuch7	a_tpuch7	C4
	a_tpuch8	a_tpuch8	A4
	a_tpuch9	a_tpuch9	C5
	a_tpuch10	a_tpuch10	B4
	a_tpuch11	a_tpuch11	B5
	a_tpuch12	a_tpuch12	A5
	a_tpuch13	a_tpuch13	C6
	a_tpuch14	a_tpuch14	B6
	a_tpuch15	a_tpuch15	A6
A: T2CLK	a_t2clk	a_t2clk	C2

Table 2-6 Pin Names and Abbreviations (Continued)

Pin List	Pin Name	Abbreviation	Ball
B: TPUCH[0:15]	b_tpuch0	b_tpuch0	H2
	b_tpuch1	b_tpuch1	H1
	b_tpuch2	b_tpuch2	G1
	b_tpuch3	b_tpuch3	G2
	b_tpuch4	b_tpuch4	G3
	b_tpuch5	b_tpuch5	F1
	b_tpuch6	b_tpuch6	F2
	b_tpuch7	b_tpuch7	E1
	b_tpuch8	b_tpuch8	F3
	b_tpuch9	b_tpuch9	G4
	b_tpuch10	b_tpuch10	E2
	b_tpuch11	b_tpuch11	D1
	b_tpuch12	b_tpuch12	F4
	b_tpuch13	b_tpuch13	D2
	b_tpuch14	b_tpuch14	E3
	b_tpuch15	b_tpuch15	C1
B: T2CLK	b_t2clk	b_t2clk	B1
QADC_A/QADC_B			
ETRIG[1:2]	etrig1	etrig1	C16
	etrig2	etrig2	B16
A: AN0/ANW/PQB0	a_an0_anw_pqb0	aan0_pqb0	A8
A: AN1/ANX/PQB1	a_an1_anx_pqb1	aan1_pqb1	D8
A: AN2/ANY/PQB2	a_an2_any_pqb2	aan2_pqb2	C8
A: AN3/ANZ/PQB3	a_an3_anz_pqb3	aan3_pqb3	B8
A: AN[48:51]/PQB[4:7]	a_an48_pqb4	aan48_pqb4	A9
	a_an49_pqb5	aan49_pqb5	B9
	a_an50_pqb6	aan50_pqb6	D9
	a_an51_pqb7	aan51_pqb7	C9
A: AN[52:54]/MA[0:2]/PQA[0:2]	a_an52_ma0_pqa0	aan52_pqa0	A10
	a_an53_ma1_pqa1	aan53_pqa1	B10
	a_an54_ma2_pqa2	aan54_pqa2	A11
A: AN[55:56]]/PQA[3:4]	a_an55_pqa3	aan55_pqa3	D10
	a_an56_pqa4	aan56_pqa4	C10
A: AN[57:59]/PQA[5:7]	a_an57_pqa5	aan57_pqa5	B11
	a_an58_pqa6	aan58_pqa6	D11
	a_an59_pqa7	aan59_pqa7	C11
B: AN0/ANW/PQB0	b_an0_anw_pqb0	ban0_pqb0	A12
B: AN1/ANX/PQB1	b_an1_anx_pqb1	ban1_pqb1	B12
B: AN2/ANY/PQB2	b_an2_any_pqb2	ban2_pqb2	A13
B: AN3/ANZ/PQB3	b_an3_anz_pqb3	ban3_pqb3	A14

Table 2-6 Pin Names and Abbreviations (Continued)

Pin List	Pin Name	Abbreviation	Ball
B: AN[48:51]/PQB[4:7]	b_an48_pqb4	ban48_pqb4	B13
	b_an49_pqb5	ban49_pqb5	C12
	b_an50_pqb6	ban50_pqb6	D12
	b_an51_pqb7	ban51_pqb7	A15
B: AN[52:54]/MA[0:2]/PQA[0:2]	b_an52_ma0_pqa0	ban52_pqa0	B14
	b_an53_ma1_pqa1	ban53_pqa1	C13
	b_an54_ma2_pqa2	ban54_pqa2	B15
B: AN[55:56]/PQA[3:4]	b_an55_pqa3	ban55_pqa3	D13
	b_an56_pqa4	ban56_pqa4	C14
B: AN[57:59]/PQA[5:7]	b_an57_pqa5	ban57_pqa5	C15
	b_an58_pqa6	ban58_pqa6	D14
	b_an59_pqa7	ban59_pqa7	D15
VRH	vrh	vrh	B7
VRL	vrl	vrl	A7
VDDA	vdda	vdda	C7
VSSA	vssa	vssa	D7
TOUCAN_A/TOUCAN_B			
A: CNTX0	a_cntx0	a_cntx0	K19
B: CNTX0	b_cntx0	b_cntx0	H4
A: CNRX0	a_cnrx0	a_cnrx0	K20
B: CNRX0	b_cnrx0	b_cnrx0	H3
CMF			
EPEE	epee	epee	P18
VPP	vpp	vpp	P17
VDDF	vddf	vddf	R18
VSSF	vssf	vssf	P19
Global Power Supplies			
VDDL	vddl	vddl	D17, E4, K4, K17, R17. T4, U10, U15
VDDH	vddh	vddh	A1, A16, A20, B2, B19, P20, Y1, Y20, W2, W19
VDDI	vddi	vddi	T17, U5, D6, D16
KAPWR	kapwr	kapwr	T18
VDDSRAM	vddsram	vddsram	J4
VSS	vss	vss	J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12