SECTION 4
BURST BUFFER

The burst buffer module consists of the burst buffer controller (BBC) and the instruction memory protection unit (IMPU).

The BBC delivers the RCPU instruction fetch accesses from the instruction bus onto the U-bus. It utilizes the full U-bus pipeline and a special page access attribute in order to take full advantage of the U-bus bandwidth. It can handle both burstable and non-burstable external memories as well as non-burstable internal memories (flash EEPROM, SRAM).

The IMPU allows the memory to be divided into four regions with different attributes, as well as a default global region (for memory space that is not included in either of the two regions). Each of the two regions can be of size 4 Kbytes to 4 Gbytes. Overlap between regions is allowed.

The IMPU includes registers that contain the following information: region base address, region size and the region's access permissions. For each access (from the processor to the memory), the IMPU finds which region matches the address. If more than one region matches, the region with the lowest index is chosen. If no region is matched, the global region is chosen.

The IMPU compares the attributes of the access from the processor to the attributes of the appropriate region. If the access is allowed, the proper signals are sent to the BBC. If the access is not permitted, an interrupt is sent to the processor.

The IMPU does not support address translation. The effective fetch address issued by the processor is the one that is transferred to the U-bus.

4.1 Burst Buffer Block Diagram

Figure 4-1 is a block diagram of the burst buffer.

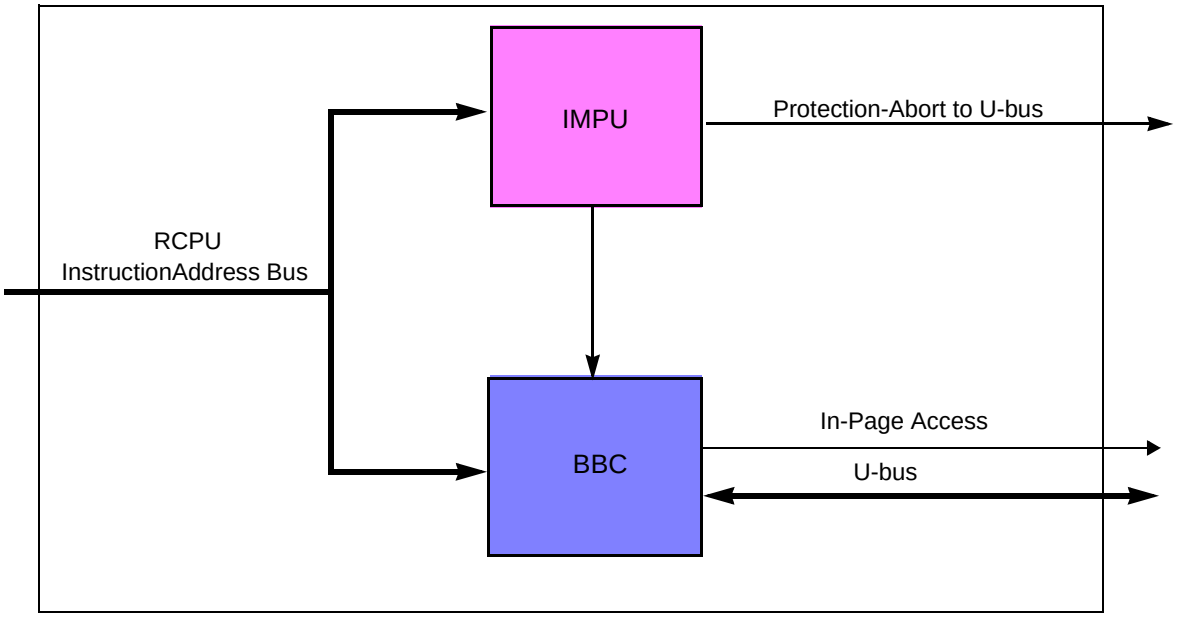

Figure 4-1 Burst Buffer Block Diagram

4.2 Burst Buffer Features

The BBC offers the following features:

- Supports pipelined access to internal memory and burstable access to the external memory.
- Supports the de-coupled interface with the RCPU instruction unit.
- Serves as parked master on the U-bus, resulting in zero clocks delay for RCPU fetch access to cross to the U-bus.
- Full utilization of the U-bus pipeline for fetch accesses.
- Tightly interfaced with L2U Interface module, taking advantage of full U-bus bandwidth and back-to-back accesses.
- Supports program trace and show cycle attributes.
- Supports special attribute for debug port fetch accesses.
- Is programmed using the MPC555 **mtspr/mfspr** instructions to/from implementation specific special-purpose registers.
- Designed for minimum power consumption.

The IMPU has the following features:

- Four regions in which the base address and size can be programmed.
- Region sizes of 4 Kbytes up to 4 Gbytes (in powers of two) can be programmed. (A region must start on the specified region size boundary.)
- Overlap between regions is allowed.
- Each of the four regions supports the following attributes:
  — Access protection (user/supervisor fetch or no access).
  — Guarded attribute (causes an interrupt in case of fetch try).

— On/off option
- Global region entry declares the default access protection and guarded attributes for all memory areas not covered by the four regions:
- Interrupt generated upon access violation or fetch from guarded region.
- MPC555 MSR[IR] bit controls MPU protection.
- Programming is done using MPC555 **mtspr/mfspr** instructions to/from implementation specific special purpose registers.
- Designed for minimum power consumption.

4.3 Little-Endian Support

The BBC supports little-endian operation only when bursts are disabled (see **4.6.4 BBC Module Configuration Register (BBCMCR)** for more details. The BBC does not support little-endian in the following cases:

1. For internal code/data memories

4.4 Modes Of Operation

The burst buffer module can operate in the following modes:

- Normal
- Slave
- Reset
- Debug
- Standby
- Burst

The modes of operation are described in the following paragraphs.

4.4.1 Normal Operation

During normal operation, the burst buffer module transfers fetch accesses from the CPU to the U-bus. When a new access is issued by the CPU, it is transferred in parallel to both the IMPU and the BBC. The IMPU compares the address of the access to its region programming. The BBC determines whether the access can be immediately transferred to the U-bus. If not, it requests the U-bus for the next clock.

Each new BBC U-bus access is accompanying by the burst request attribute. If burstable access is enabled, the BBC performs a burst access; otherwise, it performs a single access.

If the IMPU detects an access violation, it does the following:

- Cancels the request that was forwarded to the BBC
- Informs the RCPU core that the requested address generated an exception

If the required address contains show cycle or program trace attributes, the BBC delivers the access to the U-bus even if the request is cancelled (due to the exception it caused).

The BBC forwards show cycle, program trace and debug port access attributes accompanying the CPU access along with the U-bus access.

4.4.2 Slave Operation.

The burst buffer module is operating as a U-bus slave module when the instruction memory protection unit (IMPU) registers are accessed by the user in order to be programmed. This programming is done using the **mtspr /mfspr** instructions.

4.4.3 Reset Operation

On reset the BBC goes to an idle state, and all pending U-bus accesses are ignored. The IMPU goes to a disabled state in which all memory space is accessible to both user and supervisor.

4.4.4 Debug Mode Operation

When the CPU is in debug mode, fetch accesses are attached with a special attribute. If this attribute is asserted, the BBC must initiate not-burstable accesses to the debug port.

4.4.5 Standby Mode Operation

In this low-power modes the CPU stops issuing further accesses. The BBC clocks are turned off, and the BBC enters a power save state. When the low-power mode is exited, clocks are activated and a new access from the CPU will activate the BBC.

4.4.6 Burst Operation

The BBC can run burst accesses on the U-bus. Such burst cycles, if forwarded to external memory, are then exported to the EBI as burst cycles (if bursts are enabled by the USIU).

The BE bit defined in **4.6.4 BBC Module Configuration Register (BBCMCR)** determines whether the BBC operates burst cycles or not. Burst requests are enabled only when the BE bit is set.

NOTE

The negated state of the BE bit is useful mainly when the RCPU core runs in serialized mode.

4.4.7 Error Detection.

If the IMPU detects access violation, the following actions must be taken:

1. Cancel the request that was forwarded to the burst buffer controller
2. Inform the RCPU core that the requested address generated an exception

If the required address contains show cycle or program trace attributes, than the BBC delivers the access onto the U-bus even if the request is cancelled (due to the exception it caused).

The way the IMPU notifies the RCPU core for an interrupt is by feeding error information into four bits (1, 3, 4 and 10) in the SRR1 regsiter in the core. Only one bit is set at a time. The exception vector (address) that the core issues for this event is 0xnnn0-1300. The encoding of the status bits is as follows:

- SRR1 = 0
- SRR3 = Gaurded storage.
- SRR4 = Protected storage.
- SRR10 = 0

4.5 Exception Table Relocation

The BBC has the ability to relocate the exception table. Exception table relocation is a feature to save memory space in the exception table. This is done by mapping exceptions to be separated by 8 bytes instead of 256 bytes (see **Table 4-1**). The relocation feature only maps the exception table into the internal memory space of the MPC555, which requries MSR[IP] = 1. This feature is important in multi-MPC555 systems, where more than one MCU can have internal exception tables with the same exception addresses issued by the RCPU.

The relocation feature also saves the wasted space between exception table entries when each exception entry contains only a branch instruction to the exception routine, which is located elsewhere.

If exception relocation is enabled (ETRE bit is set in the BBCMCR), all exception routines (except the reset exception routine) can be controlled to either remain in the lower addresses of the memory (base address + exception offset) or to be relocated to memory (base address + 32 Kbytes). The reset exception routine location is fixed in memory (base address + the reset exception offset) and can not be relocated.

See **4.6.4 BBC Module Configuration Register (BBCMCR)** for programming details.

4.5.1 Exception Table Relocation Operation

When an exception is requested, the CPU initiates a fetch cycle that branches to the exception routine associated with the exception that caused the fetch. The exception addresses are fixed within the RCPU architecture and are 0x100 bytes apart from each other, starting at address 0x0000_0100 or 0xFFF0_0100, depending on the value of the MSR[IP] bit.

If the relocation feature is disabled, the BBC transfers the exception fetch address to the internal bus of the MPC555 with no interference.

In order to activate exception table relocation, the following steps are required:

1. Set the MSR[IP] bit. To set this bit out of reset, set the appropriate bit in the reset configuration word.
2. Set the ETRE bit in BBCMCR register. See **4.6.4 BBC Module Configuration Register (BBCMCR)** for programming details.

If the relocation feature is enabled, the BBC translates the starting address of the exception routine into the address located at the lowest portion of the internal memory. At that location, the user must insert a series (table) of consecutive branch instructions that point to the appropriate exception routines. Thus, the CPU branches twice to reach the appropriate exception routine.

NOTE

The 8 Kbytes allocated for the exception table can be almost fully utilized. This is possible if the MPC555's address space is *not* mapped to the exception address space — that is, if addresses 0xFFF0_0000 to 0xFFF0_1FFF are not part of the MPC555 address apace. In this case, these 8 Kbytes can be fully utilized by the compiler, except for the lower 64 words (256 bytes), which are reserved for the exception pointers.

NOTE

That if the CPU issues any address that falls between two successive exception entries (e.g., 0xFFF0_0104), then an exception is generated to the CPU if exception relocation is enabled. See **4.6.4 BBC Module Configuration Register (BBCMCR)**.

Table 4-1 Exception Addresses Mapping by BBC

Name of Exception	Address Issued by CPU (20 LSBs)[1]	Mapped Address by Exception Table Relocation Logic	
		BBCMCR[OERC] = 0[2]	BBCMCR[OERC] = 1
Reserved	0x0_0000	0x0000	0x8000
System Reset	0x0_0100	0x0008	0x0008[3]
Machine Check	0x0_0200	0x0010	0x8010
Data Storage	0x0_0300	0x0018	0x8018
Instruction Storage	0x0_0400	0x0020	0x8020
External Interrupt	0x0_0500	0x0028	0x8028
Alignment	0x0_0600	0x0030	0x8030
Program	0x0_0700	0x0038	0x8038
Floating Point unavailable	0x0_0800	0x0040	0x8040
Decrementer	0x0_0900	0x0048	0x8048
Reserved	0x0_0A00	0x0050	0x8050
Reserved	0x0_0B00	0x0058	0x8058
System Call	0x0_0C00	0x0060	0x8060
Trace	0x0_0D00	0x0068	0x8068
Floating Point Assist	0x0_0E00	0x0070	0x8070
Implementation Dependant Software Emulation	0x0_1000	0x0080	0x8080
Implementation Dependant Storage Error	0x0_1300	0x0098	0x8098
Implementation Dependant Data Breakpoint	0x0_1C00	0x00E0	0x80E0

Table 4-1 Exception Addresses Mapping by BBC

Name of Exception	Address Issued by CPU (20 LSBs)[1]	Mapped Address by Exception Table Relocation Logic	
		BBCMCR[OERC] = 0[2]	BBCMCR[OERC] = 1
Implementation Dependant Instruction Breakpoint	0x0_1D00	0x00E8	0x80E8
Implementation Dependant Maskable External Breakpoint	0x0_1E00	0x00F0	0x80F0
Non-Maskable External Breakpoint	0x0_1F00	0x00F8	0x80F8

NOTES:

1. Assuming 12 MSBs = 0xFFF0, which is set by MSR[IP] = 1.
2. OERC bit; See **4.6.4 BBC Module Configuration Register (BBCMCR)**.
3. The reset exception is NOT affected by OERC.

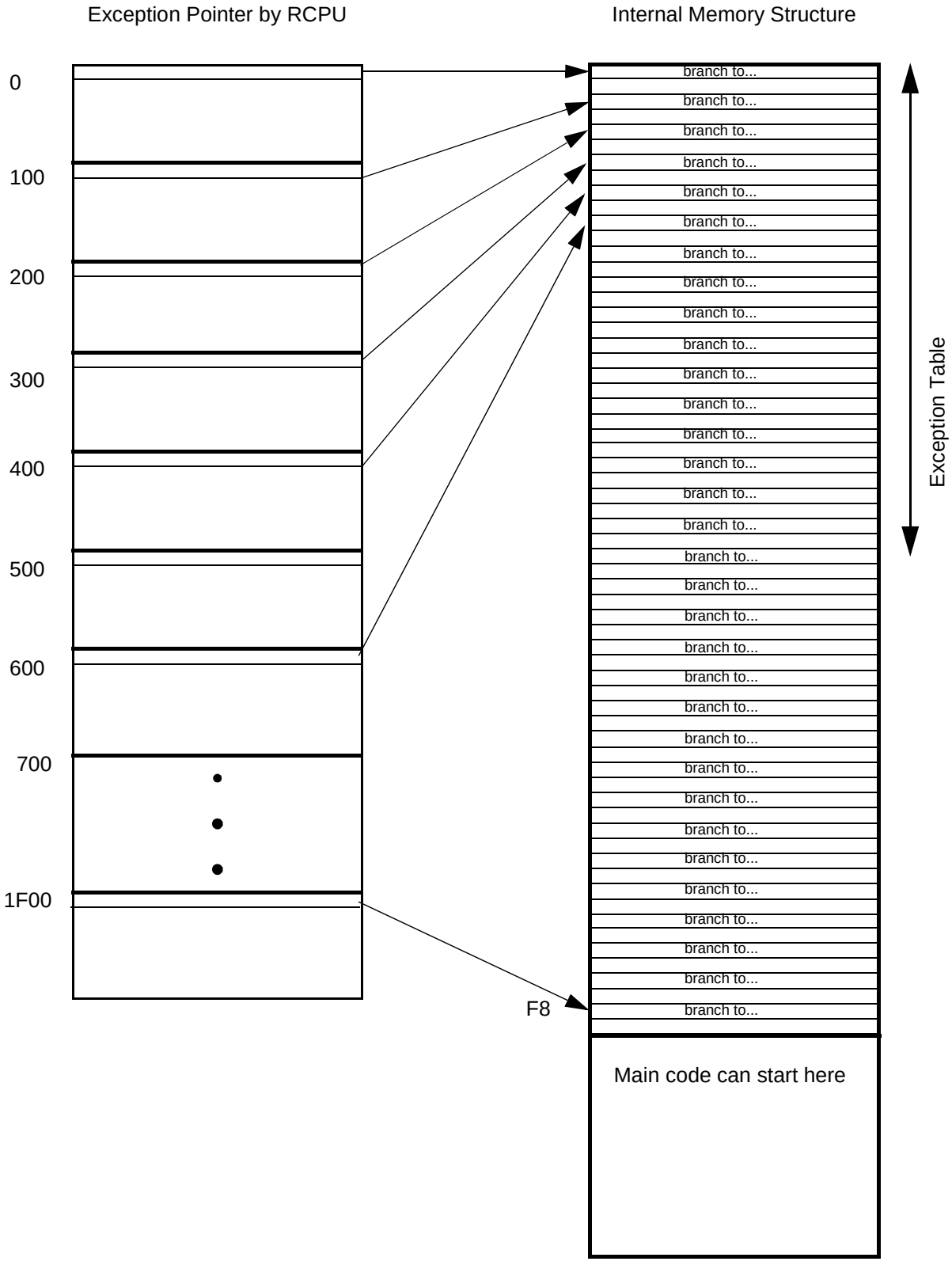

Figure 4-2 Exception Table Entries Mapping

4.6 Burst Buffer Programming Model

The BBC and IMPU module configuration registers are MPC555 special-purpose registers (SPRs). They are programmed with the MPC555 **mtspr/mfspr** instructions.

All the registers can be accessed in supervisor mode only. The processor generates an exception internally if an attempt is made to access the registers from user mode.

The following 32-bit registers contain the starting address and the size of the region. There is one register for each region.

Table 4-2 Region Base Address Registers RBA[0:1]

Register Name	Address (Decimal)	ub_addr[18:27] (hex)
MI_RBA0	784	0x2180
MI_RBA1	785	0x2380
MI_RBA2	786	0x2580
MI_RBA3	787	0x2780

The following registers hold the attributes of the corresponding regions and of the default region. Each of the four MI_RAx registers contains access permission attributes. The MI_GRA (global region attribute) register contains two additional bits to enable each of the MI_RBAx registers.

Table 4-3 Region Attributes Registers

Register Name	Address (Decimal)	ub_addr [18:27] (Hex)
MI_RA0	816	0x2190
MI_RA1	817	0x2390
MI_RA2	818	0x2590
MI_RA3	818	0x2790
MI_GRA	528	0x2100

The BBC holds only one register, the BBC module configuration register (BBCMCR).

Table 4-4 BBC Module Configuration Register

Register name	Addr (Decimal)	ub_addr [0:31] (Hex)
BBCMCR	560	0x2110

4.6.1 Region Base Address Registers

MI_RBA[0:3] — Region Base Address Register **SPR 784 – 787**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RA															
RESET:															
Unaffected by Reset															

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
RA				Reserved											
RESET:															
Unaffected by Reset															

Table 4-5 MI_RBA[0:3] Bit Settings

Bit(s)	Name	Description
0:19	RA	Region address. This field defines the base address (most significant 20 bits) for the region.
20:31	—	Reserved

4.6.2 Region Attribute Registers MI_RA[0:3] Description

MI_RA[0:3] – Region Attribute Registers **SPR 816 – 819**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RS															
RESET:															
Unaffected by Reset															

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
RS				PP		RESERVED			G	RESERVED					
RESET:															
Unaffected by Reset															

Table 4-6 MI_RA[0:3] Bit Settings

Bit(s)	Name	Description
0:19	RS	Region size. The region size is a power of two, determined as follows: 0000_0000_0000_0000_0000 — 4 Kbytes 0000_0000_0000_0000_0001 — 8 Kbytes 0000_0000_0000_0000_0011 — 16 Kbytes 0000_0000_0000_0000_0111 — 32 Kbytes 0000_0000_0000_0000_1111 — 64 Kbytes 0000_0000_0000_0001_1111 — 128 Kbytes 0000_0000_0000_0011_1111 — 256 Kbytes 0000_0000_0000_0111_1111 — 512 Kbytes 0000_0000_0000_1111_1111 — 1 Mbyte 0000_0000_0001_1111_1111 — 2 Mbytes 0000_0000_0011_1111_1111 — 4 Mbytes 0000_0000_0111_1111_1111 — 8 Mbytes 0000_0000_1111_1111_1111 — 16 Mbytes 0000_0001_1111_1111_1111 — 32 Mbytes 0000_0011_1111_1111_1111 — 64 Mbytes 0000_0111_1111_1111_1111 — 128 Mbytes 0000_1111_1111_1111_1111 — 256 Mbytes 0001_1111_1111_1111_1111 — 512 Mbytes 0011_1111_1111_1111_1111 — 1 Gbyte 0111_1111_1111_1111_1111 — 2 Gbytes 1111_1111_1111_1111_1111 — 4 Gbytes
20:21	PP	Protection bits 00 = No supervisor access, no user access 01 = Supervisor fetch access, no user access 10 = Supervisor fetch access, user fetch access 11 = Supervisor fetch access, user fetch access
22:24	—	Reserved
25	G	Guarded attribute for region 0 = Fetch is allowed from guarded region. 1 = Fetch is prohibited from guarded region. An attempted fetch will generate an exception.
26:31	—	Reserved

4.6.3 Global Region Attribute Register Description (MI_GRA)

MI_GRA — Global Region Attribute Register **SPR 528**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ENR0	ENR1	ENR2	ENR3	RESERVED											
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
RESERVED				PP		RESERVED			G	RESERVED					
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-7 MI_GRA Bit Settings

Bit(s)	Name	Description
0	ENR0	Enable region 0 of IMPU 0 = Region 0 is off 1 = Region 0 is on
1	ENR1	Enable region 1 of IMPU 0 = Region 1 is off 1 = Region 1 is on
2	ENR2	Enable region 2 of IMPU 0 = Region 2 is off 1 = Region 2 is on
3	ENR3	Enable region 3 of IMPU 0 = Region 3 is off 1 = Region 3 is on
4:19	—	Reserved
20:21	PP	Protection bits 00 = No supervisor access, no user access 01 = Supervisor fetch access, no user access 10 = Supervisor fetch access, user fetch access 11 = Supervisor fetch access, user fetch access
22:24	—	Reserved
25	G	Guarded attribute for region 0 = Fetch is allowed from guarded region. 1 = Fetch is prohibited from guarded region. An attempted fetch will generate an exception.
26:31	—	Reserved

4.6.4 BBC Module Configuration Register (BBCMCR)

BBCMCR — BBC Module Configuration Register **SPR 560**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Reserved															
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	LSB 31
Reserved		BE	ETRE	OERC	Reserved										
RESET:															
0	0	0	ID[19]*	0	0	0	0	0	0	0	0	0	0	0	0

* Reset value is taken from the indicated bit of the reset configuration word.

Table 4-8 BBCMCR Bit Settings

Bit(s)	Name	Description
16:17	—	Reserved
18	BE	Burst enable 0 = BBC does not request burst accesses 1 = BBC requests burst accesses
19	ETRE	Exception table relocation enable 0 = Exception table relocation is off — the BBC does *not* map exception addresses 1 = Exception table relocation is on — the BBC maps exception addresses to a branch instruction table. Refer to **4.5 Exception Table Relocation**.
20	OERC	Other exceptions relocation control. 0 = All exceptions except reset are mapped to the internal memory base address. 1 = All exceptions except reset are mapped to the internal memory base address + 32 Kbytes.
21:31	—	Reserved