



INDEX

-A-

A(0
 31), 9-4
ACKERR 16-30
Acknowledge error (ACKERR) 16-30
Address
 -mark wakeup 14-59
 space 13-7
address type (AT0-AT3), 9-37
ALE 21-54
ALEE 21-56
alignment exception, 3-47
ALU-BFU 3-5
AN 13-3, 13-5
Analog
 front-end multiplexer 13-13
 input
 multiplexed 13-5
 port A 13-3
 port B 13-4
 section contents 13-1
 submodule block diagram 13-11
 supply pins 13-5
arbitration, 9-30
AT(0
 3), 9-4
atomic update primitives, 3-42
atomic, 9-31

-B-

BAR 3-52
Base ID mask bits 16-29
Baud
 clock 14-51
BB, 9-7
BDIP, 9-5
BE bit 3-21
Beginning of queue 2 (BQ2) 13-38
BG, 9-7
BI, 9-6
Binary
 divider 13-24
 -weighted capacitors 13-13
Bit stuff error (STUFFERR) 16-30
BITERR 16-30
BITS 14-17
Bits per transfer
 enable (BITSE) 14-23
 field (BITS) 14-17
BITSE 14-23, 14-38

Bit-time 14-50
BKPT (TPU asserted) 17-14
BLC 17-13
BOFFINT 16-31
Boundary conditions 13-16
Boundary scan
 cells 22-1
 descriptor language 22-7
 register 22-1
BPU 3-5
BQ2 13-16, 13-38
BR, 9-7
Branch
 prediction 3-5
 processing unit 3-5
 trace enable 3-21
Branch latch control (BLC) 17-13
Branch processing unit 3-5
Break frame 14-51
Breakpoint
 asserted flag (BKPT) 17-14
 flag (PCBK) 17-14
Breakpoint counter A value and control register 21-52
Breakpoint counter B value and control register 21-53
BRKNOMSK 21-51
BSC 22-1
BSR 22-1
burst indicator (BURST), 9-36
burst inhibit (BI), 9-39
burst read cycle (illustration), 9-18
burst transfer, 9-15
burst write cycle (illustration), 9-23
BURST, 9-4
Bus
 monitor 6-13
 off interrupt
 (BOFFINT) 16-31
bus busy (BB), 9-32
bus exception control cycles, 9-43
bus grant (BG), 9-31
bus interface
 bus control signals, 9-2
 bus operation
 address transfer phase related signals, 9-35
 arbitration phase, 9-30
 basic transfer protocol, 9-8
 burst mechanism, 9-16
 burst transfer, 9-15
 bus exception control cycles, 9-43
 single beat transfer
 single beat read flow, 9-8



- single beat write flow, 9-8, 9-11
- single beat transfer, 9-8
- storage reservation, 9-40
- termination signals, 9-38
- bus operations, 9-7
- bus transfer signals, 9-1
- features, 9-1
- signal descriptions, 9-3
- bus request (BR), 9-31
- bus signals (illustration), 9-3
- BUSY 16-5, 16-15
- BYP 13-12, 13-46
- Bypass mode 13-12
- BYTES field 3-18

—C—

- C bit 3-14
- CA bit 3-18
- cache control instructions, 3-43
- CAN2.0B
 - system 16-3
- CANCTRL0 16-25
- CANCTRL1 16-26
- CANCTRL2 16-28
- CANICR 16-24
- Carry 3-18
- CCL 17-13
- CCW 13-1, 13-45
- CF1 13-40
- CF2 13-40
- CFSR 17-15
- CGBMSK 21-50
- CH 17-15, 17-18, 17-19
- CHAN 13-46
- CHANNEL 17-16
- Channel
 - assignments
 - multiplexed 13-47
 - nonmultiplexed 13-47
 - conditions latch (CCL) 17-13
 - interrupt
 - enable
 - /disable field (CH) 17-15
 - request level (CIRL) 17-15
 - status (CH) 17-19
 - invalid 13-46
 - number (CHAN) 13-46
 - orthogonality 17-3
 - priority registers 17-18
 - register breakpoint flag (CHBK) 17-14
 - reserved 13-46
- CHBK 17-14
- CHBMSK 21-50
- checkstop state, 3-45
- CHSTP bit 21-54
- CHSTPE 21-55
- CIE1 13-36
- CIE2 13-38
- CIER 17-15, 17-19
- CIRL 17-15

- CISR 17-8, 17-19
- class, instruction, 3-39
- CLKOUT to TA, BI assertion (when driven by the Memory Controller) G-17
- CLKOUT, 9-7
- CLKS 17-13
- Clock
 - block diagram 13-25
 - frequency 13-25
 - generation 13-24
 - phase (CPHA) 14-17
 - polarity (CPOL) 14-17
- CMPA–CMPD 21-45
- CMPE–CMPF 21-46
- CMPG–CMPH 21-47
- CNRX/TX pins 16-2
- CNTC 21-52
- CNTV 21-52
- Code 16-4
- Coherency 13-5, 13-22, 17-4
- COMM D-17
- Command
 - RAM 14-22
 - word pointer (CWP) 13-41
- Comparator 13-14
- Comparator A–D value registers 21-45
- Comparator E–F value registers 21-46
- Comparator G–H value registers 21-47
- Compare instructions 3-17
- Compare size 21-50
- Compare type 21-48, 21-50
- Completed queue pointer (CPTQP) 14-21
- Condition register 3-15, 3-17
- CONT 14-23
- contention, 9-36
- Continue (CONT) 14-23
- Continuous transfer mode 14-15
- Control registers
 - 1 (QACR1) 13-35
 - 2 (QACR2) 13-38
- controlling termination of a bus cycle for a bus error, 9-43
- Conversion
 - command word table (CCW) 13-1, 13-14
 - cycle times 13-12
 - stages 13-44
- Count register 3-19
- COUNTA 21-52
- COUNTB 21-53
- CPHA 14-17, 14-34
- CPOL 14-17, 14-34
- CPR 17-18
- CPTQP 14-21, 14-24
- CR 3-5, 3-15, 3-19
 - and compare instructions 3-17
- CR, 9-5
- CR0 field 3-16
- CR1 field 3-16
- CRCERR 16-30
- CRWE 21-50
- CRWF 21-50



CSG 21-50
CSH 21-50
CTA 21-48
CTB 21-48
CTC 21-48
CTD 21-48
CTE 21-50
CTF 21-50
CTG 21-50
CTH 21-50
CTR 3-5
CWP 13-41
Cyclic redundancy check error (CRCERR) 16-30

-D-

D(0
 31), 9-6
D0 20-3
DAC 13-1
DAE/source instruction service register 3-22
DAR 3-22, 3-46, 3-51, 3-52
DAR, 3-46, 3-51
Data
 field for RX/TX frames (TOUCAN) 16-4
 frame 14-50
Data address register 3-22
Data space only 20-3
data storage interrupt, 3-46
DCNR 17-19
DDRQA 13-32, 13-34
DDRQS 14-9, 14-33, 14-37
Debug enable register 21-55
debug mode disable, 3-45
DEC 3-23
DECE 21-54
DECEE 21-56
Decrementer
 register 3-23
Delay
 after transfer (DT) 14-23, 14-35
 before SCK (DSCKL) 14-18
DER 21-55
Development Port
 trap enable selection 21-48
Digital
 control section
 contents 13-1, 13-14–13-28
 input
 /output port (PQA) 13-3
 port (PQB) 13-4
 to analog converter (DAC) 13-13
DIO D-37
DIS 20-3
Disable TPU2 pins field (DTPU) 17-20
Disabled mode 13-18
Discrete input/output (DIO) D-37
 parameters D-38
DIV2 17-20
DIV8 clock 17-7
Divide by two control field (DIV2) 17-20

DIW0EN 21-48
DIW1EN 21-48
DIW2EN 21-48
DIW3EN 21-48
DLW0EN 21-52
DLW1EN 21-52
Double
 -buffered 14-53, 14-57
DPI 21-55
DPTRAM 18-4
DSCK 14-23
DSCKL 14-18
DSCR 17-12
DSISR 3-22, 3-46, 3-51, 3-52
DSSR 17-14
DT 14-23
DTL 14-18
DTPU 17-20

-E-

EA 3-33
EBRK 21-55
ECR 21-53
EE bit 3-21, 3-26
Effective address 3-33
EID 3-26
EIE 3-26
eieio, 3-43
ELE bit 3-21
EMPTY 16-5
EMU 17-4, 17-11
Emulation
 control (EMU) 17-11
 support 17-4
Encoded
 one of three channel priority levels (CH) 17-18
 time function for each channel (CHANNEL) 17-16
 type of host service (CH) 17-18
Ending queue pointer (ENDQP) 14-19
End-of-
 frame (EOF) 16-16
End-of-queue condition 13-44
ENDQP 14-19, 14-24
Entry
 table bank select field (ETBANK) 17-20
EOF 16-16
EOQ 13-17
EP bit 3-21, 3-22
ERRINT 16-31
Error
 conditions 14-58
 counters 16-9
 interrupt (ERRINT) 16-31
ESTAT 16-30
ETBANK 17-20
ETRIG 13-4
Event timing 17-3
Exception cause register 21-53
Exception prefix 3-21, 3-22
Exceptions 3-34



- classes 3-34
- little endian mode 3-21
- ordered 3-34
- precise 3-35
- unordered 3-34
- vector table 3-35, 3-36
- Execution units 3-4
- Extended message format 16-1
 - frames 16-4
- External
 - digital supply pin 13-5
 - interrupt
 - disable 3-26
 - enable 3-26
 - multiplexing 13-9
 - trigger pins 13-4
 - trigger single-scan mode 13-20
- External interrupt
 - enable 3-21, 3-26
- Externally
 - multiplexed mode (MUX) 13-35
- EXTTEST 22-5
- EXTI 21-54
- EXTIE 21-56

-F-

- Fast quadrature decode TPU function (FQD) D-28
 - parameters
 - primary channel D-29
 - secondary channel D-30
- Fault confinement state (FCS) 16-10, 16-31
- FCS 16-10, 16-31
- FE 14-49, 14-58
- FE bits 3-21, 3-22
- FE flag 3-14
- features
 - bus interface, 9-1
- Fetch serialized 21-1
- FEX bit 3-14
- FG bit 3-14
- FI bit 3-14
- Final sample time 13-12
- FL bit 3-14
- Floating-point
 - available 3-21
 - condition code 3-14
 - enabled exception summary 3-14
 - equal or zero 3-14
 - exception mode 3-21, 3-22
 - exception summary 3-14
 - fraction inexact 3-14
 - fraction rounded 3-14
 - greater than or positive 3-14
 - inexact exception 3-14
 - enable 3-15
 - invalid operation exception
 - enable 3-15
 - for $x*0$ 3-14
 - for x/x 3-14
 - for $x-x$ 3-14
 - for 0/0 3-14
 - for invalid compare 3-14
 - for invalid integer convert 3-15
 - for invalid square root 3-15
 - for SNaN 3-14
 - for software request 3-15
 - summary 3-14
 - less than or negative 3-14
 - overflow exception 3-14
 - enable 3-15
 - registers 3-12
 - result class descriptor 3-14
 - result flags 3-14
 - rounding control 3-15
 - status and control register 3-12
 - underflow exception 3-14
 - unit 3-5
 - unordered or NaN 3-14
 - zero divide exception 3-14
 - enable 3-15
 - floating-point unavailable interrupt, 3-47
 - FORMERR 16-30
 - FP bit 3-21
 - FPCC bit 3-14
 - FPRF field 3-14
 - FPRs 3-12
 - FPSCK 17-20
 - FPSCR 3-12
 - FPU 3-5
 - FPUVE 21-54
 - FPUVEE 21-56
 - F_{QCLK} 13-24
 - FQD D-28
 - FQM D-10
 - FR 3-14
 - Frame 14-50
 - size 14-58
 - Frames
 - overload 16-16
 - remote 16-15
 - Framing error (FE) flag 14-49, 14-58
 - FREEZ ACK 16-16
 - FREEZE
 - assertion response (FRZ)
 - QADC 13-6, 13-32
 - QSM 14-5
 - TPU 17-13
 - FREEZE (internal signal) 13-45
 - Frequency measurement (FQM) D-10
 - parameters D-11
 - FRZ 13-7, 13-32, 16-11, 17-13
 - FRZACK 16-11
 - FU bit 3-14
 - FULL 16-5
 - Function
 - library for TPU 17-4
 - FX bit 3-14

-G-

 - General SPRs 3-25

General-purpose registers (GPRs) 3-12
Global registers 13-31

-H-

Hall effect decode (HALLD) D-19
 parameters D-20
HALLD D-19
HALT 14-20, 16-11
Halt
 acknowledge flag (HALTA) 14-21
 QSPI (HALT) 14-20
HALTA 14-21
HALTA and MODF Interrupt Enable (HMIE) 14-41
HALTA/MODF interrupt enable (HMIE) bit 14-20
Hang on T4 (HOT4) 17-13
HMIE 14-20
HOT4 17-13
HSQR 17-16
HSSR 17-17

-I-

I/O port operation 13-7
IBRK 21-55
I-bus
 watchpoint programming 21-48
I-bus support
 control register 21-47
ICTRL 21-47
ID
 Extended (IDE) field 16-5
 HIGH field 16-5
 LOW field 16-5
IDE 16-5
Identifier (ID) 16-1
 bit field 16-6
IDLE 14-48, 14-58, 16-30
Idle
 CAN status (IDLE) 16-30
 frame 14-50
 -line
 detect type (ILT) 14-46
 detected (IDLE) 14-48, 14-58
 detection process 14-58
 interrupt enable (ILIE) 14-46, 14-58
 type (ILT) bit 14-58
IEEE 1149.1-1990 standard. See JTAG
IFLAG 16-32
Ignore first match 21-48
IIFM 21-48
ILIE 14-46, 14-58
illegal and reserved instructions, 3-39
ILSCI 14-8, 14-9
ILT 14-46, 14-58
IMASK 16-32
IMB 13-1, 13-23
implementation dependent software emulation interrupt,
 3-49
implementation specific data TLB error interrupt, 3-50
implementation specific debug interrupt, 3-51

implementation specific instruction TLB error interrupt,
 3-49
IMUL-IDIV 3-5
Information processing time (IPT) 16-9
Initial sample time 13-12
Input
 sample time (IST) 13-27, 13-46
Instruction
 pipeline 3-37
 sequencer 3-3
 set summary 3-29
 timing 3-36
Instruction fetch
 show cycle control 21-1
instruction storage interrupt, 3-46
instructions
 cache control, 3-43
 storage control, 3-44
instructions, partially executed, 3-52
Integer exception register 3-17
Integer unit 3-5
Interchannel communication 17-4
Intermission 16-16
Intermodule bus (IMB) 13-1
Interrupt
 sources 13-29
Interrupt Level of SCI (ILSCI) 14-8, 14-9
Interrupts
 QADC 13-28
 TOUCAN 16-18
 TPU 17-5
interrupts, 3-44
Inter-transfer delay 14-14
invalid and preferred instructions, 3-39
Invalid channel number 13-46
IPT 16-9
 \overline{IRQ} 17-5
ISCTL 21-1
IST 13-27, 13-46
isync, 3-43
IU 3-5
IW 21-48

-J-

Joint test action group. See JTAG
JTAG 22-1
 instruction register 22-4
 non-IEEE 1149.1-1990 operation 22-7
 signals 22-1, 22-2

-K-

KR/RETRY, 9-5

-L-

LBRK 21-55
LBUF 16-27
L-bus support
 control register 1 21-49





- control register 2 21-50
- LCK 20-3
- LCTRL1 21-49
- LCTRL2 21-50
- LE bit 3-22
- Least significant bit (LSB) 13-13
- Left justified
 - signed result word table (LJSRR) 13-48
 - unsigned result word table (LJURR) 13-48
- Length of delay after transfer (DTL) 14-18
- Link register 3-18
- Little endian mode 3-22
- LJSRR 13-48
- LJURR 13-48
- Load/store unit 3-5, 3-6
- Lock
 - /release/busy mechanism 16-14
- Loop
 - mode
 - (LOOPS) 14-46
- LOOPQ 14-20
- LOOPS 14-46
- Low power stop (LPSTOP)
 - QADC 13-6
 - QSM 14-5
- Lowest buffer transmitted first (LBUF) 16-27
- Low-power
 - stop mode enable (STOP)
 - QADC 13-32
 - TPU 17-11
- LR 3-5, 3-18, 17-19
- LSB 13-13
- LSU 3-5, 3-6
- LW0EN 21-51
- LW0IA 21-51
- LW0IADC 21-51
- LW0LA 21-51
- LW0LADC 21-51
- LW0LD 21-51
- LW0LDDC 21-51
- LW1EN 21-51
- LW1IA 21-51
- LW1IADC 21-51
- LW1LA 21-51
- LW1LADC 21-51
- LW1LD 21-51
- LW1LDDC 21-51

-M-

- M 14-46, 14-51
- Machine
 - check enable 3-21
 - state register 3-20
 - status save/restore register 0 3-24
 - status save/restore register 1 3-24
- machine check interrupt, 3-45
- Machine status save/restore register 1 3-24
- Mask
 - examples for normal/extended messages 16-8
 - registers (RX) 16-7

- Master
 - /slave mode select (MSTR) 14-17
- master
 - external
 - arbitration phase, 9-30
- MCE 21-54
- MCEE 21-55
- MCPWM D-21
- ME bit 3-21
- Message
 - buffer
 - address map 16-22
 - code for RX/TX buffers 16-5
 - deactivation 16-13
 - structure 16-3
 - format error (FORMERR) 16-30
- Mid-analog supply voltage 13-13
- MISO 14-33, 14-37
- Mode
 - fault flag (MODF) 14-21, 14-26
 - select (M) 14-46
- Mode Fault Flag (MODF) 14-41
- Modes
 - disabled 13-18
 - reserved 13-18
 - scan. See Scan modes
- MODF 14-21, 14-26, 14-41
- Modulus
 - counter 14-51
- MOSI 14-33, 14-37
- Most significant bit (MSB) 13-13
- MQ1 13-36
- MQ2 13-38
- MSB 13-13
- MSR 3-20, 3-46, 3-48, 3-49, 3-50, 3-51, 3-52
- MSR, 3-45
- MSTR 14-17
- Multichannel pulse-width modulation (MCPWM) D-21
 - parameters
 - master mode D-22
 - slave channel A
 - inverted center aligned mode D-26
 - non-inverted center aligned mode D-24
 - slave channel B
 - inverted center aligned mode D-27
 - non-inverted center aligned mode D-25
 - slave edge-aligned mode D-23
- Multimaster operation 14-26
- Multiphase motor commutation (COMM) D-17
 - parameters D-18, D-19
- Multiple end-of-queue 13-17
- Multiplexed analog inputs 13-5
- MUX 13-8, 13-35

-N-

- New
 - queue pointer value (NEWQP) 14-19
- New input capture/transistion counter (NITC) D-15
 - parameters D-16
- NEWQP 14-19, 14-24



NF 14-49, 14-58
NI bit 3-15
NITC D-15
Noise
 error flag (NF) 14-49
 errors 14-58
 flag (NF) 14-58
Non-IEEE 1149.1-1990 operation 22-7
Non-IEEE floating-point operation 3-15
nonoptional instructions, 3-39
Non-recoverable interrupt 3-26
NOT ACTIVE 16-5
Not ready (NOTRDY) 16-20
NOTRDY 16-16, 16-20
NRI 3-26

-O-

OC D-33
OE bit 3-15
OP0, 9-28
OP1, 9-28
OP2, 9-28
OP3, 9-28
operand placement (effects), 3-43
operand representation (illustration), 9-28
optional instructions, 3-39
OR 14-48
Ordered exceptions 3-34
Output compare (OC) D-33
 parameters D-34
OV (overflow) bit 3-18
Overload frames 16-16
OVERRUN 16-5
Overrun error (OR) 14-48
OX bit 3-14

-P-

P 13-46
Parity
 (PF) flag 14-58
 checking 14-53
 enable (PE) 14-46
 error (PF) bit 14-49
 errors 14-58
 type (PT) 14-46
 type (PT) bit 14-53
Pause (P) 13-15, 13-46
PCBK 17-14
PCS 14-23
 to SCK delay (DSCK) 14-23
PCS0/ \overline{SS} 14-38
PCS3-PCS0/SS 14-41
PE 14-46
Period
 /pulse-width accumulator (PPWA) D-31
 parameters D-32
Periodic
 /interval timer 13-28
Periodic interrupt
 timer 6-15
Peripheral
 chip-selects (PCS) 14-23, 14-36
Peripheral Chip-Select 3-0/Slave Select (PCS3-PC-SO/SS) 14-41
PF 14-49, 14-58
PF1 13-40
PF2 13-40
Phase buffer segment 1/2 (PSEG1/2) bit field 16-28
phase-lock loop, 9-7
PIE1 13-36
PIE2 13-38
PIT 6-15
PLL, 9-7
Pointer 14-15
port size device interfaces (illustration), 9-29
port width, 9-1
PORTQA 13-32, 13-33
PORTQB 13-32, 13-33
PORTQS 14-10
PowerPC standards
 PowerPC Operating Environment Architecture (Book 3)
 branch processor, 3-43
 fixed-point processor
 special purpose registers, 3-44
 fixed-point processor, 3-44
 interrupts, 3-44
 optional facilities and instructions, 3-53
 storage control instructions, 3-44
 timer facilities, 3-53
 PowerPC Operating Environment Architecture (Book 3), 3-43
 PowerPC User Instruction Set Architecture (Book 1)
 branch instructions, 3-40
 branch processor, 3-39
 computation modes, 3-39
 exceptions, 3-39
 fixed point-processor, 3-40
 instruction classes, 3-39
 load/store processor, 3-41
 reserved fields, 3-39
 PowerPC User Instruction Set Architecture (Book 1), 3-39
 PowerPC Virtual Environment Architecture (Book 2)
 operand placement effects, 3-43
 storage control instructions, 3-43
 timebase, 3-43
 PowerPC Virtual Environment Architecture (Book 2), 3-42
 PowerPC User Instruction Set Architecture
 Book 1
 instruction fetching, 3-39
PPWA D-31
PQA 13-8
PQB 13-4, 13-8
PQSPAR 14-9, 14-33, 14-37
PR bit 3-7, 3-21
PRE 21-54
Precise exceptions 3-35



PREE 21-56
 Prescaler 13-25
 clock
 (PSCK) 17-11
 high time (PSH) 13-35
 low time (PSL) 13-35
 clock high time (PSH) 13-25
 control
 for TCR1 17-5
 for TCR2 17-7
 divide
 factor field 16-27
 register (PRES DIV) 16-8, 16-27
 PRES DIV (bit field) 16-27
 PRES DIV (register) 16-8, 16-9, 16-27
 Privilege level 3-7, 3-21
 Processor version register 3-25
 Programmable
 channel service priority 17-4
 transfer length 14-14
 Programmable time accumulator (PTA) D-3
 parameters D-4
 Propagation segment time (PROPSEG) 16-27
 PROPSEG 16-11, 16-27
 PSCK 17-11
 PSEG1 16-28
 PSEG2 16-9, 16-11, 16-28
 PSEGS1 16-11
 PSH 13-25, 13-35
 PSL 13-35
 PT 14-46, 14-53
 PTA D-3
 PTR, 9-4, 9-37
 Pulse-width modulation (PWM) D-35
 parameters D-36, D-43
 PVR 3-25
 PWM D-35

-Q-

QACR0 13-34
 QACR1 13-35
 QACR2 13-38
 QADC
 features 13-2
 pin functions diagram 13-2
 registers
 control register 0 (QACR0) 13-34
 control register 1 (QACR1) 13-35
 control register 2 (QACR2) 13-38
 conversion command word table (CCW) 13-45
 interrupt register (QADCINT) 13-31, 13-32
 module configuration register (QADCMCR) 13-6,
 13-31, 13-32
 port
 A data register (PORTQA) 13-32
 B data register (PORTQB) 13-32
 data direction register (DDRQA) 13-32
 QA data direction register (DDRQA) 13-34
 QA data register (PORTQA) 13-33
 QB data register (PORTQB) 13-33
 status register (QASR) 13-40, 13-41
 test register (QADCTEST) 13-31, 13-32
 QADCINT 13-31, 13-32
 QADCMCR 13-6, 13-31, 13-32
 QADCTEST 13-31, 13-32
 QASR 13-39
 QASR0 13-40
 QASR1 13-41
 QCLK 13-20, 13-23
 frequency 13-24
 QDDR 14-12, 14-41
 QILR 14-8
 QOM D-5
 QPAR 14-11
 QPDR 14-10, 14-41
 QS 13-41
 QSM
 pin function 14-10
 QSPI 14-13
 operating modes 14-26
 operation 14-24
 RAM 14-21
 registers
 pin control registers 14-9
 port QS
 data direction register (DDRQS) 14-9
 data register (PORTQS) 14-10
 QSPI
 control register 0 (SPCR0) 14-16
 control register 1 (SPCR1) 14-17
 control register 2 (SPCR2) 14-18
 control register 3 (SPCR3) 14-19
 status register (SPSR) 14-19
 SCI
 control register 0 (SCCR0) 14-45
 control register 1 (SCCR1) 14-45
 data register (SCDR) 14-49
 status register (SCSR) 14-47
 SCI 14-41
 operation 14-50
 pins 14-50
 registers 14-44
 QSM Data Direction Register (QDDR) 14-12, 14-41
 QSM Interrupt Level Register (QILR) 14-8
 QSM Pin Assignment Register (QPAR) 14-11
 QSM Port Data Register (QPDR) 14-10, 14-41
 QSPI 14-13
 block diagram 14-14
 enable (SPE) 14-18
 finished flag (SPIF) 14-21
 initialization operation 14-27
 loop mode (LOOPQ) 14-20
 master operation flow 14-28
 operating modes 14-26
 master mode 14-26, 14-33
 wraparound mode 14-37
 slave mode 14-26, 14-37
 operation 14-24
 peripheral chip-selects 14-36
 RAM 14-21, 14-22



- command RAM 14-22
 - receive RAM 14-22
 - transmit RAM 14-22
 - QSPI Enable (SPE) 14-41
 - QSPI Status Register (SPSR) 14-41
 - Queue 13-14
 - pointers
 - completed queue pointer (CPTQP) 14-24
 - end queue pointer (ENDQP) 14-24
 - new queue pointer (NEWQP) 14-24
 - status (QS) 13-41
 - Queue 1
 - completion
 - flag (CF1) 13-40
 - interrupt enable (CIE1) 13-36
 - operating mode (MQ1) 13-36
 - pause
 - flag (PF1) 13-40
 - interrupt enable (PIE1) 13-36
 - single-scan enable (SSE1) 13-36
 - trigger overrun (TOR1) 13-40
 - Queue 2
 - completion
 - flag (CF2) 13-40
 - interrupt enable (CIE2) 13-38
 - operating mode (MQ2) 13-38
 - pause
 - flag (PF2) 13-40
 - interrupt enable (PIE2) 13-38
 - resume (RES) 13-38
 - single-scan enable bit (SSE2) 13-38
 - trigger overrun (TOR2) 13-40
 - Queued
 - analog-to-digital converter. See QADC 13-1
 - serial
 - peripheral interface (QSPI) 14-13
 - Queued output match TPU function (QOM) D-5
 - parameters D-6
- R-
- R0 20-3
 - RAF 14-48
 - RD/WR, 9-4
 - RDRF 14-48, 14-57
 - RE 14-44, 14-46, 14-57
 - RE bit 3-22, 3-26
 - read cycle, data bus requirements, 9-30
 - Read only, SRAM 20-3
 - read/write (RD/WR), 9-36
 - Receive
 - data
 - register full (RDRF) 14-48
 - error status flag (RXWARN) 16-30
 - RAM 14-22
 - time sample clock (RT) 14-52, 14-57
 - Receiver
 - active (RAF) 14-48
 - data register (RDRF) flag 14-57
 - enable (RE) 14-46, 14-57
 - interrupt enable (RIE) 14-46
 - wakeup (RWU) 14-47, 14-59
 - Receiver Enable (RE) 14-44
 - Reception of transmitted frames 16-13
 - Recoverable exception 3-22, 3-26
 - Registers
 - CMPA–CMPD 21-45
 - CMPE–CMPF 21-46
 - CMPG–CMPH 21-47
 - COUNTA 21-52
 - COUNTB 21-53
 - DER 21-55
 - ECR 21-53
 - ICTRL 21-47
 - LCTRL1 21-49
 - LCTRL2 21-50
 - supervisor level 3-20
 - test (RAMTST) 18-4
 - user level 3-11
 - registers
 - special purpose
 - added registers, 3-44
 - unsupported registers, 3-44
 - special purpose, 3-44
 - Remote
 - frames 16-15
 - transmission request (RTR) 16-4, 16-5
 - RES 13-38
 - reservation protocol for a multi-level (local) bus, 9-41
 - Reserved
 - channel number 13-46
 - mode 13-18
 - Reset
 - status register 7-5
 - Resistor-divider chain 13-13
 - Resolution time 13-12
 - Result word table 13-1, 13-14, 13-48
 - Resynchronization jump width (RJW) bit field 16-28
 - RETRY, 9-43
 - RIE 14-46
 - Right justified, unsigned result word table (RJURR) 13-48
 - RJURR 13-48
 - RJW 16-11, 16-28
 - RN field 3-15
 - RSR 7-5
 - RSV, 9-37
 - RT 14-57
 - RTR 16-4, 16-5, 16-15
 - RWU 14-47, 14-59
 - RX
 - Length 16-4
 - RX14MSKHI 16-29
 - RX14MSKLO 16-29
 - RX15MSKHI 16-29
 - RX15MSKLO 16-29
 - RXECTR 16-33
 - RXGMSKHI 16-29
 - RXGMSKLO 16-29
 - RXWARN 16-30



- S0 14-8, 20-3
- SAMP 16-27
- Sample amplifier bypass (BYP) 13-46
- Sampling mode (SAMP) 16-27
- SAR 13-14
- SBK 14-47, 14-54
- Scan modes
 - single-scan modes
 - external trigger 13-20
- SCBR 14-45
- SCCR0 14-45
- SCCR1 14-45
- SCDR 14-49
- SCI 14-33, 14-41
 - baud
 - clock 14-51
 - rate (SCBR) 14-45
 - equation 14-45
 - idle-line detection 14-58
 - internal loop 14-59
 - operation 14-50
 - parity checking 14-53
 - pins 14-50
 - receiver
 - block diagram 14-43
 - operation 14-57
 - wakeup 14-59
 - registers 14-44
 - SCCR0 14-44
 - SCCR1 14-44
 - SCI Baud 14-53
 - SCI Baud Rates 14-52, 14-53
 - SCI SUBMODULE 14-12
 - SCSR 14-44
 - transmitter
 - block diagram 14-42
 - operation 14-53
- SCI Control Register 0 (SCCR0) 14-44
- SCI Control Register 1 (SCCR1) 14-44
- SCI Status Register (SCSR) 14-44
- SCK 14-11, 14-32, 14-37
 - actual delay before SCK (equation) 14-35
 - baud rate (equation) 14-34
- S-clock 16-8
- SCSR 14-47
- SE bit 3-21
- SEE 21-54
- Send break (SBK) 14-47, 14-54
- Sequencer, instruction 3-3
- Serial
 - clock baud rate (SPBR) 14-17
 - communication interface (SCI) 14-41
 - formats 14-51
 - mode (M) bit 14-51
 - shifter 14-54
- Serial Clock (SCK) 14-11
- Serialization
 - fetch 21-1
- Service
 - request breakpoint flag (SRBK) 17-14
- SGLR 17-19
- Simplified mnemonics 3-33
- Single-step trace enable 3-21
- SIU
 - module configuration register 6-19
- SIU signals, 9-4
- SIUMCR 6-19
- SIW0EN 21-48
- SIW1EN 21-48
- SIW2EN 21-48
- SIW3EN 21-48
- Slave Select (SS) 14-41
- Slave select signal (\overline{SS}) 14-37, 14-38
- SLW0EN 21-52
- SLW1EN 21-52
- snooping external bus activity, 3-42
- SO bit 3-18
- SOF 16-9
- Soft reset control field (SOFT_RST) 17-20
- SOFT_RST 17-20
- SOFTTRST 16-11
- Software trap enable selection 21-48
- SPBR 14-17
- SPCR0 14-16
- SPCR1 14-17
- SPCR2 14-18
- SPCR3 14-19
- SPE 14-18, 14-41
- Special-purpose registers, general 3-25
- SPI
 - finished interrupt enable (SPIFIE) 14-19
 - TSBD 14-8
- SPI Test Scan Path Select (TSBD) 14-8
- SPIF 14-21
- SPIFIE 14-19
- SPRG0–SPRG3 3-25
- SPRGs 3-25
- SPRs
 - general 3-25
- SPSR 14-19, 14-41
- SPWM D-39
- SRAM
 - data space only 20-3
 - disabling 20-3
 - locking 20-3
 - read only 20-3
 - registers 20-2
 - supervisor space only 14-8, 20-3
 - two-cycle mode 20-3
- SRAMMCR 20-3
- SRBK 17-14
- SRR 16-5
- SRR0 3-24, 3-45, 3-46, 3-48, 3-49, 3-50, 3-51, 3-52
- SRR1 3-24, 3-45, 3-46, 3-48, 3-49, 3-50, 3-51, 3-52
- SS 14-41
- \overline{SS} 14-37, 14-38
- SSE1 13-36
- SSE2 13-38



Standard
 message format 16-1
 frames 16-4
Start
 bit (beginning of data frame) 14-50
 -of-frame (SOF) symbol 16-9
State machine 13-24, 14-57
Status register (QASR) 13-39
STF 17-11
STOP 13-32, 16-17, 17-11
Stop
 clocks to TCRs (CLKS) 17-13
 enable (STOP) bit
 QADC 13-6
 QSM 14-5
 TOUCAN 16-17
 TPU 17-11
 flag (STF) 17-11
 SCI end of data frame bit 14-50
storage control instructions, 3-44
storage reservation, 9-40
STS, 9-5
STUFFERR 16-30
Subqueue 13-15
Substitute remote request (SRR) 16-5
Successive approximation register (SAR) 13-14
Summary overflow 3-18
Supervisor
 /unrestricted data space (SUPV)
 QADC 13-32
 TPU 17-11
Supervisor mode 3-20
 and SRAM 14-8, 20-3
SUPV 13-7, 13-32
SUSG 21-50
SUSH 21-50
Synchronized pulse-width modulation (SPWM) D-39
 parameters D-40, D-41
SYSE 21-54
SYSEE 21-56
system clock output, 9-7
system reset interrupt, 3-45

-T-

T2CFILTER 17-20
T2CG 17-7, 17-11
T2CLK pin filter control (T2CFILTER) 17-20
T2CSL 17-11
TA, 9-6
Table stepper motor (TSM) D-7
 parameters
 master mode D-8
 slave mode D-9
TAP controller 22-3
TB 3-19
TBL 3-20, 3-23
TBU 3-20, 3-23
TC 14-48, 14-54
TCIE 14-46, 14-55
TCK 22-3

TCNMCR 16-22
TCR 17-12
TCR1P 17-11
TCR2 clock/gate control (T2CG) 17-11
TDI 22-3
TDO 22-3
TDRE 14-48
TE 14-44, 14-46
TEA, 9-6
termination signals, 9-38
Test
 access port controller. See TAP controller
 clock 22-3
 data input 22-3
 data output 22-3
 mode select 22-3
 reset 22-3
 test register (RAMTST) 18-4
TICR 17-14, 17-21
TIE 14-46, 14-55
Time
 quanta clock 16-8
 stamp 16-4, 16-10
Time base 3-19
timebase, 3-43
TIMER 16-28
Timer
 count register
 1 prescaler control (TCR1P) 17-11
 synchronize mode (TSYNC) 16-27
Timing, instruction 3-36
TMS 22-3
TOR1 13-40
TOR2 13-40
TOUCAN
 address
 map 16-19
 bit timing configuration 16-8
 operation 16-9
 external pins 16-2
 initialization sequence 16-11
 interrupts 16-18
 message buffer address map 16-22
 operation 16-3
 receive process 16-13
 registers
 control register 0 (CANCTRL0) 16-25
 control register 1 (CTRL1) 16-8
 control register 1(CANCTRL1) 16-26
 control register 2 (CANCTRL2) 16-28
 control register 2 (CTRL2) 16-8
 error and status register (ESTAT) 16-30
 free running timer register (TIMER) 16-28
 interrupt
 configuration register (CANICR) 16-24
 flag register (IFLAG) 16-32
 mask register (IMASK) 16-32
 module configuration register (TCNMCR) 16-22
 receive
 buffer 14 mask registers (RX14MSKHI/LO)



- 16-29
- buffer 15 mask registers (RX15MSKHI/LO) 16-29
- global mask registers (RXGMSKLO/HI) 16-29
- RX/TX error counter registers (RXECTR/TXECTR) 16-33
- test configuration register (CANTCR) 16-24
- special operating modes 16-16
 - auto power save mode 16-18
 - debug mode 16-16
 - low-power stop mode 16-17
- transmit process 16-12

TPU

- address map 17-8
- components 17-2
- FREEZE flag (TPUF) 17-14
- function library 17-4
- host interface 17-2
- interrupts 17-5
- microengine 17-2
- operation 17-3
 - coherency 17-4
 - emulation support 17-4
 - event timing 17-3
 - interchannel communication 17-4
 - programmable channel service priority 17-4
- parameter RAM 17-2, 17-22
 - address map 17-22
- registers
 - channel
 - function select registers (CFSR) 17-15
 - interrupt
 - enable register (CIER) 17-5, 17-15
 - status register (CISR) 17-5, 17-19
 - priority registers (CPR) 17-18
 - decoded channel number register (DCNR) 17-19
 - development
 - support control register (DSCR) 17-12
 - support status register (DSSR) 17-14
 - host
 - sequence registers (HSQR) 17-16
 - service request registers (HSSR) 17-17
 - link register (LR) 17-19
 - module configuration register (TPUMCR) 17-10
 - service grant latch register (SGLR) 17-19
 - test configuration register (TCR) 17-12
 - TPU interrupt configuration register (TICR) 17-14, 17-21
- scheduler 17-2
- time
 - bases 17-2
- timer channels 17-2

TPU Reference Manual 17-3, 17-17

TPU2

- module configuration register 2 (TPUMCR2) 17-20

TPUF 17-14

TPUMCR 17-10

TPUMCR2 17-20

TR 21-54

- trace interrupt, 3-47
- transaction (bus), 9-8
- Transfer
 - length options 14-36
- transfer acknowledge (TA), 9-38
- transfer error acknowledge (TEA), 9-39
- transfer size (TSIZ), 9-37
- transfer start (TS), 9-36
- transfers, alignment and packaging, 9-28
- transfers, burst-inhibited, 9-16
- transfers, termination signals, 9-39
- Transmission
 - complete
 - (TC) flag 14-54
 - interrupt enable (TCIE) 14-55
- Transmit
 - /receive status (TX/RX) 16-31
 - bit error (BITERR) 16-30
 - complete
 - bit (TC) 14-48
 - interrupt enable (TCIE) 14-46
 - data
 - register empty (TDRE) flag 14-48
 - error status flag (TXWARN) 16-30
 - interrupt enable (TIE) 14-46, 14-55
 - pin configuration control (TXMODE) 16-25
 - RAM 14-22
- Transmitter Enable (TE) 14-44
- Transmitter enable (TE) 14-46, 14-53
- TRE 21-56
- Trigger
 - event 13-43
- TRST 22-3
- TS, 9-5
- TSIZ(0) 1, 9-4
- TSIZ0, 9-1
- TSIZ1, 9-1
- TSM D-7
- T_{SR} 13-6
- TSYNC 16-27
- Two-cycle mode, SRAM 20-3
- TX
 - Length 16-4
- TX/RX 16-31
- TXECTR 16-33
- TXMODE 16-25
- TXWARN 16-30

-U-

- UART D-12
- UISA register set 3-11
- Universal asynchronous receiver/transmitter (UART) D-12
 - parameters
 - receiver parameters D-14
 - transmitter parameters D-13
- Unordered exceptions 3-34
- User level registers 3-11
- Using the TPU Function Library and TPU Emulation

Mode 17-4
UX bit 3-14

-Z-

ZE bit 3-15
ZX bit 3-14



-V-

VCO 14-52
V_{DD} 13-5
V_{DDA} 13-5
V_{DDA/2} 13-13
VE bit 3-15
Vector table, exception 3-36
Vector table, exceptions 3-35
V_{IH} 13-7
V_{IL} 13-7
Voltage
 reference pins 13-5
V_{RH} 13-5, 13-13, 13-46
V_{RL} 13-5, 13-13, 13-46
V_{SS} 13-5
V_{SSA} 13-5
VX bit 3-14
VXCVI bit 3-15
VXIDI 3-14
VXIMZ bit 3-14
VXISI 3-14
VXSNAN 3-14
VXSOFRT bit 3-15
VXSQRT bit 3-15
VXVC bit 3-14
VXZDZ bit 3-14

-W-

WAKE 14-46, 14-59
Wake interrupt (WAKEINT) 16-31
WAKEINT 16-17, 16-31
WAKEMSK 16-17
Wakeup
 address mark (WAKE) 14-46, 14-59
Wired-OR
 mode
 for QSPI pins (WOMQ) 14-17
 for SCI pins (WOMS) 14-46, 14-54
WOMQ 14-17
WOMS 14-46, 14-54
Wrap
 enable (WREN) 14-19
 to (WRTO) 14-19
Wraparound mode 14-15
 master 14-37
WREN 14-19
write cycle data bus contents, 9-30
WRTO 14-19

-X-

XE bit 3-15
XER 3-17
XX bit 3-14

