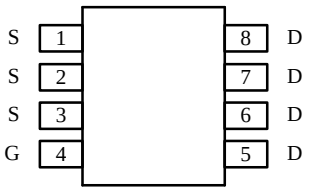
P-Channel Enhancement-Mode MOSFET

Product Summary

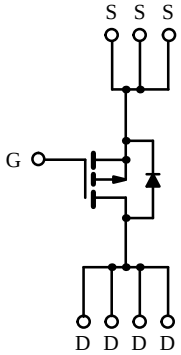
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–20	0.050 @ V_{GS} = –10 V	± 5.8
	0.065 @ V_{GS} = –6 V	± 4.9
	0.090 @ V_{GS} = –4.5 V	± 4.0

Recommended upgrade: Si4435DY or Si4953DY
Lower profile/smaller size see Si6435DQ

SO-8



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–20	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 5.8	A
	T_A = 70°C		± 4.6	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction)[a]		I_S	–2.4	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	50	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70124.
A SPICE Model data sheet is available for this product (FaxBack document #70512).

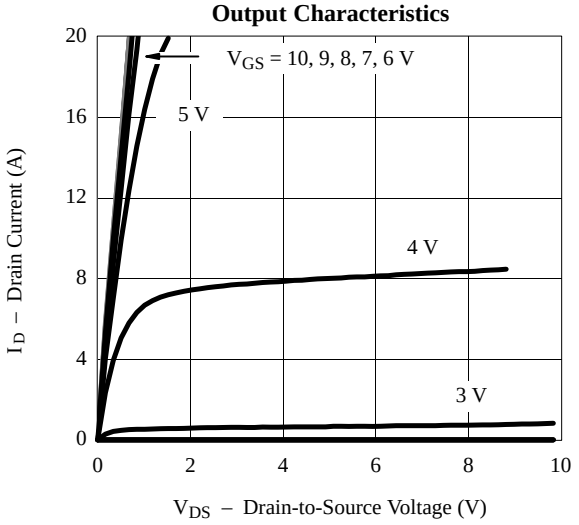
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –250 µA	–1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –16 V, V_{GS} = 0 V			–1	µA
		V_{DS} = –10 V, V_{GS} = 0 V, T_J = 70°C			–5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≤ –5 V, V_{GS} = –10 V	–20			A
		V_{DS} ≤ –5 V, V_{GS} = –4.5 V	–5			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = –10 V, I_D = –5.3 A		0.033	0.050	Ω
		V_{GS} = –6 V, I_D = –3.6 A		0.042	0.065	
		V_{GS} = –4.5 V, I_D = –2.0 A		0.056	0.090	
Forward Transconductance[b]	g_{fs}	V_{DS} = –15 V, I_D = –5.3 A		9.5		S
Diode Forward Voltage[b]	V_{SD}	I_S = –2.4 A, V_{GS} = 0 V		–0.76	–1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = –10 V, V_{GS} = –10 V, I_D = –5.3 A		27	50	nC
Gate-Source Charge	Q_{gs}			4.5		
Gate-Drain Charge	Q_{gd}			5.6		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –10 V, R_L = 10 Ω I_D ≅ –1 A, V_{GEN} = –10 V, R_G = 6 Ω		15	30	ns
Rise Time	t_r			25	60	
Turn-Off Delay Time	$t_{d(off)}$			56	120	
Fall Time	t_f			23	100	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = –2.4 A, di/dt = 100 A/µs		65	100	

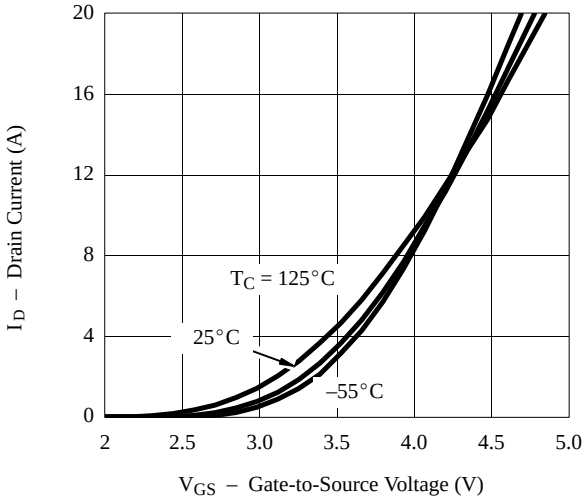
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)

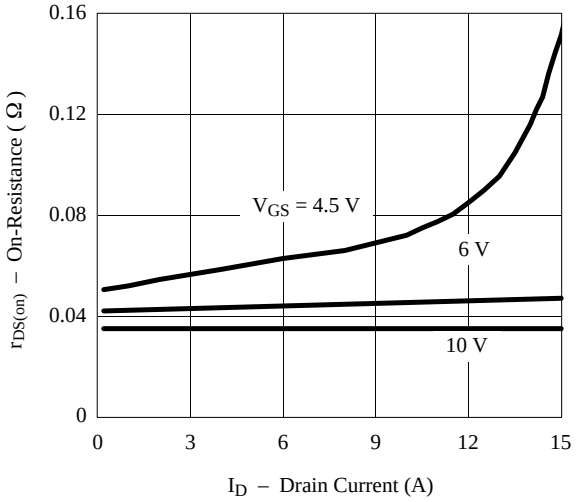
Output Characteristics



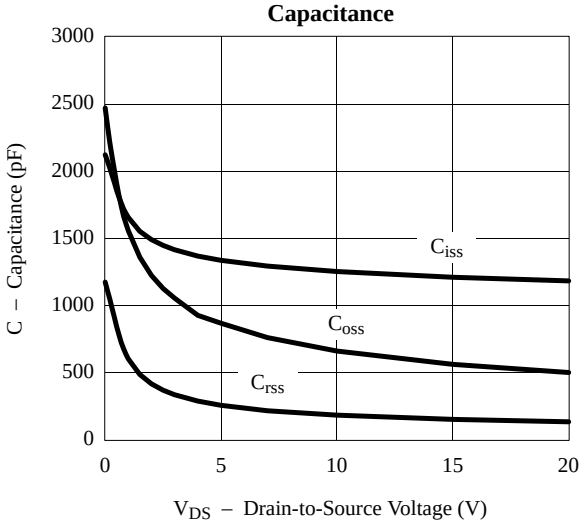
Transfer Characteristics



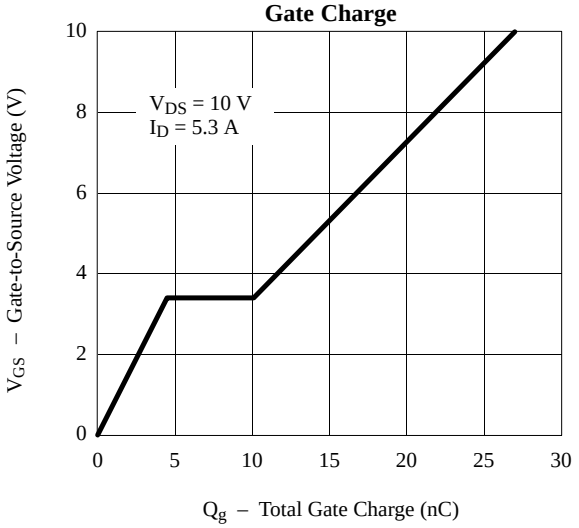
On-Resistance vs. Drain Current



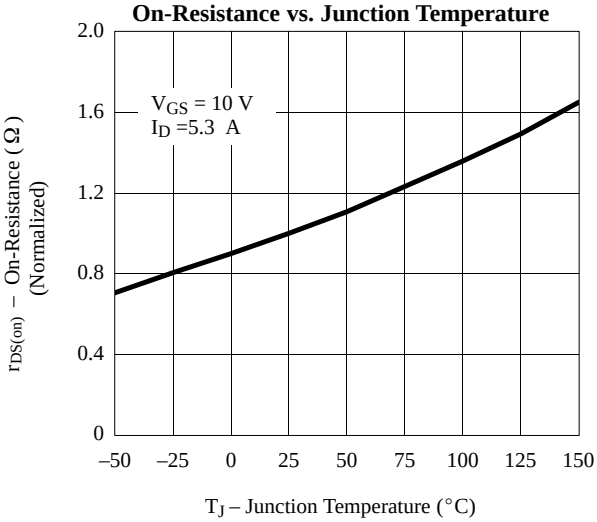
Capacitance



Gate Charge

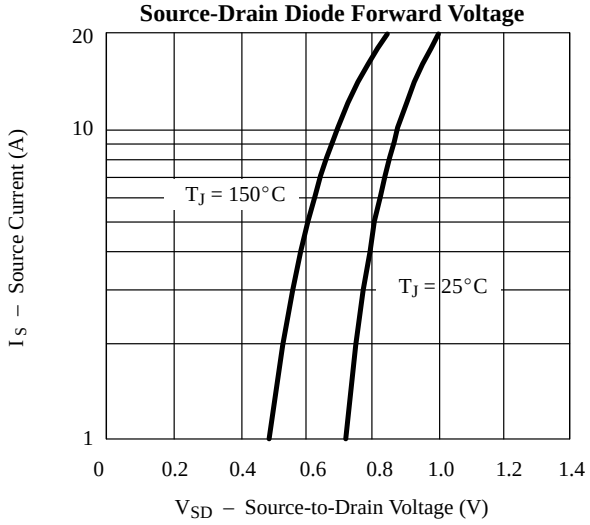


On-Resistance vs. Junction Temperature

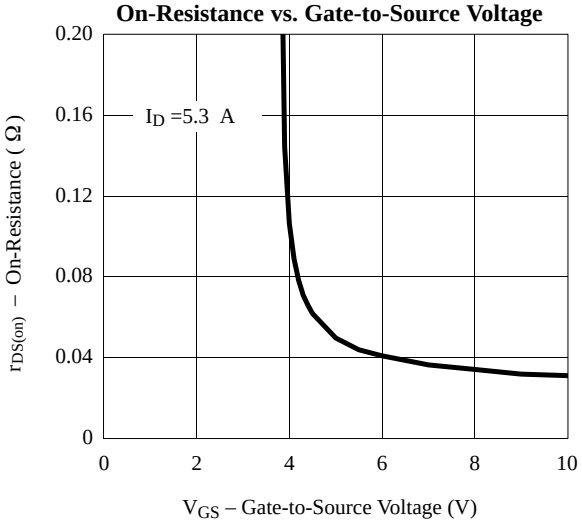


Typical Characteristics (25°C Unless Otherwise Noted)

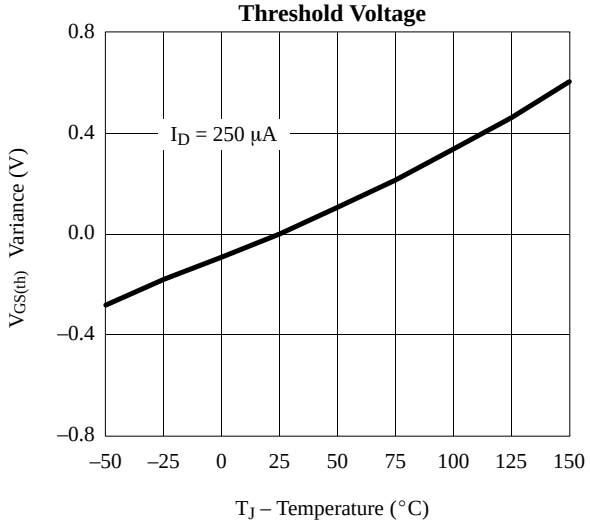
Source-Drain Diode Forward Voltage



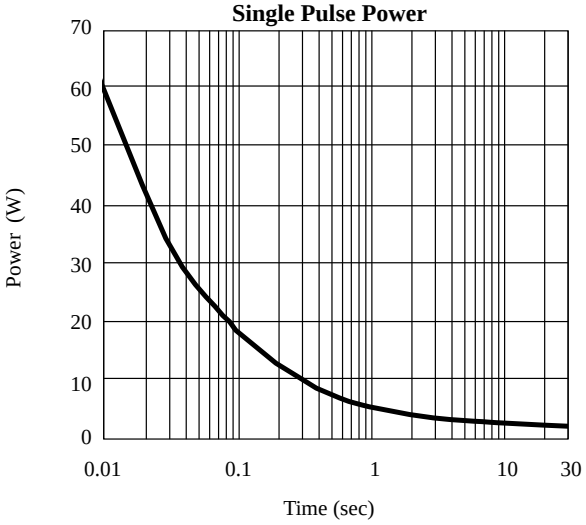
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient